LM5112

LM5112 Tiny 7A MOSFET Gate Driver

Literature Number: SNVS234B

National Semiconductor

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LM5112
Tiny 7A MOSFET Gate Driver

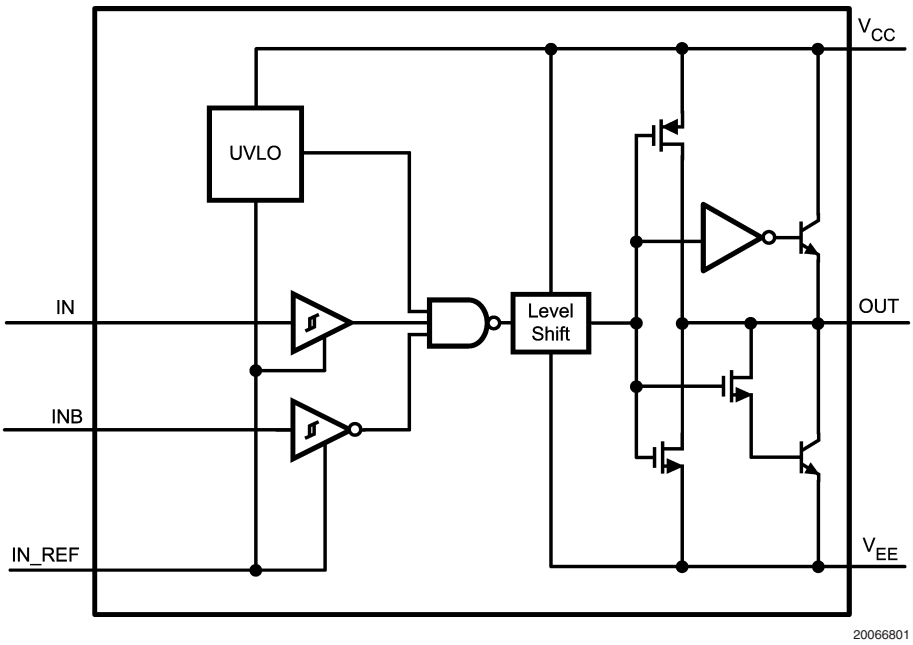
General Description

The LM5112 MOSFET gate driver provides high peak gate drive current in the tiny LLP-6 package (SOT23 equivalent footprint) or an 8-Lead exposed-pad MSOP package, with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turn-on voltage. The LM5112 provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

Features

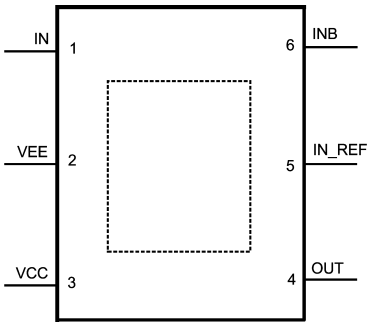
- Compound CMOS and bipolar outputs reduce output current variation
- 7A sink/3A source current
- Fast propagation times (25 ns typical)
- Fast rise and fall times (14 ns/12 ns rise/fall with 2 nF load)
- Inverting and non-inverting inputs provide either configuration with a single device
- Supply rail under-voltage lockout protection
- Dedicated input ground (IN_REF) for split supply or single supply operation
- Power Enhanced 6-pin LLP package (3.0mm x 3.0mm) or thermally enhanced MSOP8-EP package
- Output swings from V_{CC} to V_{EE} which can be negative relative to input ground

Block Diagram

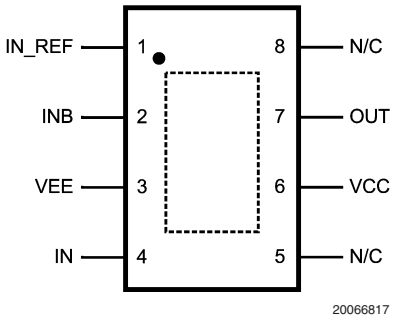


Block Diagram of LM5112

Pin Configurations



LLP-6



MSOP8-EP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5112MY	Exposed DAP MSOP8-EP	MUY08A	1000 shipped in Tape & Reel
LM5112MYX	Exposed DAP MSOP8-EP	MUY08A	3500 shipped in Tape & Reel
LM5112SD	LLP-6	SDE06A	1000 shipped in Tape & Reel
LM5112SDX	LLP-6	SDE06A	4500 shipped in Tape & Reel

Pin Descriptions

Pin		Name	Description	Application Information
LLP-6	MSOP-8			
1	4	IN	Non-inverting input pin	TTL compatible thresholds. Pull up to VCC when not used.
2	3	VEE	Power ground for driver outputs	Connect to either power ground or a negative gate drive supply for positive or negative voltage swing.
3	6	VCC	Positive Supply voltage input	Locally decouple to VEE. The decoupling capacitor should be located close to the chip.
4	7	OUT	Gate drive output	Capable of sourcing 3A and sinking 7A. Voltage swing of this output is from VEE to VCC.
5	1	IN_REF	Ground reference for control inputs	Connect to power ground (VEE) for standard positive only output voltage swing. Connect to system logic ground when VEE is connected to a negative gate drive supply.
6	2	INB	Inverting input pin	TTL compatible thresholds. Connect to IN_REF when not used.
- - -	5, 8	N/C	Not internally connected	
- - -	- - -	Exposed Pad	Exposed Pad, underside of package	Internally bonded to the die substrate. Connect to VEE ground pin for low thermal impedance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to V_{EE}	–0.3V to 15V
V_{CC} to IN_REF	–0.3V to 15V
IN/INB to IN_REF	–0.3V to 15V
IN_REF to V_{EE}	–0.3V to 5V
Storage Temperature Range	–55˚C to +150˚C
Maximum Junction Temperature	+150˚C
Operating Junction Temperature	–40˚C+125˚C
ESD Rating	2kV

Electrical Characteristics

T_J = –40˚C to +125˚C, V_{CC} = 12V, INB = IN_REF = V_{EE} = 0V, No Load on output, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
V_{CC}	V_{CC} Operating Range	V_{CC} – IN_REF and V_{CC} - V_{EE}	3.5		14	V
UVLO	V_{CC} Under-voltage Lockout (rising)	V_{CC} – IN_REF	2.4	3.0	3.5	V
V_{CCH}	V_{CC} Under-voltage Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current			1.0	2.0	mA
CONTROL INPUTS						
V_{IH}	Logic High		2.3			V
V_{IL}	Logic Low				0.8	V
V_{thH}	High Threshold		1.3	1.75	2.3	V
V_{thL}	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN = INB = 0V	-1	0.1	1	µA
I_{IH}	Input Current High	IN = INB = V_{CC}	-1	0.1	1	µA
OUTPUT DRIVER						
R_{OH}	Output Resistance High	I_{OUT} = -10mA (Note 2)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = 10mA (Note 2)		1.4	2.5	Ω
I_{SOURCE}	Peak Source Current	OUT = V_{CC}/2, 200ns pulsed current		3		A
I_{SINK}	Peak Sink Current	OUT = V_{CC}/2, 200ns pulsed current		7		A
SWITCHING CHARACTERISTICS						
td1	Propagation Delay Time Low to High, IN/ INB rising (IN to OUT)	C_{LOAD} = 2 nF, see *Figure 1*		25	40	ns
td2	Propagation Delay Time High to Low, IN / INB falling (IN to OUT)	C_{LOAD} = 2 nF, see *Figure 1*		25	40	ns
tr	Rise time	C_{LOAD} = 2 nF , see *Figure 1*		14		ns
tf	Fall time	C_{LOAD} = 2 nF , see *Figure 1*		12		ns
LATCHUP PROTECTION						
	AEC –Q100, METHOD 004	T_J = 150˚C		500		mA
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient, 0 LFPM Air Flow	LLP-6 Package MSOP8-EP Package		40 60		˚C/W
θ_{JC}	Junction to Case	LLP-6 Package MSOP8-EP Package		7.5 4.7		˚C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

Timing Waveforms

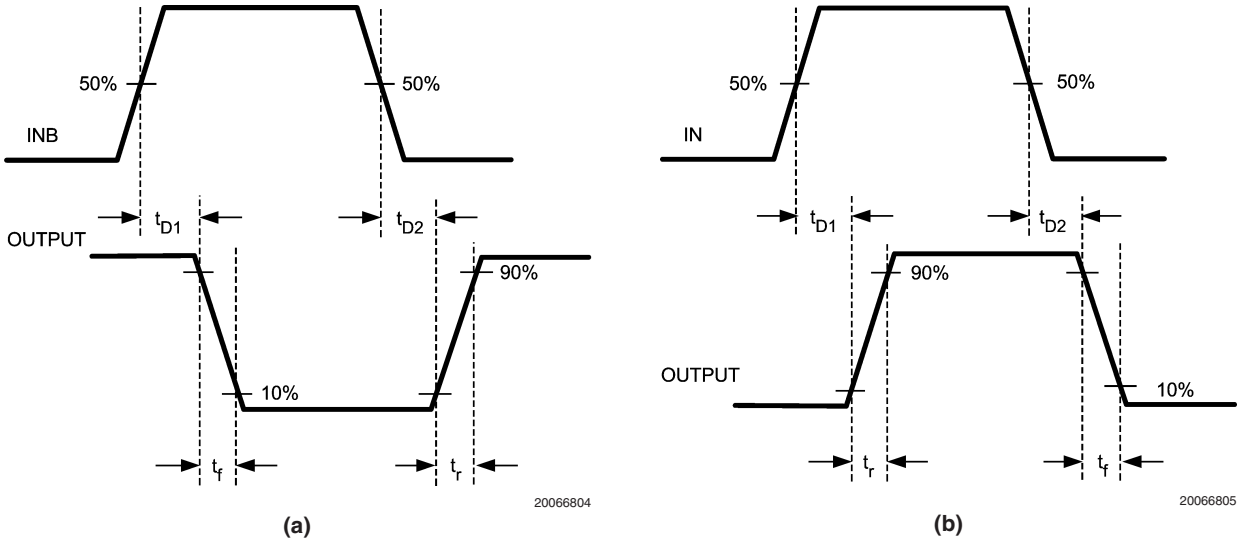
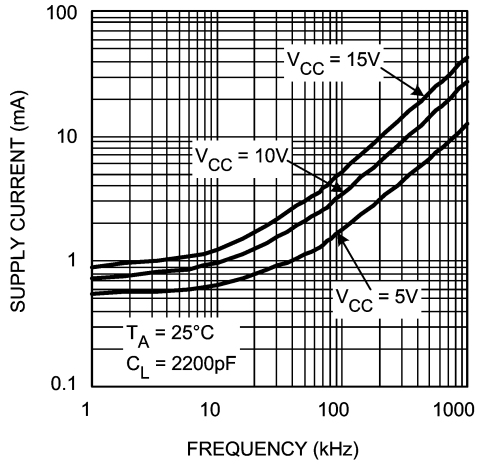


FIGURE 1. (a) Inverting, (b) Non-Inverting

Typical Performance Characteristics

Supply Current vs Frequency



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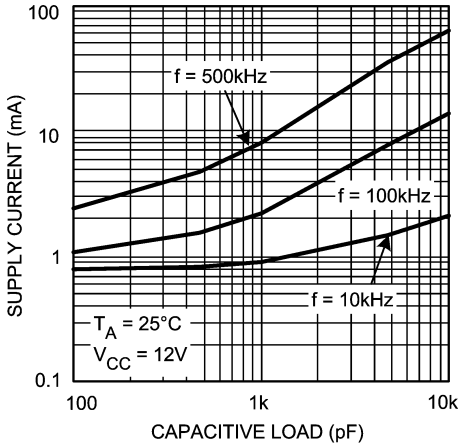
Supply Current vs Capacitive Load



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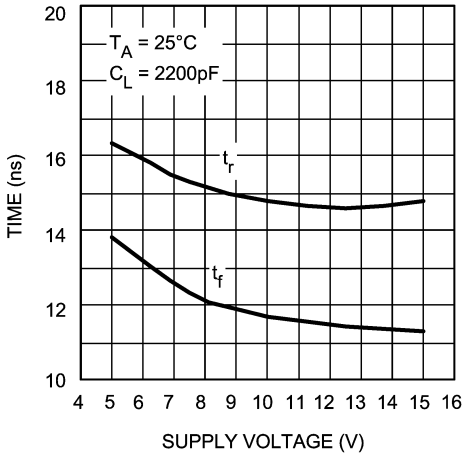
Rise and Fall Time vs Supply Voltage



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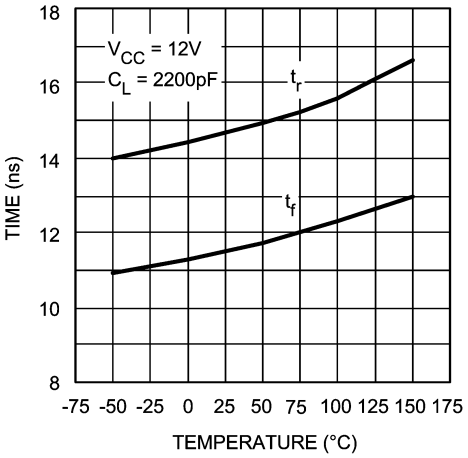
Rise and Fall Time vs Temperature



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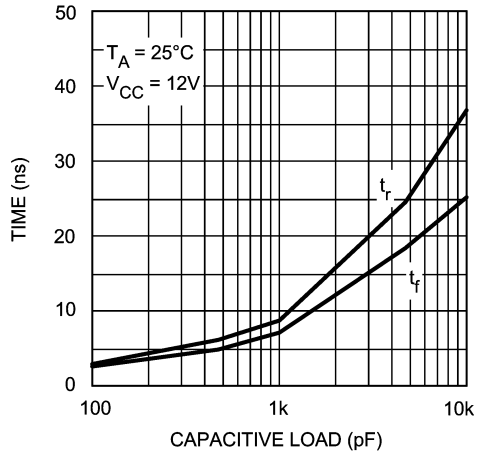
Rise and Fall Time vs Capacitive Load



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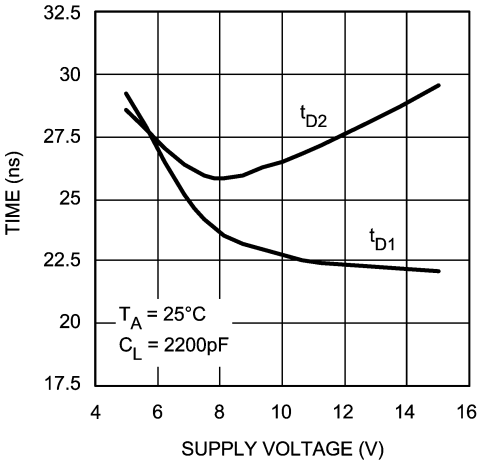
Delay Time vs Supply Voltage



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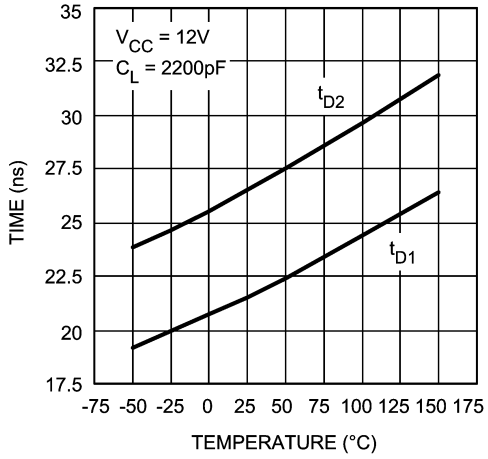
Typical Performance Characteristics (Continued)

Delay Time vs Temperature



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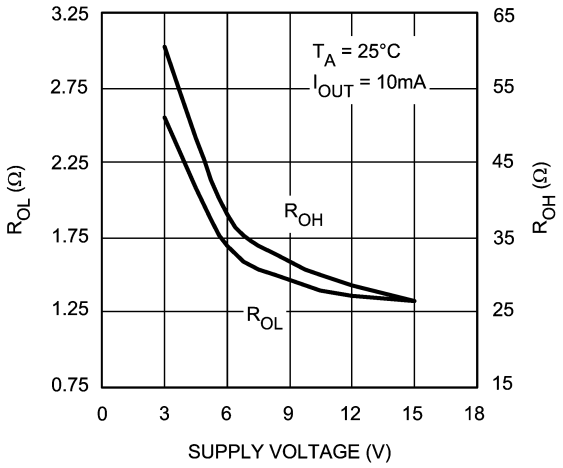
RDSON vs Supply Voltage



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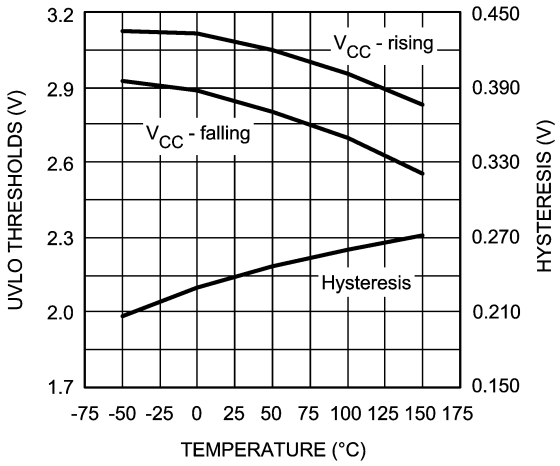
UVLO Thresholds and Hysteresis vs Temperature



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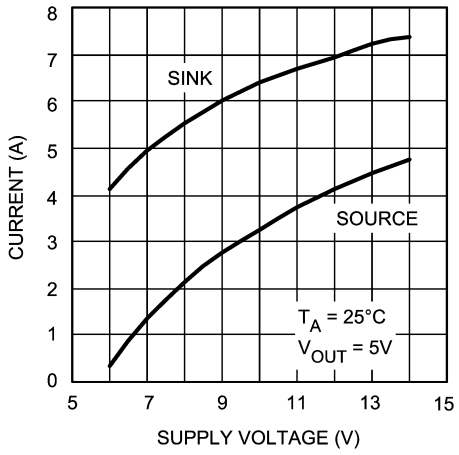
Peak Current vs Supply Voltage



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Simplified Application Block Diagram

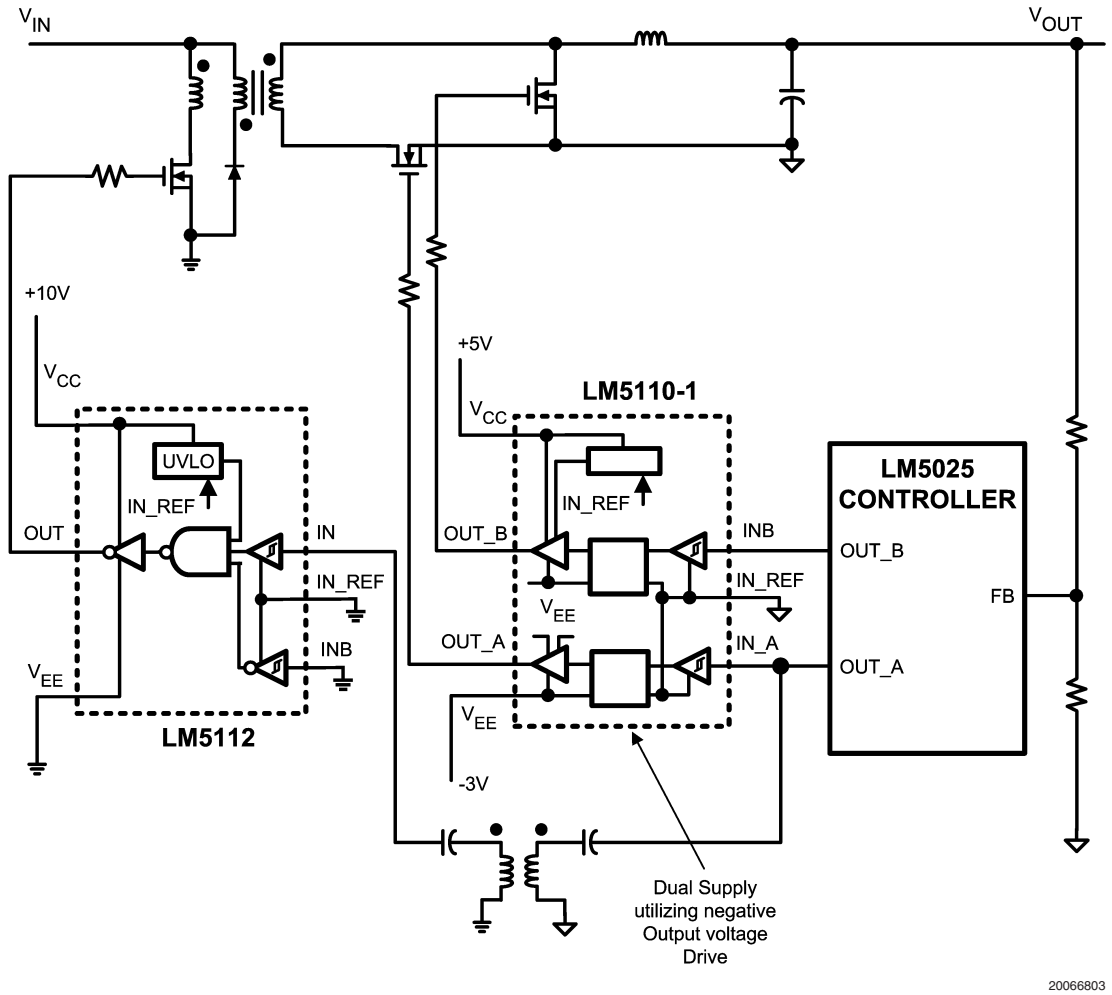


FIGURE 2. Simplified Application Block Diagram

Detailed Operating Description

The LM5112 is a high speed , high peak current (7A) single channel MOSFET driver. The high peak output current of the LM5112 will switch power MOSFET's on and off with short rise and fall times, thereby reducing switching losses considerably. The LM5112 includes both inverting and non-inverting inputs that give the user flexibility to drive the MOSFET with either active low or active high logic signals. The driver output stage consists of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical Miller plateau region of the MOSFET V_{GS} , while the MOS device provides rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

The control inputs of the driver are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and separate input/output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gates from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground.

The isolated input and output stage grounds provide the capability to drive the MOSFET to a negative V_{GS} voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the LM5112 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN_REF potential to as low as 14 V below the Vcc gate drive supply. For reliable operation, the maximum voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14V.

The minimum recommended operating voltage between Vcc and IN_REF is 3.5V. An Under Voltage Lock Out (UVLO) circuit is included in the LM5112 which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.8V the driver is disabled and the output pin is held in the low state. The UVLO hysteresis prevents chattering during

Detailed Operating Description

(Continued)

brown-out conditions; the driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds 3.0V.

Layout Considerations

Attention must be given to board layout when using LM5112. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The driver needs a very low impedance path for current return to ground avoiding inductive loops. Two paths for returning current to ground are a) between LM5112 IN_REF pin and the ground of the circuit that controls the driver inputs and b) between LM5112 V_{EE} pin and the source of the power MOSFET being driven. Both paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. These ground paths should be distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5112. With rise and fall times in the range of 10 to 30nsec, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated when driving large capacitive loads.
3. If either channel is not being used, the respective input pin (IN or INB) should be connected to either V_{EE} or V_{CC} to avoid spurious output signals.

Thermal Performance

INTRODUCTION

The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (Tj) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components should be estimated in worst case operating conditions. The junction temperature can be calculated based on the power dissipated on the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the PCB design and the operating environment.

DRIVE POWER REQUIREMENT CALCULATIONS IN LM5112

LM5112 is a single low side MOSFET driver capable of sourcing / sinking 3A / 7A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.

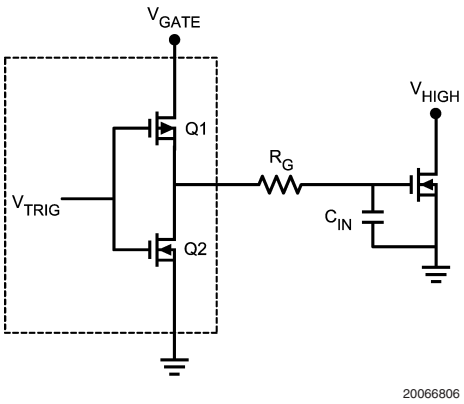


FIGURE 3.

The schematic above shows a conceptual diagram of the LM5112 output and MOSFET load. Q1 and Q2 are the switches within the gate driver. Rg is the gate resistance of the external MOSFET, and Cin is the equivalent gate capacitance of the MOSFET. The equivalent gate capacitance is a difficult parameter to measure as it is the combination of Cgs (gate to source capacitance) and Cgd (gate to drain capacitance). The Cgd is not a constant and varies with the drain voltage. The better way of quantifying gate capacitance is the gate charge Qg in coloumbs. Qg combines the charge required by Cgs and Cgd for a given gate drive voltage Vgate. The gate resistance Rg is usually very small and losses in it can be neglected. The total power dissipated in the MOSFET driver due to gate charge is approximated by:

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

Where

F_{SW} = switching frequency of the MOSFET.

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12V.

Therefore, the power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12V is equal to

$$P_{DRIVER} = 12V \times 30\ nC \times 300\ kHz = 0.108W.$$

In addition to the above gate charge power dissipation, -transient power is dissipated in the driver during output transitions. When either output of the LM5112 changes state, current will flow from V_{CC} to V_{EE} for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the LM5112 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V V_{GATE} supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

$$P_D = 0.118 + 0.008 + 0.012 = 0.138W.$$

We know that the junction temperature is given by

$$T_J = P_D \times \theta_{JA} + T_A$$

Or the rise in temperature is given by

$$T_{RISE} = T_J - T_A = P_D \times \theta_{JA}$$

Thermal Performance (Continued)

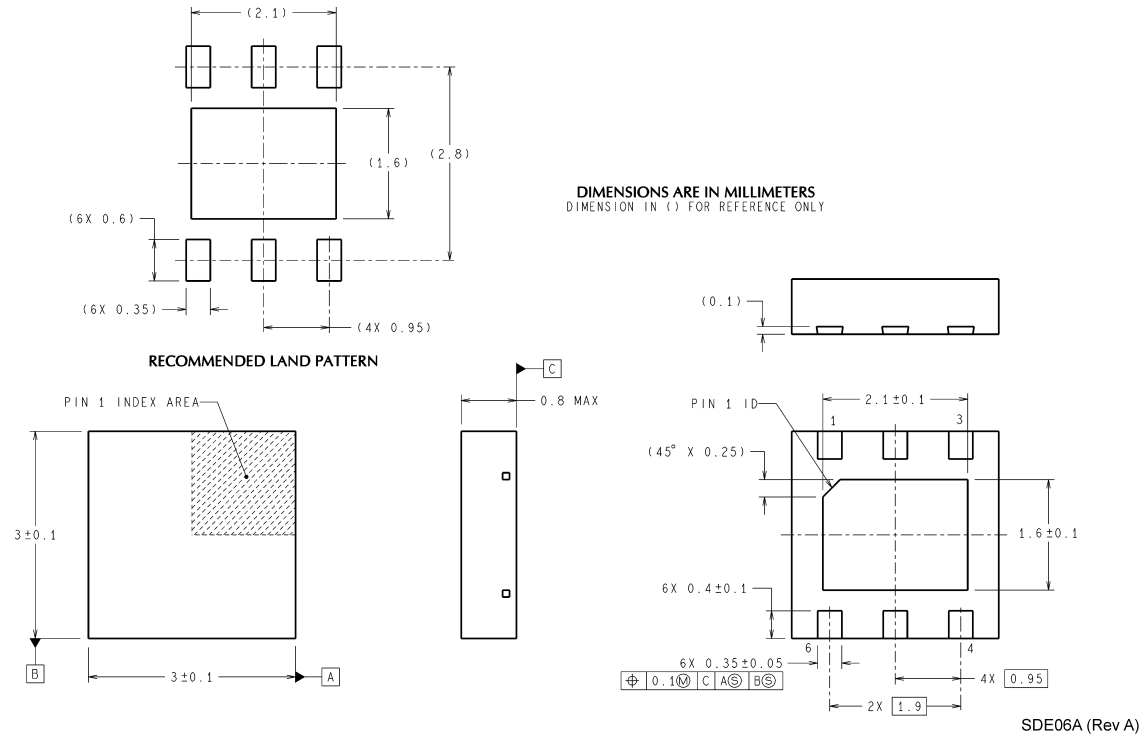
For LLP-6 package, the integrated circuit die is attached to leadframe die pad which is soldered directly to the printed circuit board. This substantially decreases the junction to ambient thermal resistance (θ_{JA}). By providing suitable means of heat dispersion from the IC to the ambient through exposed copper pad, which can readily dissipate heat to the surroundings, θ_{JA} as low as 40˚C / Watt is achievable with the package. The resulting Trise for the driver example above is thereby reduced to just 5.5 degrees.

Therefore T_{RISE} is equal to

$$T_{RISE} = 0.138 \times 40 = 5.5^{\circ}C$$

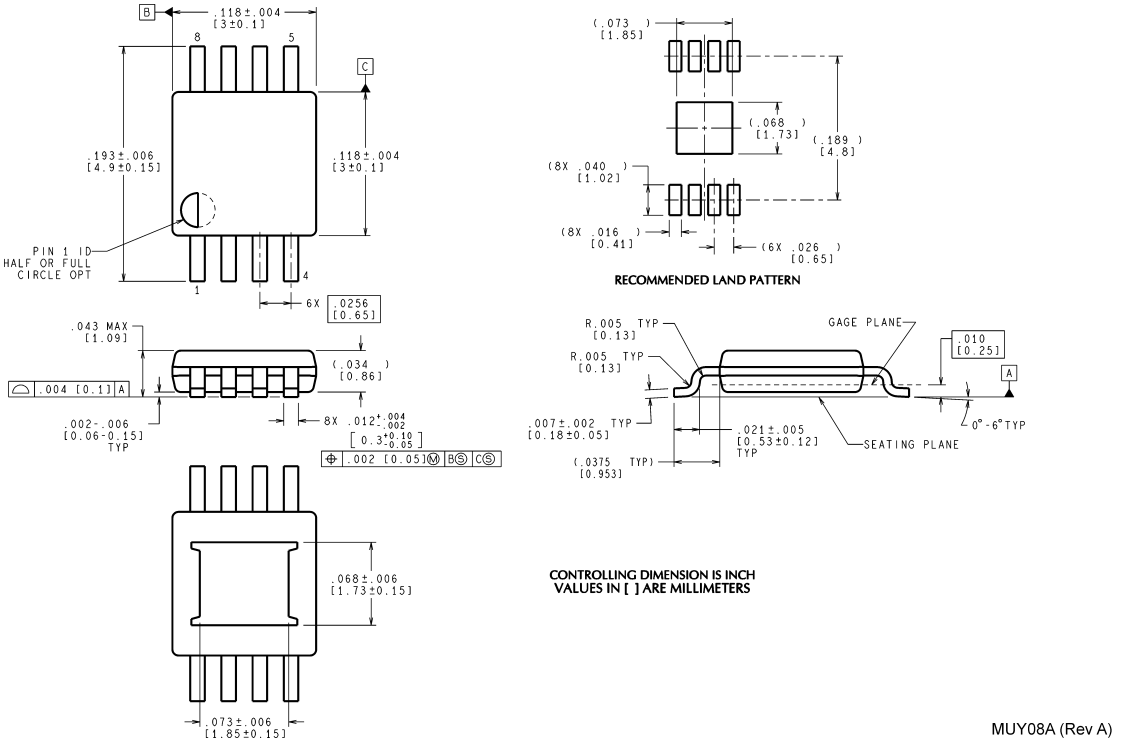
For MSOP8-EP θ_{JA} is typically 60˚C/W.

Physical Dimensions inches (millimeters) unless otherwise noted



SDE06A (Rev A)

6-Lead LLP Package
NS Package Number SDE06A



MUY08A (Rev A)

8-Lead eMSOP-8 Package
NS Package Number MUY08A

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