



# AD565A\*/AD566A\*

### Low Cost

The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, non saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.

DIGITAL-TO-ANALOG CONVERTERS 2-63

# SPECIFICATIONS

( $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ , unless otherwise specified)

MODEL	AD565AJ			AD565AK			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
<b>DATA INPUTS<sup>1</sup> (Pins 13 to 24)</b>							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	$\mu\text{A}$
Bit OFF Logic "0"		+35	+100		+35	+100	$\mu\text{A}$
<b>RESOLUTION</b>			12			12	Bits
<b>OUTPUT</b>							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	$\pm 0.8$	$\pm 1.0$	$\pm 1.2$	$\pm 0.8$	$\pm 1.0$	$\pm 1.2$	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	$\Omega$
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, $R_2 = 50\Omega$ fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
$T_{\min}$ to $T_{\max}$	-1.5		+10	-1.5		+10	V
<b>ACCURACY (error relative to full scale) <math>+25^{\circ}\text{C}</math></b>							
		$\pm 1/4$	$\pm 1/2$		$\pm 1/8$	$\pm 1/4$	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
$T_{\min}$ to $T_{\max}$		$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
<b>DIFFERENTIAL NONLINEARITY <math>+25^{\circ}\text{C}</math></b>							
$T_{\min}$ to $T_{\max}$		$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$	LSB
<b>TEMPERATURE COEFFICIENTS</b>							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/ $^{\circ}\text{C}$
Bipolar Zero		5	10		5	10	ppm/ $^{\circ}\text{C}$
Gain (Full Scale)		15	50		10	20	ppm/ $^{\circ}\text{C}$
Differential Nonlinearity		2			2		ppm/ $^{\circ}\text{C}$
<b>SETTLING TIME TO <math>1/2\text{LSB}</math></b>							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
<b>FULL SCALE TRANSITION</b>							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
<b>TEMPERATURE RANGE</b>							
Operating	0		+70	0		+70	$^{\circ}\text{C}$
Storage	-65		+150	-65		+150	$^{\circ}\text{C}$
<b>POWER REQUIREMENTS</b>							
$V_{CC}$ , +11.4 to +16.5V dc		3	5		3	5	mA
$V_{EE}$ , -11.4 to -16.5V dc		-12	-18		-12	-18	mA
<b>POWER SUPPLY GAIN SENSITIVITY<sup>2</sup></b>							
$V_{CC} = +11.4$ to $+16.5\text{V}$ dc		3	10		3	10	ppm of F.S./%
$V_{EE} = -11.4$ to $-16.5\text{V}$ dc		15	25		15	25	ppm of F.S./%
<b>PROGRAMMABLE OUTPUT</b>							
RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
<b>EXTERNAL ADJUSTMENTS</b>							
Gain Error with Fixed $50\Omega$							
Resistor for $R_2$ (Figure 2)		$\pm 0.1$	$\pm 0.25$		$\pm 0.1$	$\pm 0.25$	% of F.S. Range
Bipolar Zero Error with Fixed $50\Omega$ Resistor for $R_1$ (Figure 3)		$\pm 0.05$	$\pm 0.15$		$\pm 0.05$	$\pm 0.1$	% of F.S. Range
Gain Adjustment Range (Figure 2)	$\pm 0.25$			$\pm 0.25$			% of F.S. Range
Bipolar Zero Adjustment Range	$\pm 0.15$			$\pm 0.15$			% of F.S. Range
<b>REFERENCE INPUT</b>							
Input Impedance	15k	20k	25k	15k	20k	25k	$\Omega$
<b>REFERENCE OUTPUT</b>							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads) <sup>3</sup>	1.5	2.5		1.5	2.5		mA
<b>POWER DISSIPATION</b>		225	345		225	345	mW

## NOTES

<sup>1</sup> The digital inputs are guaranteed but not tested over the operating temperature range.

<sup>2</sup> The power supply gain sensitivity is tested in reference to a  $V_{CC}$ ,  $V_{EE}$  of  $\pm 15\text{V}$  dc.

<sup>3</sup> For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied. Specifications subject to change without notice.

MODEL	MIN	AD565AS TYP	MAX	MIN	AD565AT TYP	MAX	UNITS
DATA INPUTS <sup>1</sup> (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R <sub>2</sub> = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T <sub>min</sub> to T <sub>max</sub>	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C							
		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S. Range
T <sub>min</sub> to T <sub>max</sub>		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY +25°C							
T <sub>min</sub> to T <sub>max</sub>		±1/2	±3/4		±1/4	±1/2	LSB
MONOTONICITY GUARANTEED							
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V <sub>CC</sub> , +11.4 to +16.5V dc		3	5		3	5	mA
V <sub>EE</sub> , -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>							
V <sub>CC</sub> = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V <sub>EE</sub> = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGES (see Figures 2, 3, 4)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads) <sup>3</sup>	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION							
		225	345		225	345	mW

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

# SPECIFICATIONS $(T_A = +25^\circ\text{C}, V_{EE} = -15\text{V}, \text{ unless otherwise specified})$

MODEL	AD566AJ			AD566AK			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS <sup>1</sup> (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	$\mu$ A
Bit OFF Logic "0"		+35	+100		+35	+100	$\mu$ A
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	$\pm 0.8$	$\pm 1.0$	$\pm 1.2$	$\pm 0.8$	$\pm 1.0$	$\pm 1.2$	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	$\Omega$
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R <sub>1</sub> and R <sub>2</sub> = 50 $\Omega$ fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T <sub>min</sub> to T <sub>max</sub>	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C							
		$\pm 1/4$ (0.006)	$\pm 1/2$ (0.012)		$\pm 1/8$ (0.003)	$\pm 1/4$ (0.006)	LSB % of F.S.R.
T <sub>min</sub> to T <sub>max</sub>		$\pm 1/2$ (0.012)	$\pm 3/4$ (0.018)		$\pm 1/4$ (0.006)	$\pm 1/2$ (0.012)	LSB % of F.S.R.
DIFFERENTIAL NONLINEARITY +25°C							
T <sub>min</sub> to T <sub>max</sub>		$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$	LSB
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V <sub>EE</sub> = -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>							
V <sub>EE</sub> = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50 $\Omega$ Resistor for R <sub>2</sub> (Figure 3)		$\pm 0.1$	$\pm 0.25$		$\pm 0.1$	$\pm 0.25$	% of F.S.R.
Bipolar Zero Error with Fixed 50 $\Omega$ Resistor for R <sub>1</sub> (Figure 4)		$\pm 0.05$	$\pm 0.15$		$\pm 0.05$	$\pm 0.1$	% of F.S.R.
Gain Adjustment Range (Figure 3)	$\pm 0.25$			$\pm 0.25$			% of F.S.R.
Bipolar Zero Adjustment Range	$\pm 0.15$			$\pm 0.15$			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	$\Omega$
POWER DISSIPATION							
		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants	Two (2)- Bipolar Operation at Digital Input Only						
Reference Voltage	+1V to +10V, Unipolar						
Accuracy	10 Bits ( $\pm 0.05\%$ of Reduced F.S.) for 1V dc Reference Voltage						
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ						
Output Slew Rate 10%-90%	5mA/ $\mu$ s						
90%-10%	1mA/ $\mu$ s						
Output Settling Time (all bits on and a 0-10V step change in reference voltage)	1.5 $\mu$ s to 0.01% F.S.						
CONTROL AMPLIFIER							
Full Power Bandwidth	300kHz						
Small-Signal Closed-Loop Bandwidth	1.8MHz						

## NOTES

<sup>1</sup> The digital input levels are guaranteed but not tested over the temperature range.

<sup>2</sup> The power supply gain sensitivity is tested in reference to a V<sub>EE</sub> of -15V dc.

Specifications subject to change without notice.

MODEL	AD566AS			AD566AT			UNITS	
	MIN	TYP	MAX	MIN	TYP	MAX		
DATA INPUTS <sup>1</sup> (Pins 13 to 24)								
TTL or 5 Volt CMOS								
Input Voltage								
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V	
Bit OFF Logic "0"	0		+0.8	0		+0.8	V	
Logic Current (each bit)								
Bit ON Logic "1"		+120	+300		+120	+300	μA	
Bit OFF Logic "0"		+35	+100		+35	+100	μA	
RESOLUTION			12			12	Bits	
OUTPUT								
Current								
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA	
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA	
Resistance (exclusive of span resistors)								
	6k	8k	10k	6k	8k	10k	Ω	
Offset								
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.	
Bipolar (Figure 4 R <sub>1</sub> and R <sub>2</sub> = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.	
Capacitance								
Compliance Voltage		25			25		pF	
T <sub>min</sub> to T <sub>max</sub>	-1.5		+10	-1.5		+10	V	
ACCURACY (error relative to full scale) -25°C								
		±1/4	±1/2		±1/8	±1/4	LSB	
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.	
T <sub>min</sub> to T <sub>max</sub>		±1/2	±3/4		±1/4	±1/2	LSB	
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.	
DIFFERENTIAL NONLINEARITY -25°C								
T <sub>min</sub> to T <sub>max</sub>		±1/2	±3/4		±1/4	±1/2	LSB	
MONOTONICITY GUARANTEED								
TEMPERATURE COEFFICIENTS								
Unipolar Zero		1	2		1	2	ppm/°C	
Bipolar Zero		5	10		5	10	ppm/°C	
Gain (Full Scale)		7	10		3	5	ppm/°C	
Differential Nonlinearity		2			2		ppm/°C	
SETTLING TIME TO 1/2LSB								
All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns	
FULL SCALE TRANSITION								
10% to 90% Delay plus Rise Time		15	30		15	30	ns	
90% to 10% Delay plus Fall Time		30	50		30	50	ns	
POWER REQUIREMENTS								
V <sub>EE</sub> = -11.4 to -16.5V dc		-12	-18		-12	-18	mA	
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>								
V <sub>EE</sub> = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S. /%	
PROGRAMMABLE OUTPUT								
RANGE (see Figures 3, 4, 5)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V	
EXTERNAL ADJUSTMENTS								
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.	
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.	
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.	
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.	
REFERENCE INPUT								
Input Impedance	15k	20k	25k	15k	20k	25k	Ω	
POWER DISSIPATION								
		180	300		180	300	mW	
MULTIPLYING MODE PERFORMANCE (All Models)								
Quadrants								
Reference Voltage								
Accuracy								
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)								
Output Slew Rate								
90%-90%								
Output Settling Time (all bits on and a 0-10V step change in reference voltage)								
Two (2)- Bipolar Operation at Digital Input Only +1V to +10V, Unipolar 10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage								
40kHz typ								
5mA/μs								
1mA/μs								
1.5μs to 0.01% F.S.								
CONTROL AMPLIFIER								
Full Power Bandwidth								
300kHz								
Small-Signal Closed-Loop Bandwidth								
1.8MHz								

Specifications subject to change without notice.

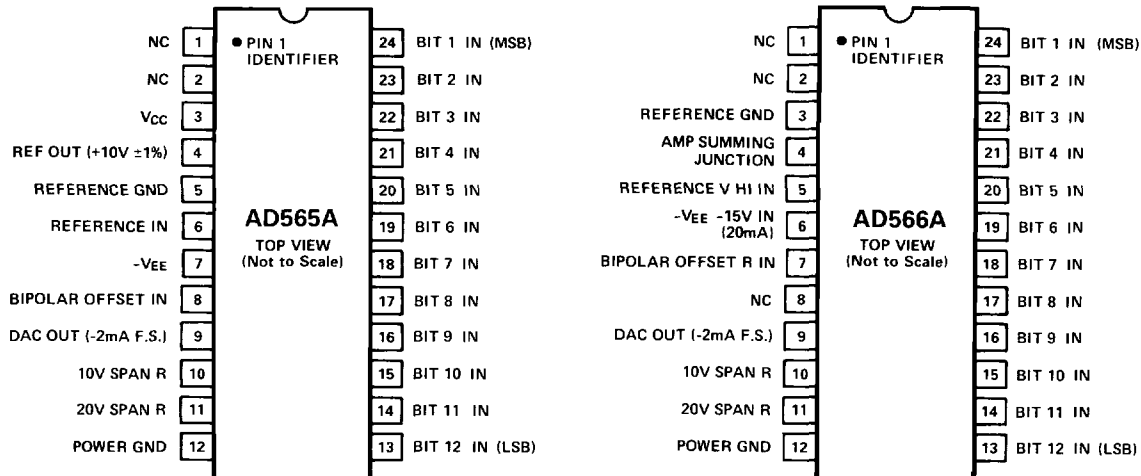
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

although only those shown in boldface are tested on all production units.

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to Power Ground	0V to +18V
$V_{EE}$ to Power Ground (AD565A)	0V to -18V
Voltage on DAC Output (Pin 9)	-3V to +12V
Digital Inputs (Pins 13 to 24) to	
Power Ground	-1.0V to +7.0V
Ref in to Reference Ground	$\pm 12V$
Bipolar Offset to Reference Ground	$\pm 12V$
10V Span R to Reference Ground	$\pm 12V$
20V Span R to Reference Ground	$\pm 24V$
Ref out (AD565A)	Indefinite Short to Power Ground
	Momentary Short to $V_{CC}$
Power Dissipation	1000mW

## PIN DESIGNATIONS



## AD565A ORDERING GUIDE

Model	Package Option *	Temp. Range	Linearity Error Max @ 25°C	Max Gain T.C. (ppm of F.S./°C)
AD565AJD/BIN	Ceramic (D-24)	0 to +70°C	$\pm 1/2$ LSB	50
AD565AKD/BIN	Ceramic (D-24)	0 to +70°C	$\pm 1/4$ LSB	20
AD565ASD/BIN	Ceramic (D-24)	-55°C to +125°C	$\pm 1/2$ LSB	30
AD565ATD/BIN	Ceramic (D-24)	-55°C to +125°C	$\pm 1/4$ LSB	15

\*See Section 14 for package outline information.

## AD566A ORDERING GUIDE

Model	Package Option *	Temp. Range	Linearity Error Max @ +25°C	Max Gain T.C. (ppm of F.S./°C)
AD566AJD/BIN	Ceramic (D-24)	0 to +70°C	$\pm 1/2$ LSB	10
AD566AKD/BIN	Ceramic (D-24)	0 to +70°C	$\pm 1/4$ LSB	3
AD566ASD/BIN	Ceramic (D-24)	-55°C to +125°C	$\pm 1/2$ LSB	10
AD566ATD/BIN	Ceramic (D-24)	-55°C to +125°C	$\pm 1/4$ LSB	3

\*See Section 14 for package outline information.

## GROUNDING RULES

The AD565A and AD566A bring out separate reference and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

## CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50 $\Omega$  fixed resistor is substituted for the 100 $\Omega$  trimmer, unipolar zero will typically be within  $\pm 1/2$ LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50 $\Omega$  resistor for the 100 $\Omega$  bipolar offset trimmer will give a bipolar zero error typically within  $\pm 2$ LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to  $\pm 1/2$ LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

## FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

### STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

### STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100 $\Omega$  gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120 $\Omega$  resistor in series with the gain resistor at pin 10 to the op amp output.

## FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

### STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100 $\Omega$  trimmer R1 to give -5.000 volts output.

### STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100 $\Omega$  gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

## FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or  $\pm 2.5$  volt and  $\pm 10$  volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or  $\pm 2.5$ ), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the  $\pm 10$  volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The  $\pm 10$  volt option is shown in Figure 3.

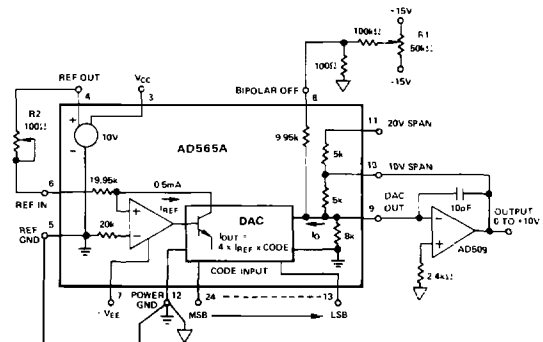


Figure 1. 0 to +10V Unipolar Voltage Output

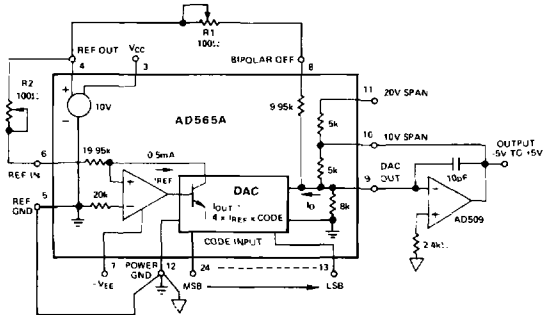


Figure 2.  $\pm 5$ V Bipolar Voltage Output

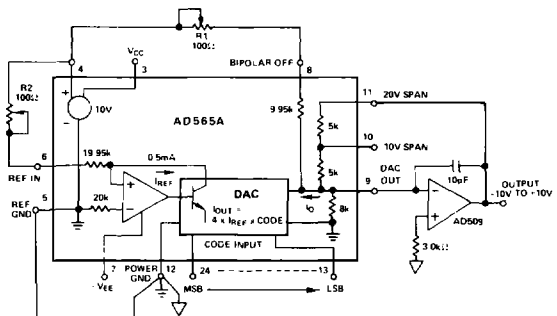


Figure 3.  $\pm 10$ V Voltage Output

## CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50 $\Omega$  fixed resistor is substituted for the 100 $\Omega$  trimmer, unipolar zero will typically be within  $\pm 1/2$ LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50 $\Omega$  resistor for the 100 $\Omega$  bipolar offset trimmer will give a bipolar zero error typically within  $\pm 2$ LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to  $\pm 1/2\text{LSB}$  of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

**FIGURE 4. UNIPOLAR CONFIGURATION**

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

### STEP 1... ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

## STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

**FIGURE 5. BIPOLAR CONFIGURATION**

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

## STEP 1... OFFSET ADJUST

Turn OFF all bits. Adjust  $100\Omega$  trimmer R1 to give -5.000 output volts.

## STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100 $\Omega$  gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

### FIGURE 6. OTHER VOLTAGE RANGES

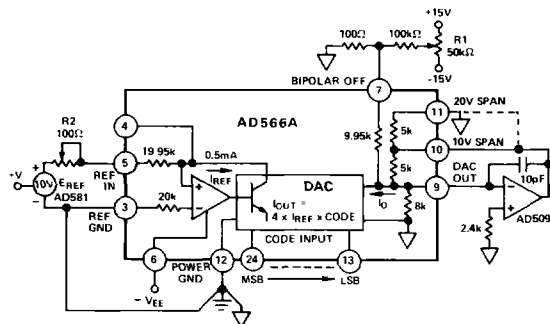
The AD566A can also be easily configured for a unipolar 0 to +5 volt range or  $\pm 2.5$  volt and  $\pm 10$  volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or  $\pm 2.5$ V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to  $V_{REF}$ .

for the bipolar range. For the  $\pm 10$  volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The  $\pm 10$  volt option is shown in Figure 6.

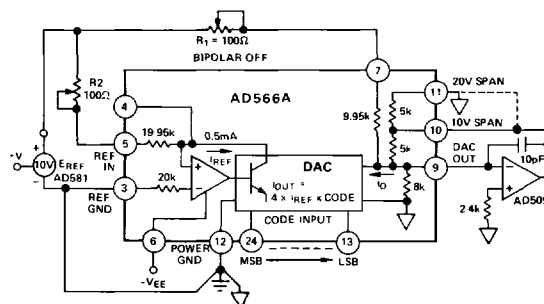
DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
0	000000000000	Zero	-Full Scale	Zero
1	111111111111	Mid-Scale -1LSB	Zero -1LSB	+FS -1LSB
0	000000000000	+1/2 FS	Zero	-FS
1	111111111111	+FS -1LSB	- Full Scale -1LSB	Zero -1LSB

\*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

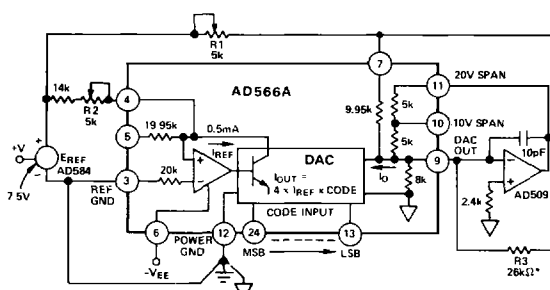
Table 1. Digital Input Codes



**Figure 4. 0 to +10V Unipolar Voltage Output**



**Figure 5.  $\pm 5V$  Bipolar Voltage Output**



\*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE

**Figure 6.  $\pm 10V$  Voltage Output**