

High-Speed 12-Bit Monolithic D/A Converters

AD565A*/AD566A*

FEATURES

Single Chip Construction

Very High-Speed Settling to 1/2LSB

AD565A: 250ns max AD566A: 350ns max Full-Scale Switching Time: 30ns

Guaranteed for Operation with ±12V Supplies: AD565A

with -12V Supply: AD566A

Linearity Guaranteed Over Temperature:

1/2LSB max (K, T Grades)

Monotonicity Guaranteed Over Temperature

Low Power: AD566A = 180mW max; AD565A = 225mW max

Use with On-Board High-Stability Reference (AD565A)

or with External Reference (AD566A)

Low Cost

PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters which incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

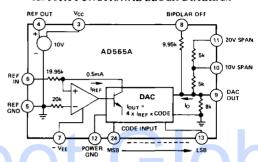
The AD565A and AD566A use 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10-90% full-scale transition time less than 35ns and settle to within ±1/2LSB in 250ns max (350ns for AD566A). Both are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD565A and AD566A the ideal choice for high-speed display drivers as well as fast analog-to-digital converters.

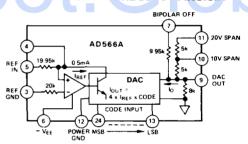
The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

^aCovered by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349; 4,020,486; 3,747,088.

AD565A FUNCTIONAL BLOCK DIAGRAM



AD566A FUNCTIONAL BLOCK DIAGRAM



AD565A and AD566A are available in four performance grades. The J and K are specified for use over the 0 to +70°C temperature range while the S and T grades are specified for the -55°C to +125°C range. All are packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package.

PRODUCT HIGHLIGHTS

- The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
- 2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
- 3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.

SPECIFICATIONS $T_A = \pm 25^{\circ}C$, $V_{CC} = \pm 15V$, $V_{EE} = -15V$, unless otherwise specified)

MODEL	MIN	AD565AJ TYP	MAX	MIN	AD565AK TYP	MAX	UNITS
DATA INPUTS ¹ (Pins 13 to 24) TTL or 5 Volt CMOS							
Input Voltage Bit ON Logic "1" Bit OFF Logic "0"	+2.0		+5.5 +0.8	+2.0		+5.5 +0.8	v v
Logic Current (each bit) Bit ON Logic "1" Bit OFF Logic "0"		+120 +35	+300 +100		+120 +35	+300 +100	μΑ μΑ
RESOLUTION		.,,,	12			12	Bits
OUTPUT				-			
Current Unipolar (all bits on)		-2 0	2.4		3.0		
Bipolar (all bits on or off)	-1.6 ±0.8	±1 0	-2.4 ±1.2	-1.6 ±0.8	-2.0 ±1.0	-2.4 ±1.2	mA mA
Resistance (exclusive of span resistors)	41 .	al.	101	Z1.	o.	1	
Offset	6k	8k	10k	6k	8k	10k	Ω
Unipolar	15	0 01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, $R_2 = 50\Omega$ fix Capacitance	(ed)	0 05 25	0.15		0.05 25	0.1	% of F.S. Range pF
Compliance Voltage							-
ACCURACY (error relative to	-1 5		+10	-1.5		+10	v
full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T _{min} to T _{max}		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
min to imax		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C	MONOT	±1/2 ONICITY GUARA	±3/4	MONOTO	±1/4 ONICITY GUAR	±1/2	LSB
T _{min} to T _{max} TEMPERATURE COEFFICIENTS	MONOI	ONICITI GUARA	MICED	MONOTO	DAICH GOAR	ANTEED	
With Internal Reference			_		_		.0.0
Unipolar Zero Bipolar Zero		1 5	2 10		1 5	2 10	ppm/°C ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB All Bits ON-to-OFF or OFF-to-ON		250	400	_	250	400	ns
FULL SCALE TRANSITION 10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE		-					
Operating Storage	0 -65		+70 +150	0 -65		+70 +150	°C °C
POWER REQUIREMENTS	-0.5		+130	-03	_	+130	
V _{CC} , +11.4 to +16.5V dc		3	5		3	5	mA
V _{EE} , -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVIT	Y ²						4
$V_{CC} = +11.4 \text{ to } +16.5 \text{ V dc}$ $V_{EE} = -11.4 \text{ to } -16.5 \text{ V dc}$		3 15	10 25		3 15	10 25	ppm of F.S./% ppm of F.S./%
PROGRAMMABLE OUTPUT							FF
RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		v
		-2.5 to +2.5			-2.5 to +2.5		v
		0 to +10 -5 to +5			0 to +10 -5 to +5		v v
		-10 to +10			-10 to +10		v
EXTERNAL ADJUSTMENTS			_				
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		+0.1	+0.25		+0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed		±0.1	±0.25		±0.1	±0.23	n of r.s. Natige
50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2) Bipolar Zero Adjustment Range	±0.25 ±0.15			±0.25 ±0.15			% of F.S. Range % of F.S. Range
REFERENCE INPUT						_	
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT Voltage	9.90	10.00	10.10	9.90	10.00	10.10	v
Current (available for external loads) ³	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	ww
NOTES		- LL)	273		<i>LL</i> J	777	38.0

NOTES

The digital inputs are guaranteed but not tested over the operating temperature range.

The power supply gain sensitivity is tested in reference to a VCC. VEE of ±15V dc.

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							ADJUJA/ADJUUA
MODEL	MIN	AD565AS TYP	MAX	MIN	AD565AT TYP	MAX	UNITS
DATA INPUTS ¹ (Pins 13 to 24) TTL or 5 Volt CMOS							
Input Voltage Bit ON Logic "1" Bit OFF Logic "0" Logic Current (each bit)	+2.0		+5.5 +0.8	+2.0		+5.5 +0.8	v v
Bit ON Logic "1" Bit OFF Logic "0"		+120 +35	+300 +100		+120 +35	+300 +100	μΑ μΑ
RESOLUTION			12			12	Bits
ОUТРUТ							
Current Unipolar (all bits on)	-1.6	-2 ()	-2.4	-1.6	-2 O	-2.4	mA
Bipolar (all bits on or off) Resistance (exclusive of span	±0.8	±1 0	±1.2	±0.8	±1 0	±1.2	mA
resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset			0.05			0.05	Prof.C.C. Booms
Unipolar Bipolar (Figure 3, R ₂ = 50Ω fix Capacitance	red)	0 01 0 05 25	0.05		0 01 0 05 25	0.05	% of F.S. Range % of F.S. Range pF
Comphance Voltage		23			2,		γ.
T _{min} to T _{max}	-15		+10	-1 5		+10	v
ACCURACY terror relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
Tuti scale) +23 C		(0.006)	(0.012)		(0.003)	(0.006)	% of F S. Range
T _{min} to T _{max}		±1'2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T _{min} to T _{max}	MONOTO	ONICITY GUAR	ANTEED	MONOTO	ONICITY GUAR	ANTEED	
TEMPERATURE COEFFICIENTS With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero Gain (Full Scale)		5 15	10 30		5 10	10 15	ppm/°C ppm/°C
Differential Nonlinearity		2	,0		2	13	ppm/°C
SETTLING TIME TO 1/2LSB All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION 10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating Storage	-55 -65		+125 +150	-55 -65		+125 +150	°C °C
POWER REQUIREMENTS	-03		*150	-07		- 150	
V _{CC} , +11.4 to +16.5V dc		3	5		3	5	mA
V _{EE} , -11.4 to -16.5V dc		-12	-18		-12	-18	mA.
POWER SUPPLY GAIN SENSITIVIT	TY ²				_		
$V_{CC} = +11.4 \text{ to } +16.5 \text{V dc}$ $V_{EE} = -11.4 \text{ to } -16.5 \text{V dc}$		3 15	10 25		3 15	10 25	ppm of F.S./% ppm of F.S./%
PROGRAMMABLE OUTPUT				-			
RANGES (see Figures 2, 3, 4)		0 to +5		<u> </u>	0 to +5 -2.5 to +2.5		v v
		-2 5 to +2.5 0 to +10			0 to +10		v
		-5 to +5		ĺ	-5 to +5		v
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS Gain Error with Fixed 50Ω							
Resistor for R2 (Figure 2)		±0.1	±0,25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed		10.05	40.15		40.05		W - 6 E 6 B
50Ω Resistor for R1 (Figure 3) Gain Adjustment Range (Figure 2)		±0.05	±0.15	±0.25	±0.05	±0.1	% of F.S. Range % of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT	15k	20k	25k	15k	20k	25k	Ω
Input Impedance REFERENCE OUTPUT	138	20K	23K	176	20K		
Voltage Current (available for external	9.90	10.00	10.10	9.90	10.00	10.10	v
loads)3	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW
C :: 6::	d am all amade						

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

		AD566AJ			AD566AK		
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS ¹ (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage Bit ON Logic "1"	. 2.0		+5.5	+2.0		+5.5	v
Bit OFF Logic "0"	+2.0 0		+0.8	0		+0.8	ľ
Logic Current (each bit)	v		10.0	ľ			,
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μΑ
RESOLUTION			12			12	Bits
OUTPUT							
Current			1.4				
Unipolar (all bits on) Bipolar (all bits on or off)	-1.6 ±0.8	-2.0 ±1.0	-2.4 ±1.2	-1.6 ±0.8	-2.0 ±1.0	-2.4 ±1.2	mA
Resistance (exclusive of span	-0.0	-10		_ ±0.8	21.0	-1.2	mA
resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to		0.01	0.05		0.01	0.05	% of F.S.R.
zero per Figure 3) Bipolar (Figure 4 R ₁ and		0.01	0.05		0.01	0.05	WOIP.S.K.
$R_2 = 50\Omega \text{ fixed}$		0.05	0.15		0.05	0.1	% of F S.R
Capacitance		25			25		pF
Compliance Voltage							
T _{min} to T _{max}	-1.5		+10	-1.5		÷10	V
ACCURACY (error relative to				l	14.0		
full scale) +25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0 003)	±1/4 (0.006)	LSB % of F.S R
T _{min} to T _{max}		±1/2	±3/4		±1/4	(0.006) ±1/2	LSB
·min · · max		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S R
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±174	±1/2	LSB
T _{min} to T _{max}	MONOTO	NICITY GUARA	ANTEED	MONOTON	NICITY GUARA	NTEED	
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10	l	5	10	ppm/°C
Gain (Full Scale) Differential Nonlinearity		7 2	10		3 2	5	ppm/°C ppm/°C
							ррии С
SETTLING TIME TO 1/2LSB All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
							113
FULL SCALE TRANSITION 10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V _{EE} , -11.4 to -16.5V dc		-12	-18		-12	-18	m A
POWER SUPPLY GAIN SENSITIVITY ²							
V _{EE} = -11.4 to -16.5 V dc		15	25		15	25	ppm of F S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		v
		-2 5 to +2.5			-2.5 to +2.5		v
		0 to +10 -5 to +5			0 to +10 -5 to +5		V V
		-10 to +10			-10 to +10		v
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω							
Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		10.05					% of F S.R
Gain Adjustment Range (Figure 3)	+0.35	±0.05	±0.15	±0.25	±0.05	±0.1	% of F S.R
Bipolar Zero Adjustment Range	±0.25 ±0.15			±0.15			% of F S.R
REFERENCE INPUT	7						
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Mo	rdels)						
Quadrants		Two (2)- Bin	olar Operati	on at Digital Inc	out Only		
Reference Voltage		+1V to +10V	. Unipolar		•		
Accuracy		10 Bits (±0.0	5% of Redu	ed F.S.) for 1V	de Reference Vo	ltage	
Reference Feedthrough (unipolar mode,							
all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/µs					
90%-10%		lmA/μs					
Output Settling Time (all bits on and a 0-10V							
step change in reference voltage)		1.5µs to 0.01	% F.S.				
CONTROL AMPLIFIER					_		
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

NOTES

The digital input levels are guaranteed but not tested over the temperature range.

The power supply gain sensitivity is tested in reference to a VEE of -15V dc.

Specifications subject to change without notice.

MODEL	MIN	AD566AS TYP	MAX	MIN	AD566AT TYP	MAX	UNITS
DATA INPUTS ¹ (Pins 13 to 24) TTL or 5 Volt CMOS							
Input Voltage Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	l v
Bit OFF Logic "0"	0		+0.8	0		+0.8	v
Logic Current (each bit) Bit ON Logic "1"		+120	+300		+120	+300	μΑ
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
DUTPUT							
Current	-1.6	-2 ()	-2.4	-1.6	-2 0	-2.4	l
Unipolar (all bits on) Bipolar (all bits on or off)	±0.8	=2 0 =1 0	±1.2	±0.8	±1 0	-2.4 ±1.2	mA mA
Resistance (exclusive of span							
resistors)	6k	8k	10k	6k	8k	10k	σ
Offset Unipolar (adjustable to							
zero per Figure 3)		0 01	0.05		0.01	0.05	% of FSR
Bipolar (Figure 4 R and							1
$R_2 = 50\Omega$ fixed) Capacitance		0.05 25	0.15		0.05 25	0.1	% of F.S.R pF
Compliance Voltage							r.
T _{man} to T _{max}	-1 5		+10	-1 5		+10	V
ACCURACY (error relative to	•		_				1
full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB % of F S.R.
T _{min} to T _{max}		(0 006) ±1/2	(0.012) ±3/4		(0 003) ±1 4	(0.006) ±1/2	LSB
-mui -o -max		(0.012)	(0.018)		(0,006)	(0.012)	° of F.S.R.
DIFFERENTIAL NONLINEARITY							
-25°C		±1,2	±3/4		±1/4	±1/2	LSB
T _{min} to T _{max}	MONO	TONICITY GUAR	ANTEED	MONO	TONICITY GUA	RANTEED	
TEMPERATURE COEFFICIENTS			2			_	0
Unipolar Zero Bipolar Zero		1 5	10	ı	l 5	2 10	ppm-°C ppm-°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
ETTLING TIME TO 1/2LSB All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
TULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time 90% to 10% Delay plus Fall Time		15 30	30 50	ļ	15 30	30 50	ns ns
POWER REQUIREMENTS	_		20	-			113
V _{EE} 11.4 to -16.5V de		-12	-18		-12	-18	mA
OWER SUPPLY GAIN SENSITIVITY ²							
$V_{EE} = -11.4$ to -16.5V dc		15	25	ł	15	25	ppm of F S 1%
ROGRAMMABLE OUTPUT					0 - 2		
RANGE (see Figures 3, 4, 5)		0 to +5 -2 5 to +2 5			0 to +5 -2.5 to +2.5		V V
		0 to +10			0 to +10		v
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
XTERNAL ADJUSTMENTS Gain Error with Fixed 50Ω		40.1	±0.25	ļ	±0.1	±0.25	% of F.S.R.
Resistor R2 (Figure 3) Bipolar Zero Error with Fixed		±0.1	±0.23	1	10.1	±0.23	VOLF.S.R.
50Ω Resistor for R1 (Figure 4)		±0 05	±0.15		±0.05	±0.1	% of F.S R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			70 15			% of F.S.R.
EFERENCE INPUT Input Impedance	15k	20k	25k	15k	20k	25k	Ω
OWER DISSIPATION		180	300		180	300	mW
IULTIPLYING MODE PERFORMANCE (All M	odels)						·
Quadrants	/			on at Digital Inj	out Only		
Reference Voltage		+1V to +10V	, Unipolar			t.	
Accuracy Reference Feedthrough (unipolar mode,		10 Bits (±0,0	or Kedu	ted P.S.) for 1V	de Reference V	onage	

Reference Feedthrough (unipolar mode,

all bits OFF, and 1 to +10V [p-p], sinewave

frequency for 1/2LSB [p-p] feedthrough)
Output Slew Rate 10%-90%
90%-10% 40kHz typ 5mA/µs 1mA/µs

Output Settling Time (all bits on and a 0-10V step change in reference voltage)

1.5µs to 0.01% F.S. CONTROL AMPLIFIER

Full Power Bandwidth Small-Signal Closed-Loop Bandwidth Specifications subject to change without notice. 300kHz 1.8MHz

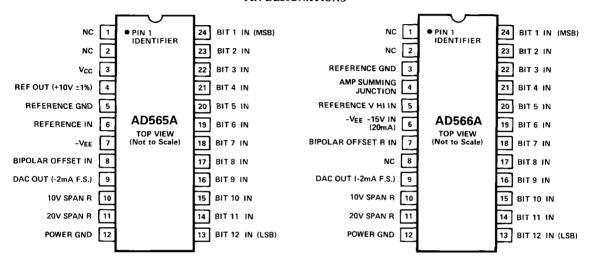
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed,

although only those shown in boldface are tested on all production

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground
V _{EE} to Power Ground (AD565A) 0V to -18V
Voltage on DAC Output (Pin 9) $\dots -3V$ to $+12V$
Digital Inputs (Pins 13 to 24) to
Power Ground1.0V to +7.0V
Ref in to Reference Ground ± 12V
Bipolar Offset to Reference Ground ± 12V
10V Span R to Reference Ground ± 12V
20V Span R to Reference Ground ±24V
Ref out (AD565A) Indefinite Short to Power Ground
Momentary Short to V _{CC}
Power Dissipation 1000mW

PIN DESIGNATIONS



AD565A ORDERING GUIDE

Model	Package Option*	Temp. Range	Linearity Error Max @ 25°C	Max Gain T.C. (ppm of F.S./°C)
AD565AJD/BIN	Ceramic (D-24)	0 to +70°C	± 1/2LSB	50
AD565AKD/BIN	Ceramic (D-24)	$0 \text{ to } + 70^{\circ}\text{C}$	$\pm 1/4LSB$	20
AD565ASD/BIN	Ceramic (D-24)	- 55°C to + 125°C	$\pm 1/2LSB$	30
AD565ATD/BIN	Ceramic (D-24)	55°C to 1125°C	$\pm 1/4LSB$	15

^{*}See Section 14 for package outline information.

AD566A ORDERING GUIDE

Model	Package Option*	Temp. Range		Max Gain T.C. (ppm of F.S./°C)
AD566AJD/BIN	Ceramic (D-24)	0 to +70°C	$\pm 1/2LSB$	10
AD566AKD/BIN	Ceramic (D-24)	0 to + 70°C	$\pm 1/4LSB$	3
AD566ASD/BIN	Ceramic (D-24)	-55°C to +125°C	$\pm 1/2LSB$	10
AD566ATD/BIN	Ceramic (D-24)	-55°C to $+125$ °C	$\pm 1/4LSB$	3

^{*}See Section 14 for package outline information.

Applying the AD565A/AD566A

GROUNDING RULES

The AD565A and AD566A bring out separate reference and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, unipolar zero will typically be within $\pm 1/2$ LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer will give a bipolar zero error typically within ± 2 LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to $\pm 1/2$ LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120 Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or ± 2.5 volt and ± 10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ± 2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ± 10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ± 10 volt option is shown in Figure 3.

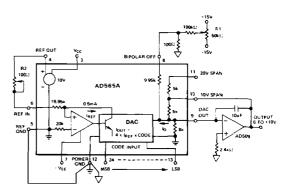


Figure 1. 0 to +10V Unipolar Voltage Output

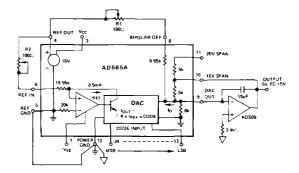


Figure 2. ±5V Bipolar Voltage Output

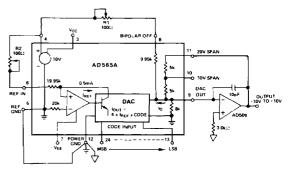


Figure 3. ±10V Voltage Output

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within $\pm 1/2LSB$ (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within $\pm 2LSB$ (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer. R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 6. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 to +5 volt range or ± 2.5 volt and ± 10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or ± 2.5 V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF}

for the bipolar range, For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 6.

DIGITAL	INPUI	ANALOG GUIPCI					
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*			
000000	000000	Zero	-Full Scale	Zero			
011111	111111	Mid Scale -1LSB	Zero -1LSB	+FS -1LSB			
100000	000000	+1/2 FS	Zero	-FS			
111111	111111	+FS-1LSB	+ Full Scale -1LSB	Zero -1LSB			

Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

DIGITAL INDUST

Table I. Digital Input Codes

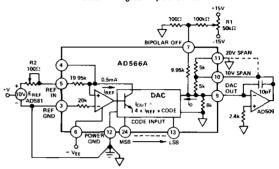


Figure 4. 0 to +10V Unipolar Voltage Output

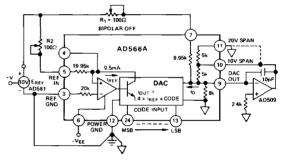
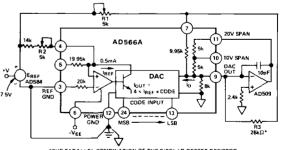


Figure 5. ±5V Bipolar Voltage Output



THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSE CURRENT THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE

Figure 6. ±10V Voltage Output