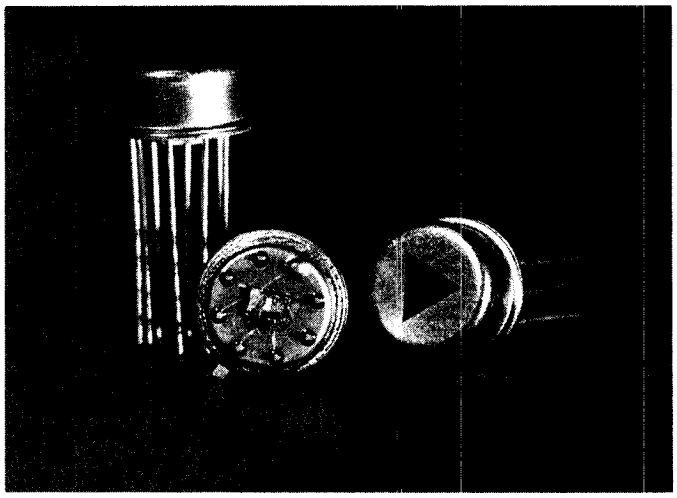
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES
Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{os}: 25μV max (AD517L), 150μV max (AD517J)
Low V_{os} Drift: 0.5μV/°C (AD517L)
Internal Compensation
Internal Compensation
Low Cost



PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 25μV and offset voltage drifts less than 0.5μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the full military temperature range, −55°C to +125°C. The AD517S is also available with full processing to the requirements of MIL-STD-883, Level B.

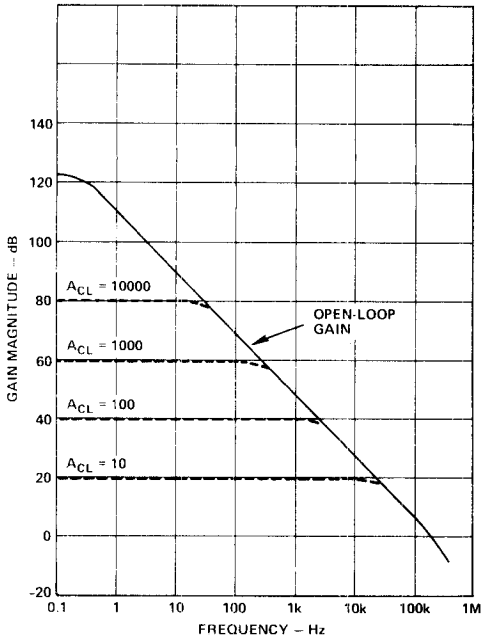
PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models. Testing is performed using a controlled-temperature drift bath following a 5 minute warm-up period.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Every AD517 is baked for 48 hours at +150°C, temperature cycled from −65°C to +200°C, and subjected to a high G shock test to assure reliability and long-term stability.

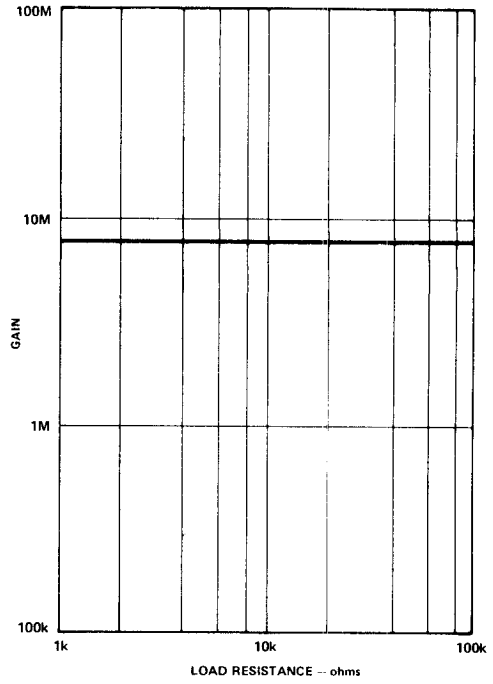
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD517J	AD517K	AD517L	AD517S[1]
OPEN LOOP GAIN				
V_O = ±10V, $R_L \geqslant 2k\Omega$	10^6 min	*	*	*
T_{min} to T_{max}	500,000 min	*	*	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geqslant 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	250kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leqslant 10k\Omega$	150μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
(T_{min} to T_{max})	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	1nA max	0.75nA max	0.25nA max	**
T_{min} to T_{max}	1.5nA max	1.25nA max	0.4nA max	2nA max
INPUT BIAS CURRENT				
Initial	5nA max	2nA max	1nA max	**
T_{min} to T_{max}	8nA max	3.5nA max	1.5nA max	10nA max
vs. Temp, T_{min} to T_{max}	±20pA/°C	±10pA/°C	±4pA/°C	**
INPUT IMPEDANCE				
Differential	15MΩ‖1.5pF	20MΩ‖1.5pF	**	**
Common Mode	$2.0x10^{11}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	2μV p-p	*	*	*
f = 10Hz	35nV/√Hz	*	*	*
f = 100Hz	25nV/√Hz	*	*	*
f = 1kHz	20nV/√Hz	*	*	*
Current, f = 10Hz	0.05pA/√Hz	*	*	*
f = 100Hz	0.03pA/√Hz	*	*	*
f = 1kHz	0.03pA/√Hz	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max Safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB min	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*

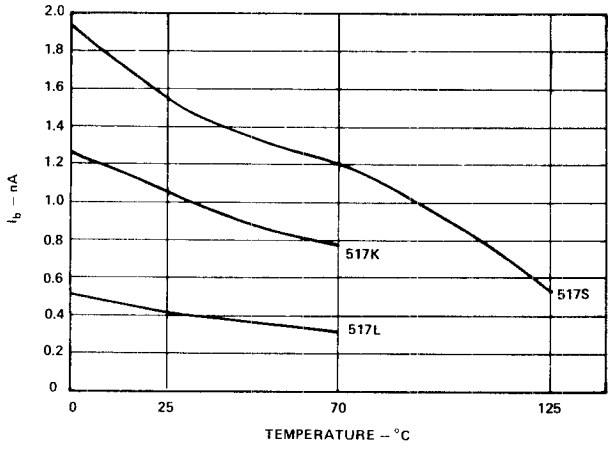
NOTES
*Specifications same as AD517J
**Specifications same as AD517K
Specifications subject to change without notice.
[1] The AD517S is available fully processed and screened to the requirements of MIL-STD-883, Level B. Consult factory for pricing.



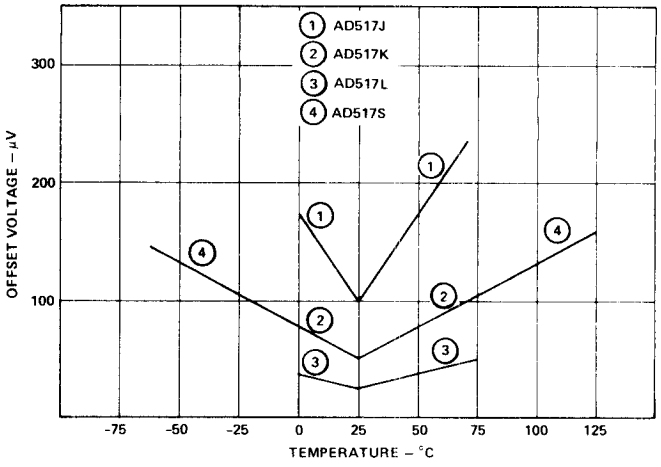
Small-Signal Gain vs. Frequency



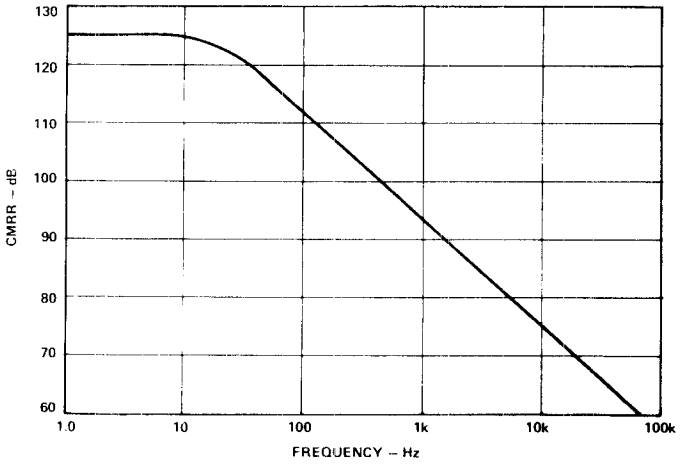
Open-Loop Gain vs. Load Resistance



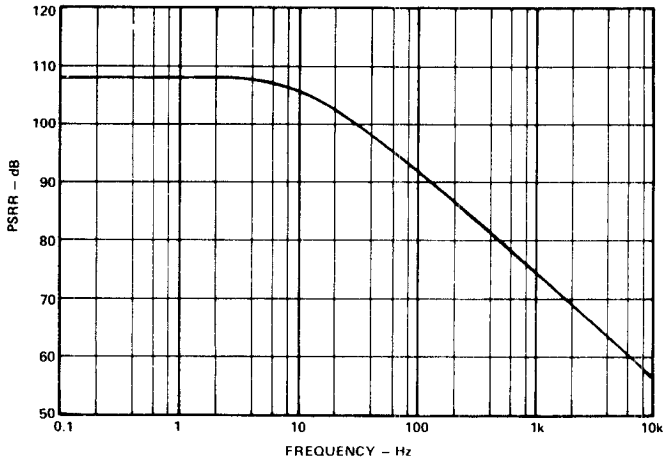
Input Bias Current vs. Temperature



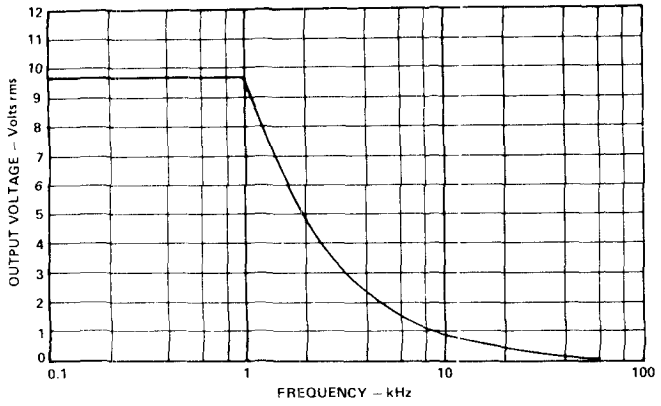
Max Untrimmed Offset Voltage vs. Temperature



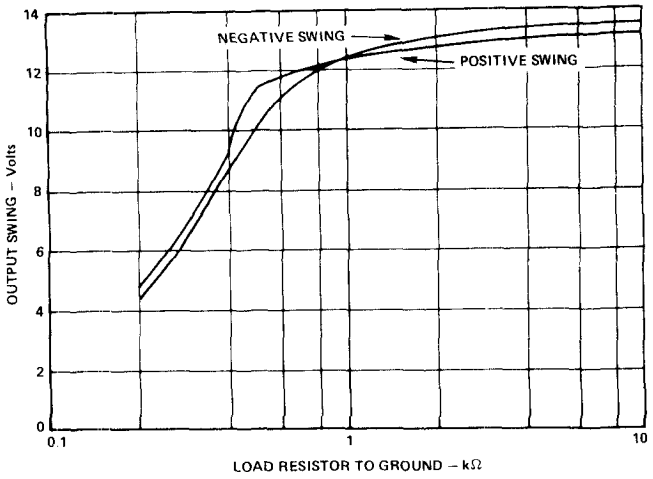
CMRR vs. Frequency



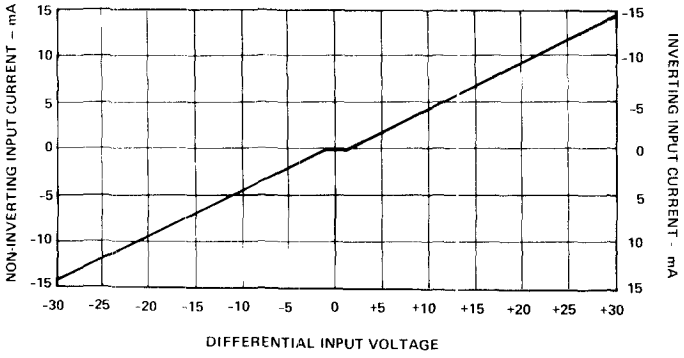
PSRR vs. Frequency



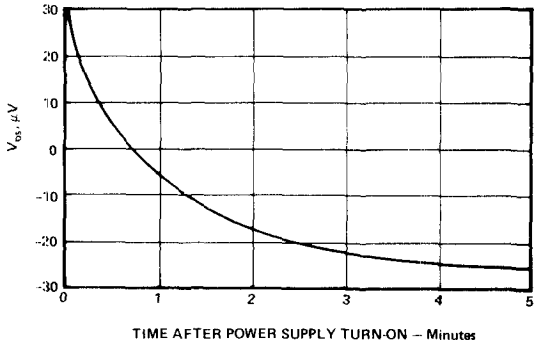
Maximum Undistorted Output vs. Frequency (Distortion ⩽ 1%)



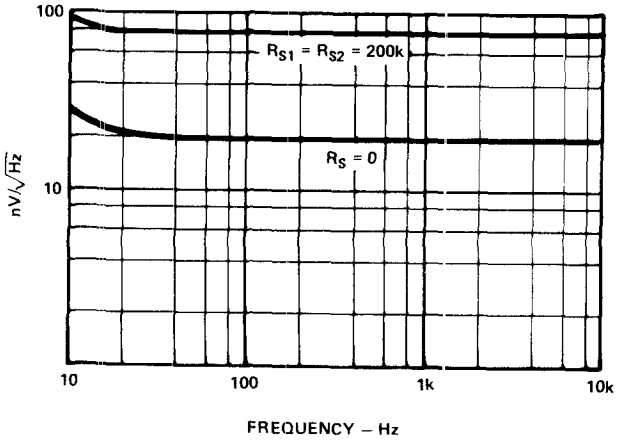
Output Voltage vs. Load Resistance



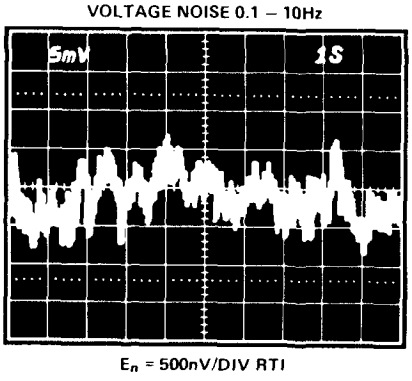
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

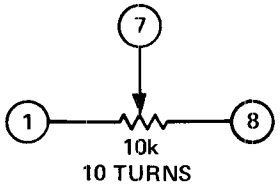
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

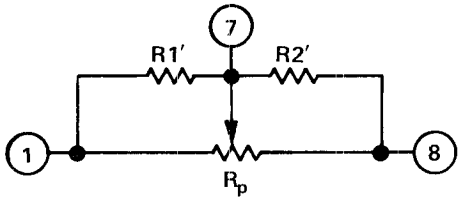
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

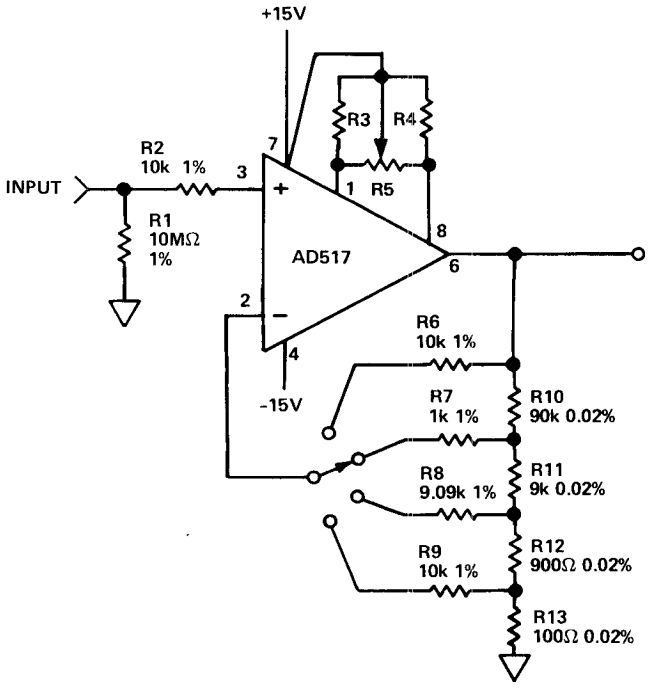


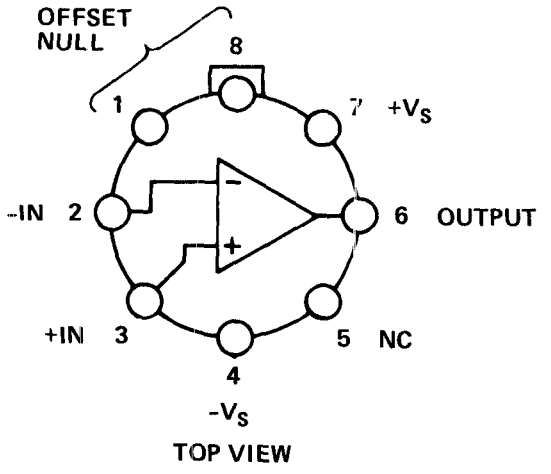
Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

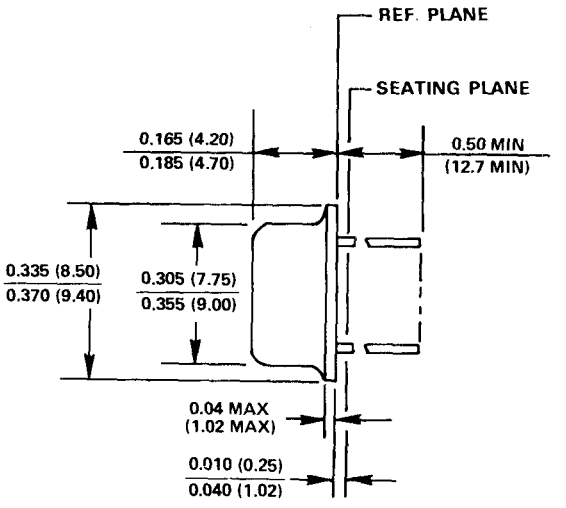
The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

PIN CONFIGURATION



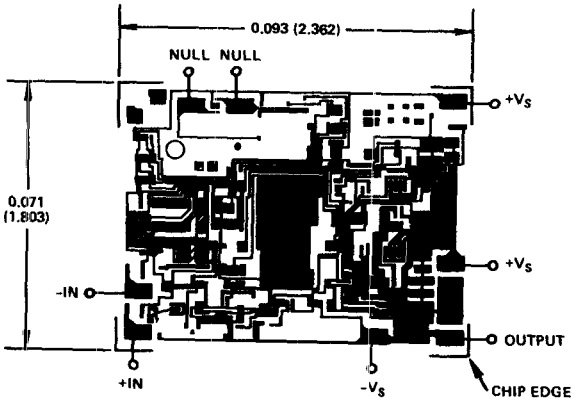
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

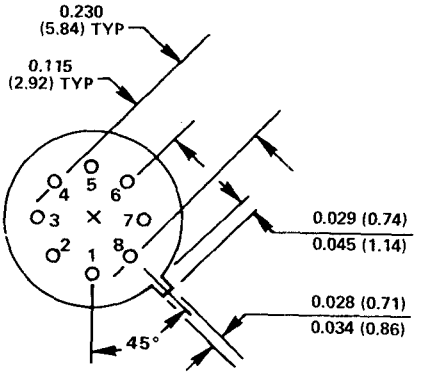


CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD517 IS AVAILABLE IN LASER-TRIMMED CHIP FORM. CONSULT CHIP CATALOG FOR DETAILS.



TO-99