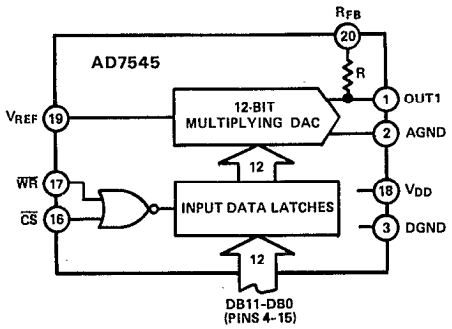
CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES
- **12-Bit Resolution**
- **Low Gain T.C.: 2ppm/°C typ**
- **Fast TTL Compatible Data Latches**
- **Single +5V to +15V Supply**
- **Small 20-Pin 0.3" DIP and 20-Terminal Surface Mount Packages**
- **Latch Free (Schottky Protection Diode Not Required)**
- **Low Cost**
- **Ideal for Battery Operated Equipment**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

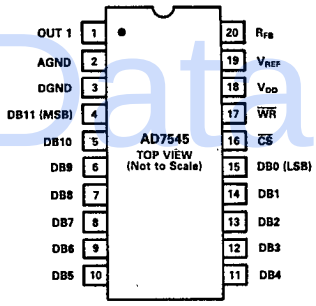
The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

PIN CONFIGURATIONS

DIP



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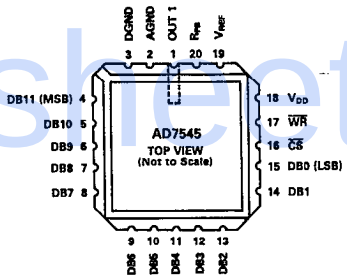

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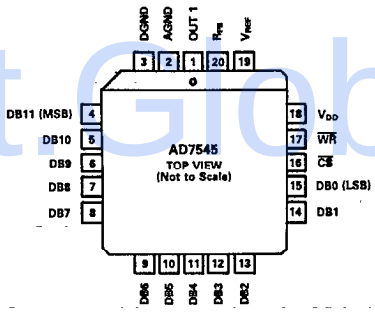


AD7545—SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits T_A = +25°C	T_{min}, T_{max}[1]	V_{DD} = +15V Limits T_A = +25°C	T_{min}, T_{max}[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{min} to T_{max}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5 and 6
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0-DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	µs max	To 1/2LSB. OUT 1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[3] (from Digital Input Change to 90% of final Analog Output)	All	300	–	250	–	ns max	OUT1 LOAD = 100Ω C_{EXT} = 13pF[4]
Digital to Analog Glitch Impulse	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5] At I_{OUT1}	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sinewave
REFERENCE INPUT							
Input Resistance (Pin 19 to GND)	All	7	7	7	7	kΩ min	Input Resistance TC = -300ppm/°C typ
		25	25	25	25	kΩ max	Typical Input Resistance = 11kΩ
ANALOG OUTPUTS							
Output Capacitance[3]							
C_{OUT1}	All	70	70	70	70	pF max	DB0-DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	200	200	200	200	pF max	DB0-DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6] I_{IN}	All	±1	±10	±1	±10	µA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3]							
DB0-DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS[7]							
Chip Select to Write Setup Time t_{CS}	All	280	380	180	200	ns min	See Timing Diagram
		200	270	120	150	ns typ	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time t_{DS}	All	140	210	90	120	ns min	
		100	150	60	80	ns typ	
Data Hold Time t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	µA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	µA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows: J, K, L, GL versions: 0 to +70°C
A, B, C, GC versions: -25°C to +85°C
S, T, U, GU versions: -55°C to +125°C

[2] This includes the effect of 5ppm max gain TC.

[3] Guaranteed but not tested.

[4] DB0-DB11 = 0V to V_{DD} or V_{DD} to 0V.

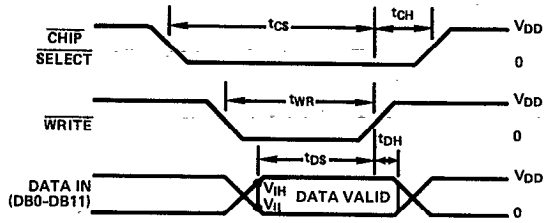
[5] Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

[6] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[7] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION	
WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0–DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0–DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $V_{IH} + V_{IL}/2$.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V, +17V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND	±25V
V_{PIN1} to DGND	−0.3V, V_{DD} +0.3V
AGND to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commercial (J, K, L, GL) Grades	0 to +70°C
Industrial (A, B, C, GC) Grades	−25°C to +85°C
Extended (S, T, U, GU) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: The amount by which the D/A converter transfer function differs from the ideal transfer function after the zero and full scale points have been adjusted. This is an end point linearity measurement.

DIFFERENTIAL NONLINEARITY: The difference between the measured change and the ideal change between any two adjacent codes. If a device has a differential nonlinearity of less than 1LSB then it will be monotonic, i.e., the output will always increase for an increase in digital code applied to the D/A converter.

PROPAGATION DELAY: This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reached 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVsecs and is measured with V_{REF} = AGND and an ADLH0032CG as the output op amp, C1 (phase compensation) = 33pF.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Maximum Gain Error T_A=+25°C V_{DD}=+5V	Package Option[3]
AD7545JN	0°C to +70°C	±2 LSB	±20 LSB	N-20
AD7545AQ	−25°C to +85°C	±2 LSB	±20 LSB	Q-20
AD7545SQ	−55°C to +125°C	±2 LSB	±20 LSB	Q-20
AD7545KN	0°C to +70°C	±1 LSB	±10 LSB	N-20
AD7545BQ	−25°C to +85°C	±1 LSB	±10 LSB	Q-20
AD7545TQ	−55°C to +125°C	±1 LSB	±10 LSB	Q-20
AD7545LN	0°C to +70°C	±1/2 LSB	±5 LSB	N-20
AD7545CQ	−25°C to +85°C	±1/2 LSB	±5 LSB	Q-20
AD7545UQ	−55°C to +125°C	±1/2 LSB	±5 LSB	Q-20
AD7545GLN	0°C to +70°C	±1/2 LSB	±1 LSB	N-20
AD7545GCQ	−25°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7545GUQ	−55°C to +125°C	±1/2 LSB	±1 LSB	Q-20
AD7545JP	0°C to +70°C	±2 LSB	±20 LSB	P-20A
AD7545SE	−55°C to +125°C	±2 LSB	±20 LSB	E-20A
AD7545KP	0°C to +70°C	±1 LSB	±10 LSB	P-20A
AD7545TE	−55°C to +125°C	±1 LSB	±10 LSB	E-20A
AD7545LP	0°C to +70°C	±1/2 LSB	±5 LSB	P-20A
AD7545UE	−55°C to +125°C	±1/2 LSB	±5 LSB	E-20A
AD7545GLP	0°C to +70°C	±1/2 LSB	±1 LSB	P-20A
AD7545GUE	−55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-20) in lieu of cerdip packages (Q-20).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military datasheets. For U.S. Standard Military Drawing (SMD) see DESC drawing 5962-87702.
[3]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

CIRCUIT INFORMATION – D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545 and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

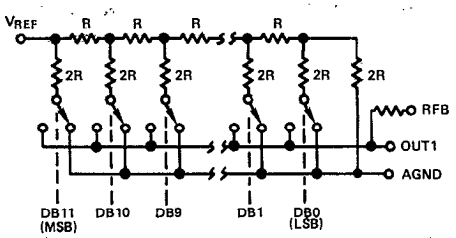


Figure 1. Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

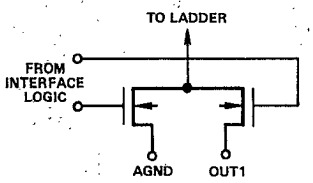


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION–DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

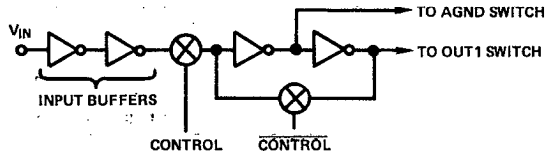


Figure 3. Digital Input Structure

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. The "G" versions (AD7545GLN, AD7545GCQ, AD7545GUD) have a guaranteed maximum gain error of ±1LSB at +25°C (V_{DD} = +5V) and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 1 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 4.

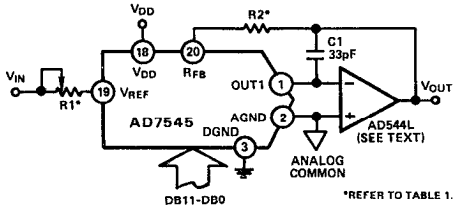


Figure 4. Unipolar Binary Operation

TRIM RESISTOR	J/A/S	K/B/T	L/C/U	GL/GC/GU
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades for V_{DD} = +5V

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive –OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 and R4 causes full scale error.

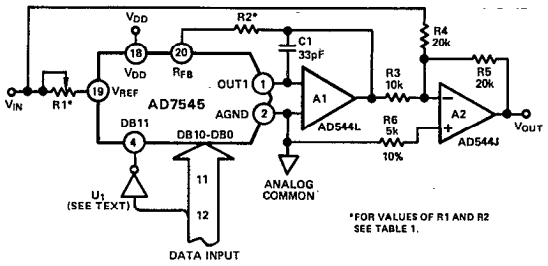


Figure 5. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table III. 2's Complement Code Table for Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

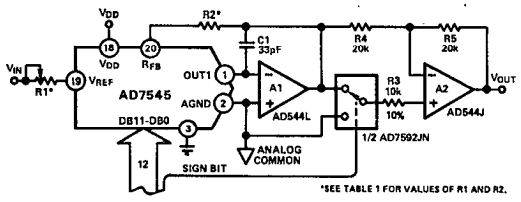


Figure 6. 12-Bit Plus Sign Magnitude D/A Converter

Sign Bit	Binary Numbers in DAC Register			Analog Output
0	1111	1111	1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high cur-

rents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545 (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT 1 and AGND may be biased at any voltage between DGND and V_{DD}. OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The AD7545 is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545 connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit.

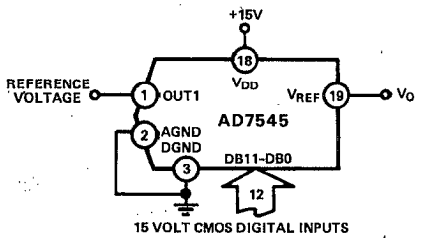


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions.

To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15V or the differential voltage between OUT1 and AGND is increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

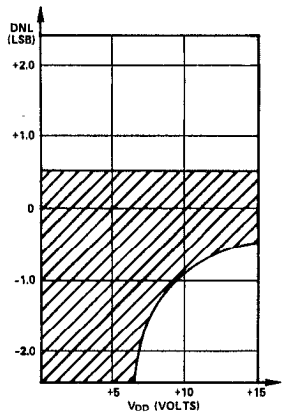


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

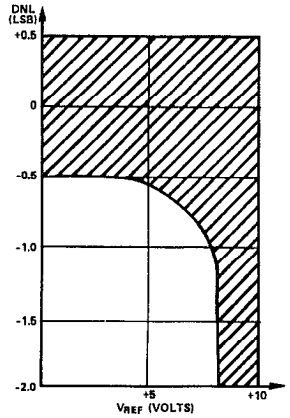


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between V_{DD} and DGND. Figure 10 shows the 2's Complement Bipolar circuit of Figure 5 modified to give a range from +2V to +8V about a "pseudo-analog ground" of 5V. This voltage range would allow operation from a single V_{DD} of +10V to +15V. The AD584 pin-programmable reference fixes AGND at +5V. V_{IN} is set at +2V by means of the series resistors R1 and R2. There is no need to buffer the V_{REF} input to the AD7545 with an amplifier because the input impedance of the D/A converter is constant. Note, however, that since the temperature coefficient of the D/A reference input resistance is typically -300ppm/°C, applications which experience wide temperature variations may require a buffer amplifier to generate

the +2.0V at the AD7545 V_{REF} pin. Other output voltage ranges can be obtained by changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. V_{DD} must be kept at least 5V above OUT1 to ensure that linearity is preserved.

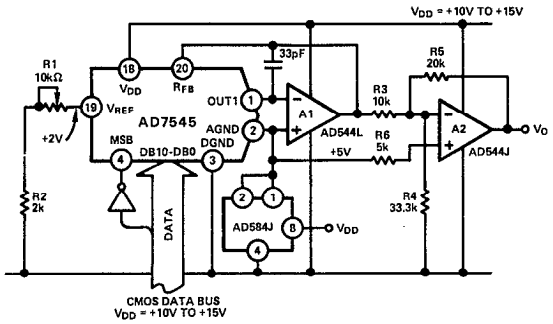


Figure 10. Single Supply "Bipolar" 2's Complement D/A Converter

MICROPROCESSOR INTERFACING OF THE AD7545

The AD7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

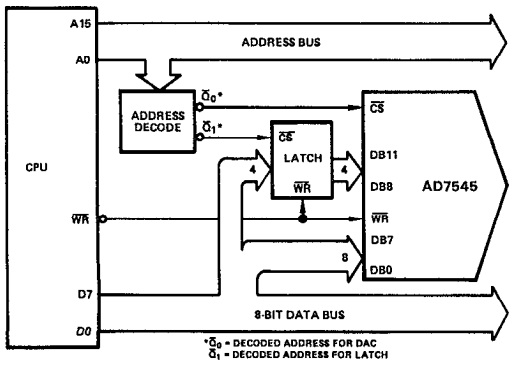


Figure 11. 8-Bit Processor to AD7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each AD7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

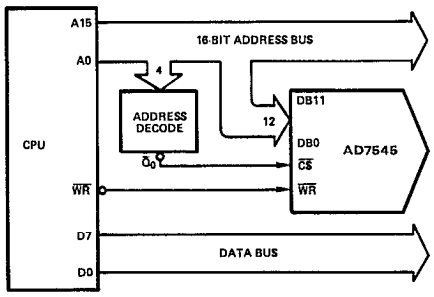


Figure 12. Connecting the AD7545 to 8-Bit Processors via the Address Bus

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Application Guide to CMOS Multiplying D/A converters available from Analog Devices, Publication Number G479.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACS – Application Note, Publication Number E630–10–6/81 available from Analog Devices.