

# NE5517, NE5517A, AU5517

## Dual Operational Transconductance Amplifier

The AU5517 and NE5517 contain two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The AU5517/NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The AU5517/NE5517 is suited for a wide variety of industrial and consumer applications.

Constant impedance of the buffers on the chip allow general use of the AU5517/NE5517. These buffers are made of Darlington transistors and a biasing network that virtually eliminate the change of offset voltage due to a burst in the bias current  $I_{ABC}$ , hence eliminating the audible noise that could otherwise be heard in high quality audio applications.

### Features

- Constant Impedance Buffers
- $\Delta V_{BE}$  of Buffer is Constant with Amplifier  $I_{BIAS}$  Change
- Excellent Matching Between Amplifiers
- Linearizing Diodes
- High Output Signal-to-Noise Ratio
- Pb-Free Packages are Available\*

### Applications

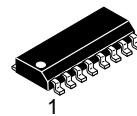
- Multiplexers
- Timers
- Electronic Music Synthesizers
- Dolby® HX Systems
- Current-Controlled Amplifiers, Filters
- Current-Controlled Oscillators, Impedances



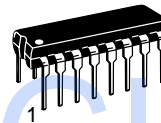
**ON Semiconductor®**

<http://onsemi.com>

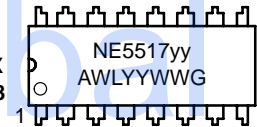
### MARKING DIAGRAMS



**SOIC-16  
D SUFFIX  
CASE 751B**

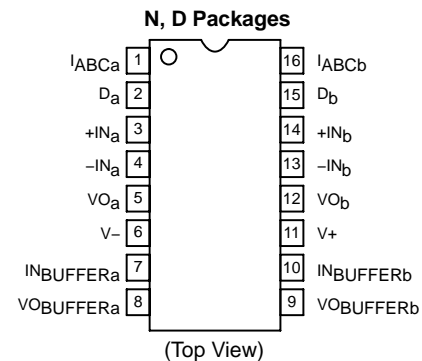


**PDIP-16  
N SUFFIX  
CASE 648**



xx = AU or NE  
yy = AN or N  
A = Assembly Location  
WL = Wafer Lot  
YY, Y = Year  
WW = Work Week  
G = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NE5517, NE5517A, AU5517

## PIN DESCRIPTION

Pin No.	Symbol	Description
1	$I_{ABCa}$	Amplifier Bias Input A
2	$D_a$	Diode Bias A
3	$+IN_a$	Non-inverted Input A
4	$-IN_a$	Inverted Input A
5	$VO_a$	Output A
6	$V-$	Negative Supply
7	$IN_{BUFFERa}$	Buffer Input A
8	$VO_{BUFFERa}$	Buffer Output A
9	$VO_{BUFFERb}$	Buffer Output B
10	$IN_{BUFFERb}$	Buffer Input B
11	$V+$	Positive Supply
12	$VO_b$	Output B
13	$-IN_b$	Inverted Input B
14	$+IN_b$	Non-inverted Input B
15	$D_b$	Diode Bias B
16	$I_{ABCb}$	Amplifier Bias Input B

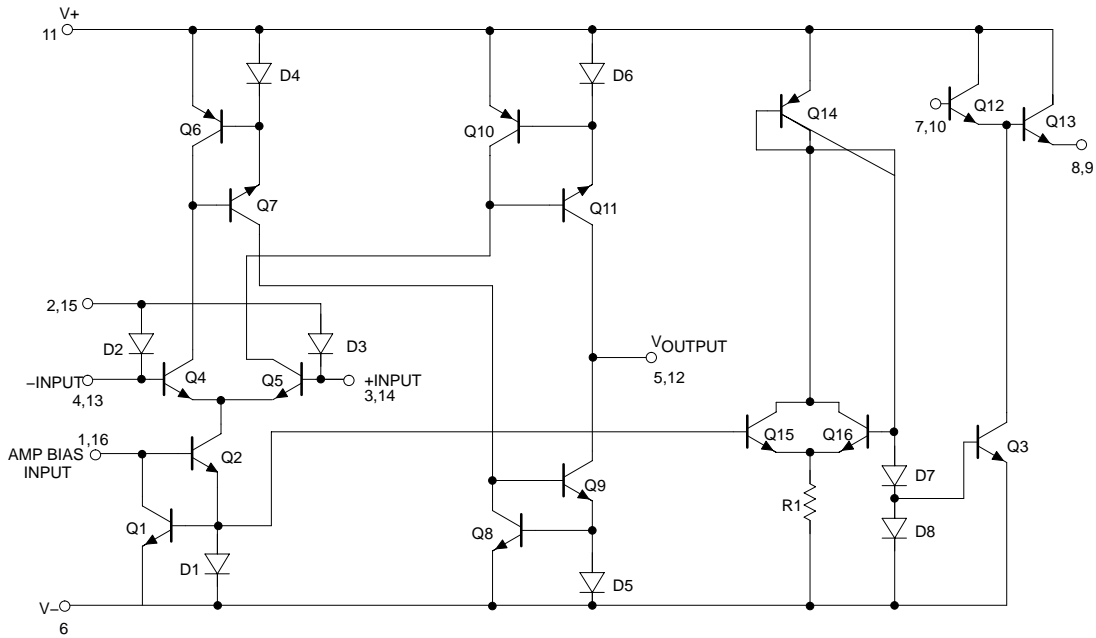


Figure 1. Circuit Schematic

# NE5517, NE5517A, AU5517



NOTE: V+ of output buffers and amplifiers are internally connected.

Figure 2. Connection Diagram

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	$V_S$	44 $V_{DC}$ or $\pm 22$	V
Power Dissipation, $T_{amb} = 25^\circ\text{C}$ (Still Air) (Note 2) NE5517N, NE5517AN NE5517D, AU5517D	$P_D$	1500 1125	mW
Thermal Resistance, Junction-to-Ambient D Package N Package	$R_{\theta JA}$	140 94	$^\circ\text{C}/\text{W}$
Differential Input Voltage	$V_{IN}$	$\pm 5.0$	V
Diode Bias Current	$I_D$	2.0	mA
Amplifier Bias Current	$I_{ABC}$	2.0	mA
Output Short-Circuit Duration	$I_{SC}$	Indefinite	
Buffer Output Current (Note 3)	$I_{OUT}$	20	mA
Operating Temperature Range NE5517N, NE5517AN AU5517T	$T_{amb}$	$0^\circ\text{C}$ to $+70^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	150	$^\circ\text{C}$
DC Input Voltage	$V_{DC}$	$+V_S$ to $-V_S$	
Storage Temperature Range	$T_{stg}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$	$^\circ\text{C}$
Lead Soldering Temperature (10 sec max)	$T_{slid}$	230	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- For selections to a supply voltage above  $\pm 22$  V, contact factory.
- The following derating factors should be applied above  $25^\circ\text{C}$   
N package at  $10.6\text{ mW}/^\circ\text{C}$   
D package at  $7.1\text{ mW}/^\circ\text{C}$ .
- Buffer output current should be limited so as to not exceed package dissipation.

# NE5517, NE5517A, AU5517

## ELECTRICAL CHARACTERISTICS (Note 4)

Characteristic	Test Conditions	Symbol	AU5517/NE5517			NE5517A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	Overtemperature Range $I_{ABC} = 5.0 \mu A$	$V_{OS}$		0.4 0.3	5.0 5.0		0.4 0.3	2.0 5.0 2.0	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of Input Offset Voltage			7.0			7.0		$\mu V/^{\circ}C$
$V_{OS}$ Including Diodes	Diode Bias Current ( $I_D$ ) = 500 $\mu A$			0.5	5		0.5	2.0	mV
Input Offset Change	$5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	$V_{OS}$		0.1			0.1	3.0	mV
Input Offset Current		$I_{OS}$		0.1	0.6		0.1	0.6	$\mu A$
$\Delta I_{OS}/\Delta T$	Avg. TC of Input Offset Current			0.001			0.001		$\mu A/^{\circ}C$
Input Bias Current	Overtemperature Range	$I_{BIAS}$		0.4 1.0	5.0 8.0		0.4 1.0	5.0 7.0	$\mu A$
$\Delta I_B/\Delta T$	Avg. TC of Input Current			0.01			0.01		$\mu A/^{\circ}C$
Forward Transconductance	Overtemperature Range	$g_M$	6700 5400	9600	13000	7700 4000	9600	12000	$\mu mho$
$g_M$ Tracking				0.3			0.3		dB
Peak Output Current	$R_L = 0, I_{ABC} = 5.0 \mu A$ $R_L = 0, I_{ABC} = 500 \mu A$ $R_L = 0, \text{Overtemperature Range}$	$I_{OUT}$	350 300	5.0 500	650	3.0 350 300	5.0 500	7.0 650	$\mu A$
Peak Output Voltage Positive Negative	$R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$ $R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	$V_{OUT}$	+12 -12	+14.2 -14.4		+12 -12	+14.2 -14.4		V
Supply Current	$I_{ABC} = 500 \mu A$ , both channels	$I_{CC}$		2.6	4.0		2.6	4.0	mA
$V_{OS}$ Sensitivity Positive Negative	$\Delta V_{OS}/\Delta V_+$ $\Delta V_{OS}/\Delta V_-$			20 20	150 150		20 20	150 150	$\mu V/V$
Common-mode Rejection Ratio		CMRR	80	110		80	110		dB
Common-mode Range			$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz			100			100		dB
Differential Input Current	$I_{ABC} = 0$ , Input = $\pm 4.0$ V	$I_{IN}$		0.02	100		0.02	10	nA
Leakage Current	$I_{ABC} = 0$ (Refer to Test Circuit)			0.2	100		0.2	5.0	nA
Input Resistance		$R_{IN}$	10	26		10	26		k $\Omega$
Open-loop Bandwidth		$B_W$		2.0			2.0		MHz
Slew Rate	Unity Gain Compensated	SR		50			50		V/ $\mu s$
Buffer Input Current	5	$I_{N\_BUFFER}$		0.4	5.0		0.4	5.0	$\mu A$
Peak Buffer Output Voltage	5	$V_{O\_BUFFER}$	10			10			V
$\Delta V_{BE}$ of Buffer	Refer to Buffer $V_{BE}$ Test Circuit (Note 6)			0.5	5.0		0.5	5.0	mV

4. These specifications apply for  $V_S = \pm 15$  V,  $T_{amb} = 25^{\circ}C$ , amplifier bias current ( $I_{ABC}$ ) = 500  $\mu A$ , Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

5. These specifications apply for  $V_S = \pm 15$  V,  $I_{ABC} = 500 \mu A$ ,  $R_{OUT} = 5.0$  k $\Omega$  connected from the buffer output to  $-V_S$  and the input of the buffer is connected to the transconductance amplifier output.

6.  $V_S = \pm 15$ ,  $R_{OUT} = 5.0$  k $\Omega$  connected from Buffer output to  $-V_S$  and  $5.0 \mu A \leq I_{ABC} \leq 500 \mu A$ .

TYPICAL PERFORMANCE CHARACTERISTICS

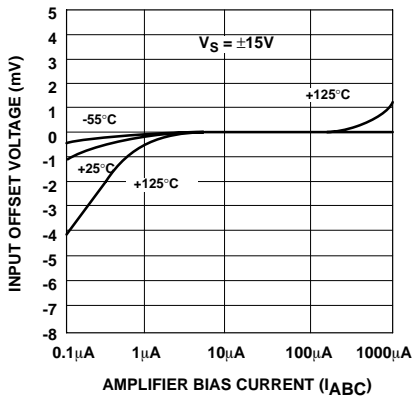


Figure 3. Input Offset Voltage

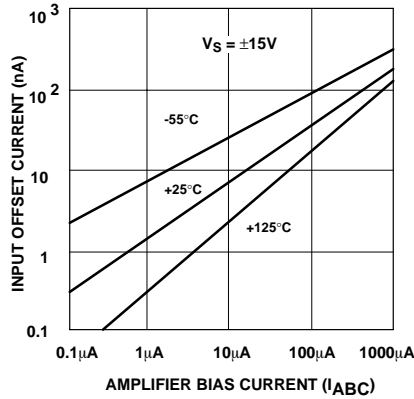


Figure 4. Input Bias Current

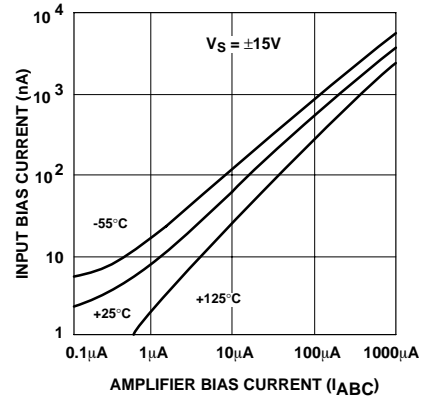


Figure 5. Input Bias Current

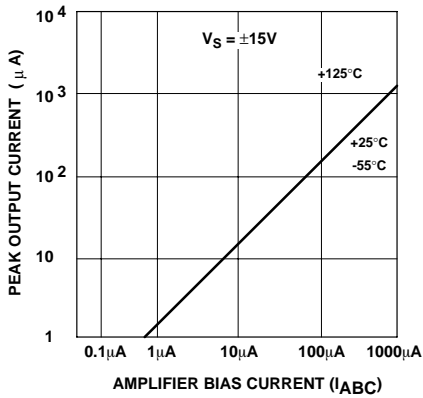


Figure 6. Peak Output Current

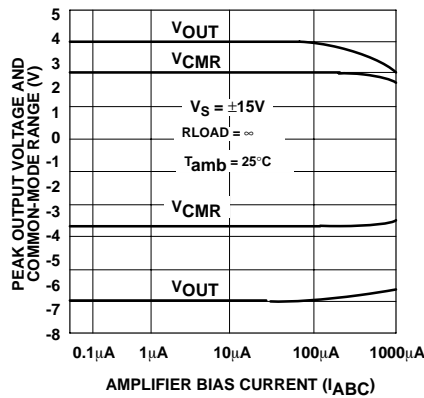


Figure 7. Peak Output Voltage and Common-Mode Range

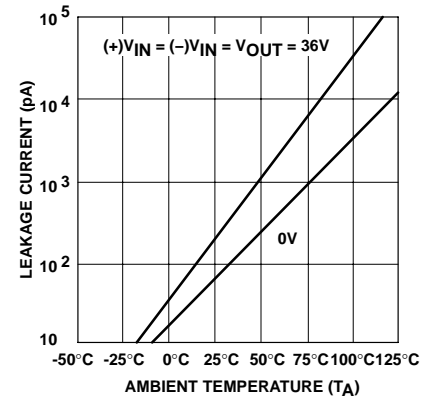


Figure 8. Leakage Current



Figure 9. Input Leakage



Figure 10. Transconductance

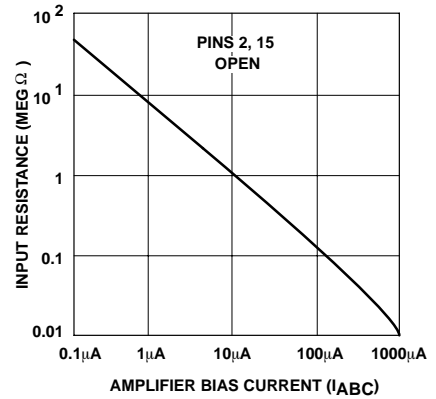


Figure 11. Input Resistance

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

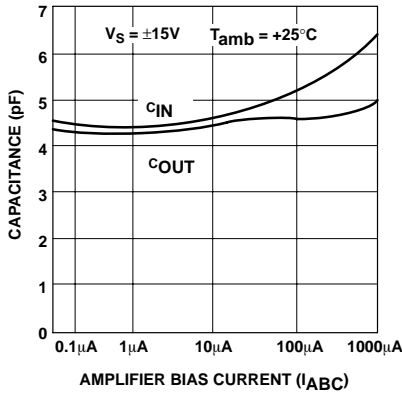


Figure 13. Input and Output Capacitance



Figure 14. Distortion vs. Differential Input Voltage



Figure 15. Voltage vs. Amplifier Bias Current



Figure 16. Noise vs. Frequency



Figure 17. Leakage Current Test Circuit



Figure 18. Differential Input Current Test Circuit

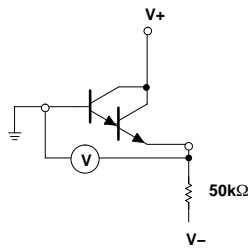


Figure 19. Buffer  $V_{BE}$  Test Circuit

APPLICATIONS



Figure 20. Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the AU5517/NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

Transconductance Amplifier

The transistor pair, Q<sub>4</sub> and Q<sub>5</sub>, forms a transconductance stage. The ratio of their collector currents (I<sub>4</sub> and I<sub>5</sub>, respectively) is defined by the differential input voltage, V<sub>IN</sub>, which is shown in Equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (\text{eq. 1})$$

Where V<sub>IN</sub> is the difference of the two input voltages

KT ≅ 26 mV at room temperature (300°k).

Transistors Q<sub>1</sub>, Q<sub>2</sub> and diode D<sub>1</sub> form a current mirror which focuses the sum of current I<sub>4</sub> and I<sub>5</sub> to be equal to amplifier bias current I<sub>B</sub>:

$$I_4 + I_5 = I_B \quad (\text{eq. 2})$$

If V<sub>IN</sub> is small, the ratio of I<sub>5</sub> and I<sub>4</sub> will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (\text{eq. 3})$$

$$\text{and } I_4 \approx I_5 \approx I_B$$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (\text{eq. 4})$$

$$I_5 - I_4 = V_{IN} \frac{(I_B^q)}{2KT}$$

The remaining transistors (Q<sub>6</sub> to Q<sub>11</sub>) and diodes (D<sub>4</sub> to D<sub>6</sub>) form three current mirrors that produce an output current equal to I<sub>5</sub> minus I<sub>4</sub>. Thus:

$$V_{IN} \left( \frac{I_B^q}{2KT} \right) = I_O \quad (\text{eq. 5})$$

The term  $\frac{(I_B^q)}{2KT}$  is then the transconductance of the amplifier and is proportional to I<sub>B</sub>.



Figure 21. Circuit Diagram of NE5517

**Linearizing Diodes**

For  $V_{IN}$  greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume  $D_2$  and  $D_3$  are biased with current sources and the input signal current is  $I_S$ . Since  $I_4 + I_5 = I_B$  and  $I_5 - I_4 = I_0$ , that is:  $I_4 = (I_B - I_0)$ ,  $I_5 = (I_B + I_0)$

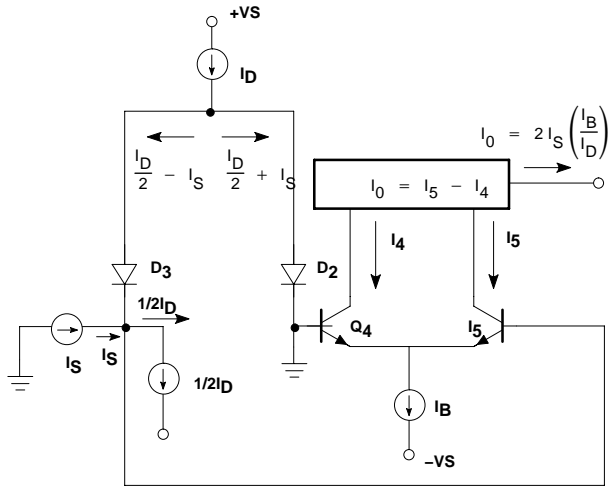


Figure 22. Linearizing Diode

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_0)}{1/2(I_B - I_0)} \quad (\text{eq. 6})$$

$$I_0 = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed  $I_D$ .

**Impedance Buffer**

The upper limit of transconductance is defined by the maximum value of  $I_B$  (2.0 mA). The lowest value of  $I_B$  for which the amplifier will function therefore determines the overall dynamic range. At low values of  $I_B$ , a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source ( $Q_{14}$ ,  $Q_{15}$ ,  $Q_{16}$ ,  $D_7$ ,  $D_8$ , and  $R_1$ ) suits the need.

**APPLICATIONS**

**Voltage-Controlled Amplifier**

In Figure 23, the voltage divider  $R_2$ ,  $R_3$  divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M$$

$$V_{OUT} = I_{OUT} \cdot R_L$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$(3) g_M = 19.2 I_{ABC}$$

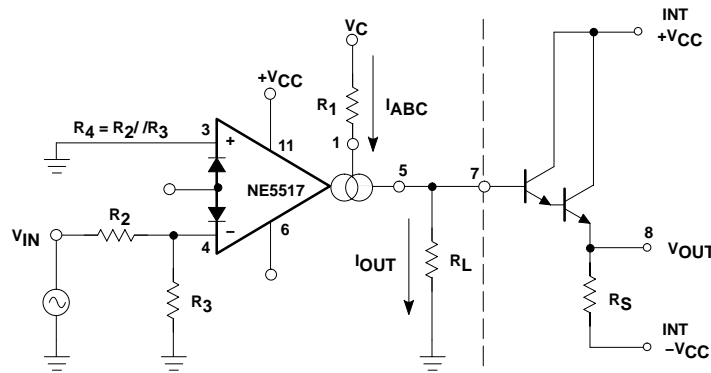
( $g_M$  in  $\mu\text{mhos}$  for  $I_{ABC}$  in mA)

Since  $g_M$  is directly proportional to  $I_{ABC}$ , the amplification is controlled by the voltage  $V_C$  in a simple way.

When  $V_C$  is taken relative to  $-V_{CC}$  the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the AU5517/NE5517.



TYPICAL VALUES:  $R_1 = 47k\Omega$   
 $R_2 = 10k\Omega$   
 $R_3 = 200\Omega$   
 $R_4 = 200\Omega$   
 $R_L = 100k\Omega$   
 $R_S = 47k\Omega$

Figure 23.



# NE5517, NE5517A, AU5517

## Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer,  $R_P$ , the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510  $\Omega$  resistors.

## Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to  $I_{ABC}$ , the amplification of a signal can be controlled easily. The output current is the product from transconductance  $\times$  input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.



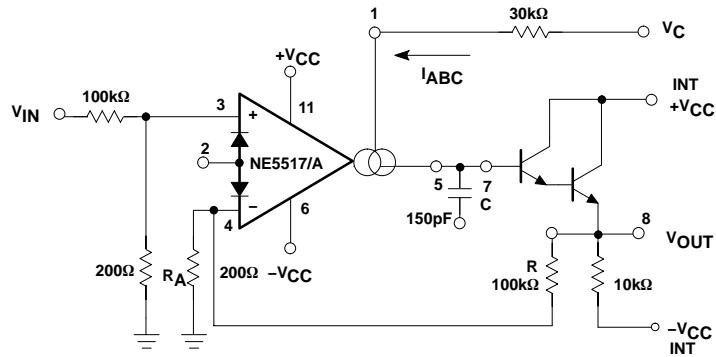
Figure 24. Gain-Controlled Stereo Amplifier



Figure 25. Amplitude Modulator



# NE5517, NE5517A, AU5517



NOTE:

$$f_O = \frac{R_A g_M}{g(R + R_A) 2\pi C}$$

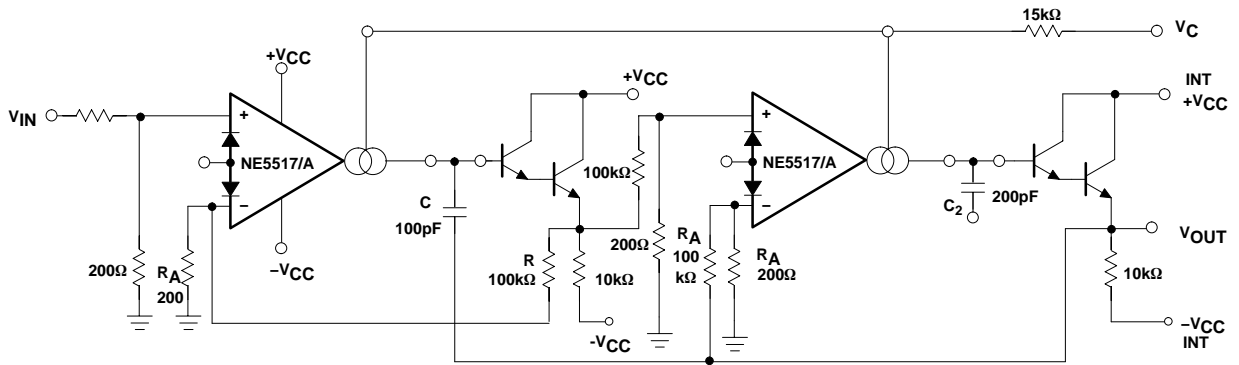
Figure 28. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{g(R + R_A) 2\pi C}$$

Figure 29. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{(R + R_A) 2\pi C}$$

Figure 30. Butterworth Filter - 2nd Order

# NE5517, NE5517A, AU5517



Figure 31. State Variable Filter

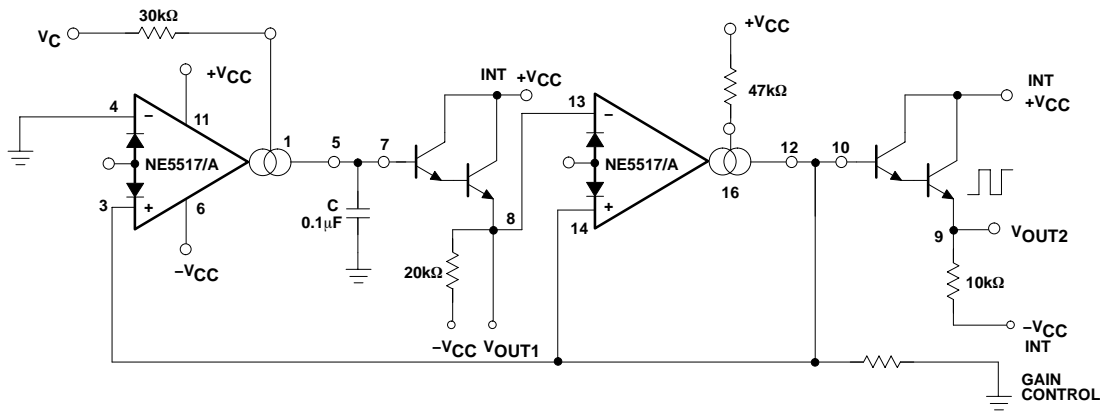


Figure 32. Triangle-Square Wave Generator (VCO)

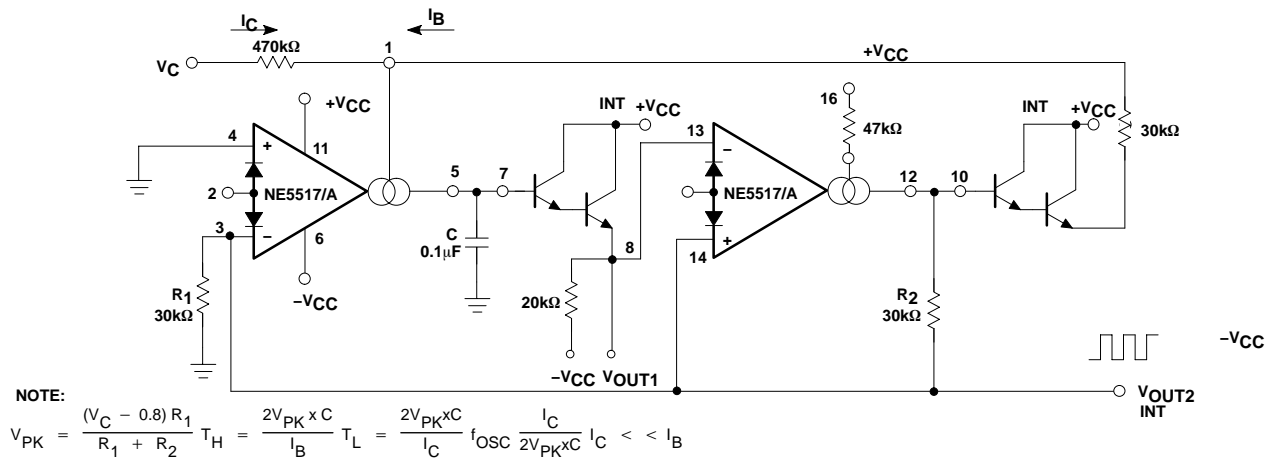


Figure 33. Sawtooth Pulse VCO

## NE5517, NE5517A, AU5517

### ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
AU5517DR2	-40 to +125 °C	SOIC-16	2500 Tape & Reel
AU5517DR2G		SOIC-16 (Pb-Free)	
NE5517D	0 to +70 °C	SOIC-16	48 Units/Rail
NE5517DG		SOIC-16 (Pb-Free)	
NE5517DR2		SOIC-16	2500 Tape & Reel
NE5517DR2G		SOIC-16 (Pb-Free)	
NE5517N		PDIP-16	25 Units/Rail
NE5517NG		PDIP-16 (Pb-Free)	
NE5517AN		PDIP-16	
NE5517ANG		PDIP-16 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NE5517, NE5517A, AU5517

## PACKAGE DIMENSIONS

### SOIC-16 CASE 751B-05 ISSUE J



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

### PDIP-16 CASE 648-08 ISSUE T



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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