# Single-Channel, 1024-Position, Digital Rheostat with SPI Interface and 50-TP Memory

# AD5174

## FEATURES

- Single-channel, 1024-position resolution
- 10 kΩ nominal resistance
- 50-times programmable (50-TP) wiper memory
- Rheostat mode temperature coefficient: 35 ppm/°C
- 2.7 V to 5.5 V single-supply operation
- ±2.5 V to ±2.75 V dual-supply operation for ac or bipolar operations
- SPI-compatible interface
- Wiper setting and memory readback
- Power on refreshed from memory
- Resistor tolerance stored in memory
- Thin LFCSP 10-lead, 3 mm × 3 mm× 0.8 mm package
- Compact MSOP, 10-lead, 3 mm × 4.9 mm × 1.1 mm package

## APPLICATIONS

- Mechanical rheostat replacements
- Op-amp: variable gain control
- Instrumentation: gain, offset adjustment
- Programmable voltage-to-current conversions
- Programmable filters, delays, time constants
- Programmable power supply
- Sensor calibration

## FUNCTIONAL BLOCK DIAGRAM

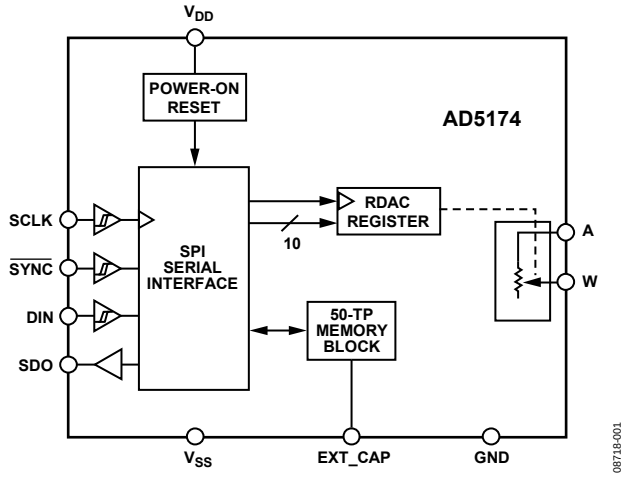


*Figure 1.*



## GENERAL DESCRIPTION

The AD5174 is a single-channel, 1024-position digital rheostat that combines industry leading variable resistor performance with nonvolatile memory (NVM) in a compact package.

This device supports both dual-supply operation at ±2.5 V to ±2.75 V and single-supply operation at 2.7 V to 5.5 V and offers 50-times programmable (50-TP) memory.

The AD5174 device wiper settings are controllable through the SPI digital interface. Unlimited adjustments are allowed before programming the resistance value into the 50-TP memory. The AD5174 does not require any external voltage supply to facilitate fuse blow and there are 50 opportunities for permanent programming. During 50-TP activation, a permanent blow fuse command freezes the resistance position (analogous to placing epoxy on a mechanical rheostat).

The AD5174 is available in a 3 mm × 3mm 10-lead LFCSP package and in a 10-lead MSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

**Rev. 0**


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## REVISION HISTORY

**3/10—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V; $V_{DD}$ = 2.5 V to 2.75 V, $V_{SS}$ = −2.5 V to −2.75 V; −40°C < $T_A$ < 125°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS—RHEOSTAT MODE | | | | | | |
| Resolution | | | 10 | | | Bits |
| Resistor Integral Nonlinearity[2, 3] | R-INL | $\|V_{DD} - V_{SS}\|$ = 3.6 V to 5.5 V | −1 | | +1 | LSB |
| | | $\|V_{DD} - V_{SS}\|$ = 3.3 V to 3.6 V | −1 | | +1.5 | LSB |
| | | $\|V_{DD} - V_{SS}\|$ = 2.7 V to 3.3 V | −2.5 | | +2.5 | LSB |
| Resistor Differential Nonlinearity[2] | R-DNL | | −1 | | +1 | LSB |
| Nominal Resistor Tolerance | | | | ±15 | | % |
| Resistance Temperature Coefficient[4, 5] | | Code = full scale | | 35 | | ppm/°C |
| Wiper Resistance | | Code = zero scale | | 35 | 70 | Ω |
| RESISTOR TERMINALS | | | | | | |
| Terminal Voltage Range[4, 6] | $V_{TERM}$ | | $V_{SS}$ | | $V_{DD}$ | V |
| Capacitance A[4] | | f = 1 MHz, measured to GND, code = half scale | | 90 | | pF |
| Capacitance W[4] | | f = 1 MHz, measured to GND, code = half scale | | 40 | | pF |
| Common-Mode Leakage Current[4] | | $V_A = V_W$ | | | 50 | nA |
| DIGITAL INPUTS | | | | | | |
| Input Logic[4] | | | | | | |
| High | $V_{INH}$ | | 2.0 | | | V |
| Low | $V_{INL}$ | | | | 0.8 | V |
| Input Current | $I_{IN}$ | | | ±1 | | µA |
| Input Capacitance[4] | $C_{IN}$ | | | 5 | | pF |
| DIGITAL OUTPUT | | | | | | |
| Output Voltage[4] | | | | | | |
| High | $V_{OH}$ | $R_{PULL\_UP}$ = 2.2 kΩ to $V_{DD}$ | $V_{DD}$ − 0.1 | | | V |
| Low | $V_{OL}$ | $R_{PULL\_UP}$ = 2.2 kΩ to $V_{DD}$ | | | | |
| | | $V_{DD}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V | | | 0.4 | V |
| | | $V_{DD}$ = 2.5 V to 2.75 V, $V_{SS}$ = −2.5 V to −2.75 V | | | 0.6 | V |
| Tristate Leakage Current | | | −1 | | +1 | µA |
| Output Capacitance[4] | | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Single-Supply Power Range | | $V_{SS}$ = 0 V | 2.7 | | 5.5 | V |
| Dual-Supply Power Range | | | ±2.5 | | ±2.75 | V |
| Supply Current | | | | | | |
| Positive | $I_{DD}$ | | | | 1 | µA |
| Negative | $I_{SS}$ | | −1 | | | µA |
| 50-TP Store Current[4, 7] | | | | | | |
| Positive | $I_{DD\_OTP\_STORE}$ | | | 4 | | mA |
| Negative | $I_{SS\_OTP\_STORE}$ | | | −4 | | mA |
| 50-TP Read Current[4, 8] | | | | | | |
| Positive | $I_{DD\_OTP\_READ}$ | | | | 500 | µA |
| Negative | $I_{SS\_OTP\_READ}$ | | −500 | | | µA |
| Power Dissipation[9] | $P_{DISS}$ | $V_{IH} = V_{DD}$ or $V_{IL}$ = GND | | | 5.5 | µW |
| Power Supply Rejection Ratio[4] | PSRR | $\Delta V_{DD}/\Delta V_{SS}$ = ±5 V ± 10% | −50 | −55 | | dB |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DYNAMIC CHARACTERISTICS[4, 10] | | | | | | |
| Bandwidth | | −3 dB, $R_{AW}$ = 5 kΩ, Terminal W, see Figure 24 | | 700 | | kHz |
| Total Harmonic Distortion | | $V_A$ = 1 V rms, f = 1 kHz, $R_{AW}$ = 5 kΩ | | −90 | | dB |
| Resistor Noise Density | | $R_{WB}$ = 5 kΩ, $T_A$ = 25°C, f = 10 kHz | | 13 | | nV/√Hz |

[1] Typical specifications represent average readings at 25°C, $V_{DD}$ = 5 V, and $V_{SS}$ = 0 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions.
[3] The maximum current in each code is defined by $I_{AW} = (V_{DD} - 1)/R_{AW}$.
[4] Guaranteed by design and not subject to production test.
[5] See Figure 9 for more details.
[6] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[7] Different from operating current; the supply current for the fuse program lasts approximately 55 ms.
[8] Different from operating current; the supply current for the fuse read lasts approximately 500 ns.
[9] $P_{DISS}$ is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[10] All dynamic characteristics use $V_{DD}$ = +2.5 V, $V_{SS}$ = −2.5 V.

## INTERFACE TIMING SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V; $V_{DD}$ = 2.5 V, $V_{SS}$ = −2.5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | Limit[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| $t_1$[2] | 20 | ns min | SCLK cycle time |
| $t_2$ | 10 | ns min | SCLK high time |
| $t_3$ | 10 | ns min | SCLK low time |
| $t_4$ | 15 | ns min | $\overline{SYNC}$ to SCLK falling edge setup time |
| $t_5$ | 5 | ns min | Data setup time |
| $t_6$ | 5 | ns min | Data hold time |
| $t_7$ | 1 | ns min | SCLK falling edge to $\overline{SYNC}$ rising edge |
| $t_8$[3] | 400 | ns min | Minimum $\overline{SYNC}$ high time |
| $t_9$ | 15 | ns min | $\overline{SYNC}$ rising edge to next SCLK fall ignored |
| $t_{10}$[4] | 450 | ns max | SCLK rising edge to SDO valid |
| $t_{MEMORY\_READ}$ | 6 | µs max | Memory readback execute time |
| $t_{MEMORY\_PROGRAM}$ | 350 | ms max | Memory program time |
| $t_{RESET}$ | 600 | µs max | Reset OTP restore time |
| $t_{POWER\text{-}UP}$[5] | 2 | ms max | Power-on 50-TP restore time |

[1] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Maximum SCLK frequency is 50 MHz.
[3] Refer to $t_{MEMORY\_READ}$ and $t_{MEMORY\_PROGRAM}$ for memory commands operations.
[4] $R_{PULL\_UP}$ = 2.2 kΩ to $V_{DD}$ with a capacitance load of 168 pF.
[5] Maximum time after $V_{DD} - V_{SS}$ is equal to 2.5 V.

### *Shift Register and Timing Diagrams*

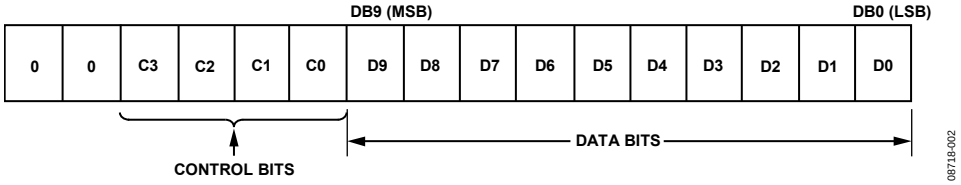



*Figure 2. Shift Register Content*

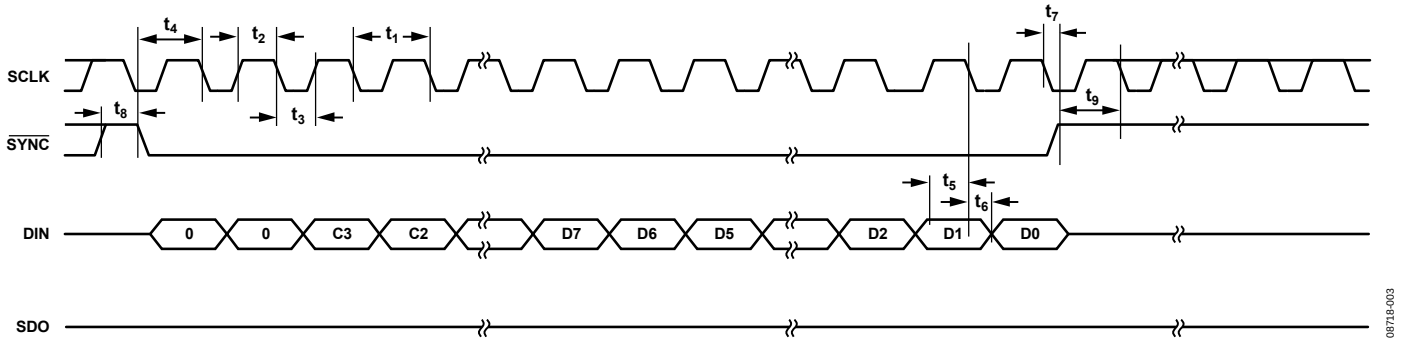



*Figure 3. Write Timing Diagram, CPOL=0, CPHA = 1*

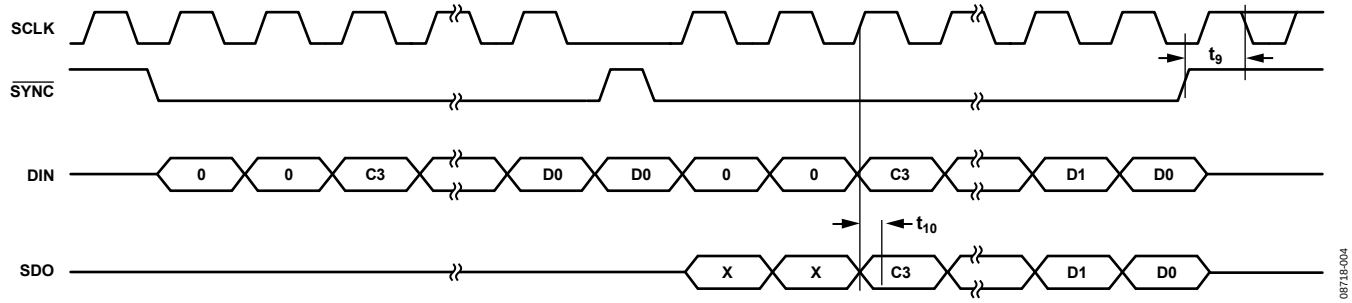



*Figure 4. Read Timing Diagram, CPOL=0, CPHA = 1*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7.0 V |
| $V_{SS}$ to GND | +0.3 V to −7.0 V |
| $V_{DD}$ to $V_{SS}$ | 7 V |
| $V_A$, $V_W$ to GND | $V_{SS}$ − 0.3 V, $V_{DD}$ + 0.3 V |
| Digital Input and Output Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| EXT_CAP to $V_{SS}$ | 7 V |
| $I_A$, $I_W$ | |
| Pulsed[1] | |
| Frequency > 10 kHz | ±6 mA/d[2] |
| Frequency ≤ 10 kHz | ±6 mA/√d[2] |
| Continuous | ±6 mA |
| Operating Temperature Range[3] | −40°C to +125°C |
| Maximum Junction Temperature ($T_J$ Maximum) | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Reflow Soldering | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 20 sec to 40 sec |
| Package Power Dissipation | ($T_J$ max − $T_A$)/$\theta_{JA}$ |

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A and W terminals at a given resistance.
[2] Pulse duty factor.
[3] Includes programming of 50-TP memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

**Table 4. Thermal Resistance.**

| Package Type | $\theta_{JA}$[1] | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 10-Lead LFCSP | 50 | 3 | °C/W |
| 10-Lead MSOP | 135 | N/A | °C/W |

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

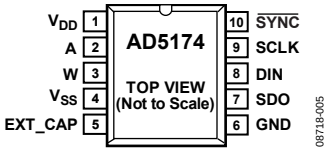



*Figure 5. MSOP Pin Configuration*

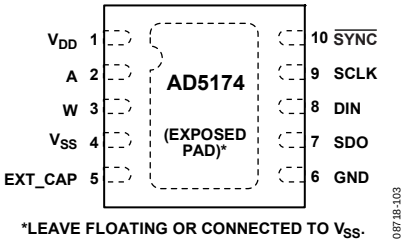



*Figure 6. LFCSP Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD}$ | Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors. |
| 2 | A | Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$. |
| 3 | W | Wiper Terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$. |
| 4 | $V_{SS}$ | Negative Supply. Connect to 0 V for single-supply applications. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors. |
| 5 | EXT_CAP | External Capacitor. Connect a 1 µF capacitor between EXT_CAP and $V_{SS}$. This capacitor must have a voltage rating of ≥7 V. |
| 6 | GND | Ground Pin, Logic Ground Reference. |
| 7 | SDO | Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the shift register in daisy-chain mode or in readback mode. |
| 8 | DIN | Serial Data Line. This pin is used in conjunction with the SCLK line to clock data into or out of the 16-bit input register. |
| 9 | SCLK | Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz. |
| 10 | $\overline{\text{SYNC}}$ | Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register and data is transferred in on the falling edges of the subsequent clocks. The selected register is updated on the rising edge of $\overline{\text{SYNC}}$ following the 16th clock cycle. If $\overline{\text{SYNC}}$ is taken high before the 16th clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the RDAC. |
| EPAD | Exposed Pad | Leave floating or connected to $V_{SS}$ |

# TYPICAL PERFORMANCE CHARACTERISTICS

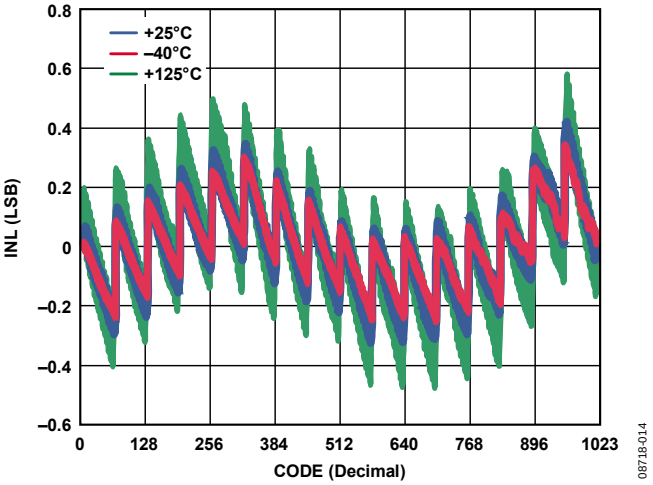



Figure 7. R-INL vs. Code vs. Temperature

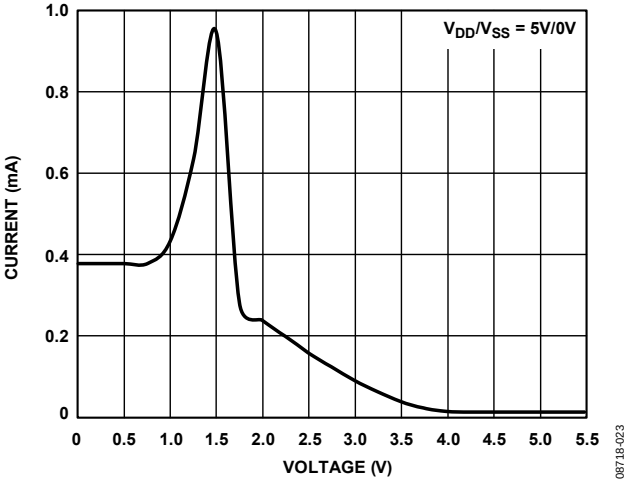



Figure 10. Supply Current ($I_{DD}$) vs. Digital Input Voltage

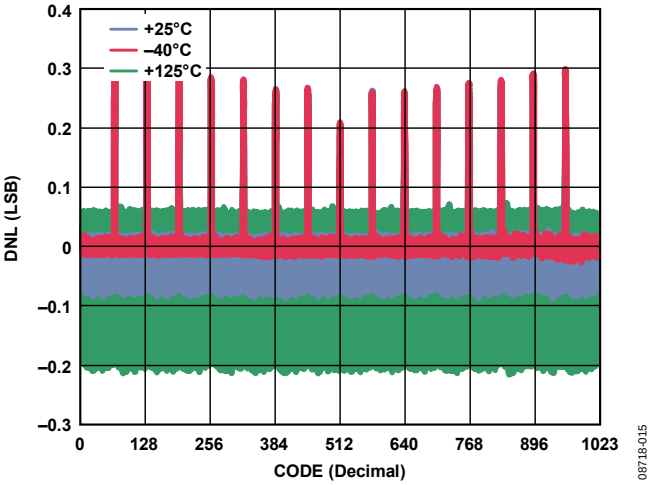



Figure 8. R-DNL vs. Code vs. Temperature

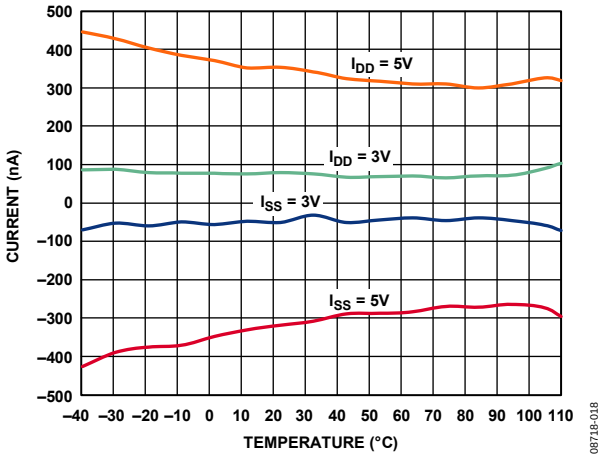



Figure 11. Supply Current ($I_{DD}$, $I_{SS}$) vs. Temperature

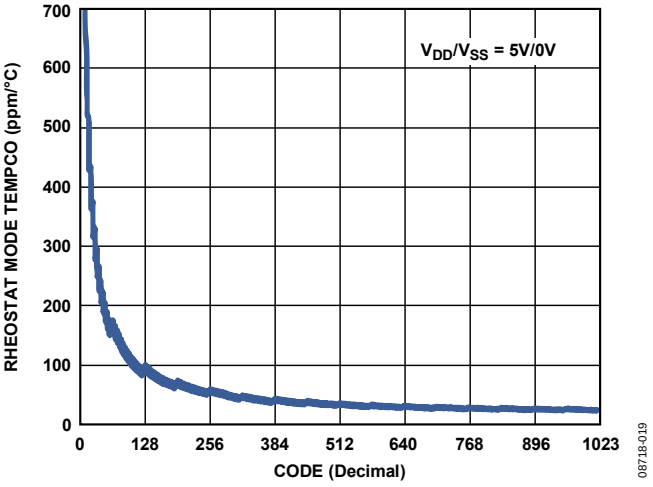



Figure 9. Tempco $\Delta R_{WA}/\Delta T$ vs. Code

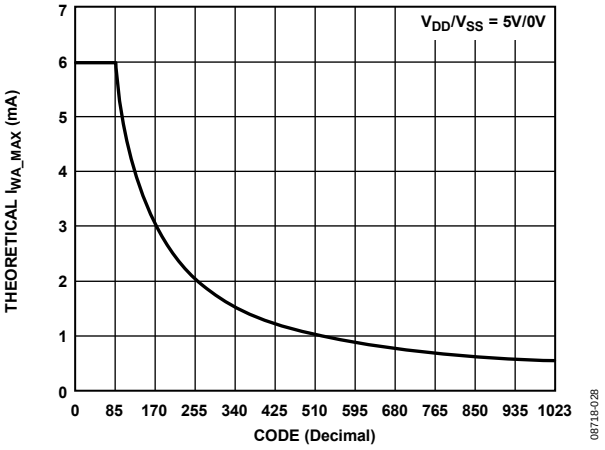



Figure 12. Theoretical Maximum Current vs. Code

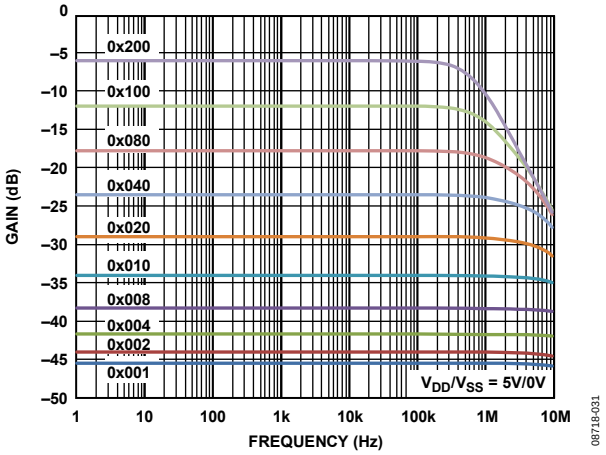



Figure 13. Bandwidth vs. Frequency vs. Code

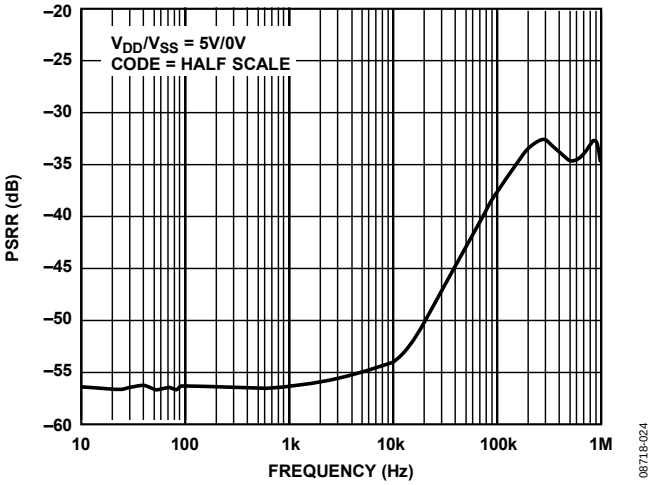



Figure 16. PSRR vs. Frequency

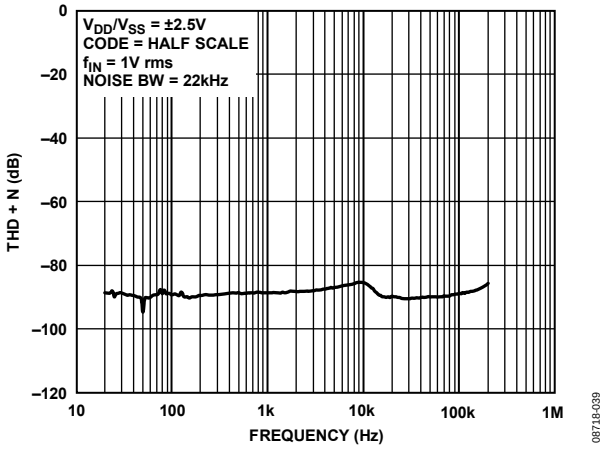



Figure 14. THD + N vs. Frequency

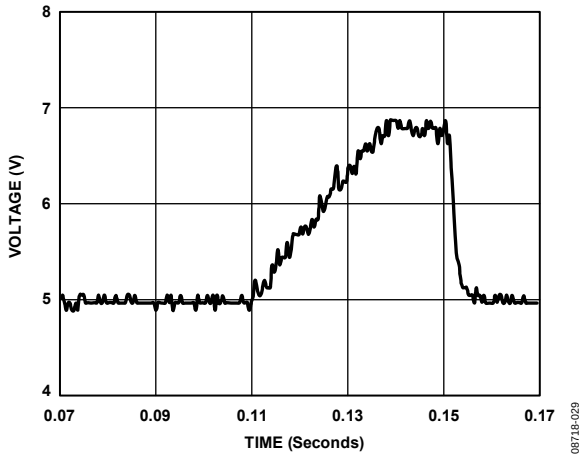



Figure 17. $V_{EXT\_CAP}$ Waveform While Writing Fuse

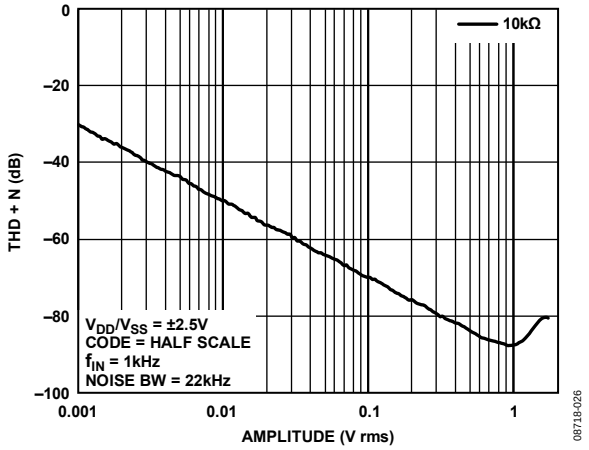



Figure 15. THD + N vs. Amplitude

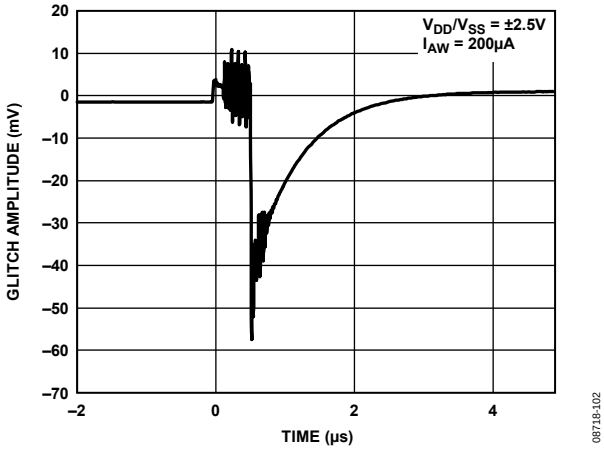



Figure 18. Maximum Glitch Energy

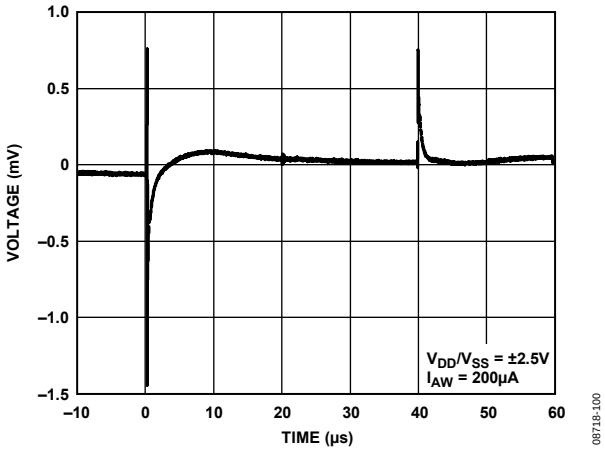



Figure 19. Digital Feedthrough

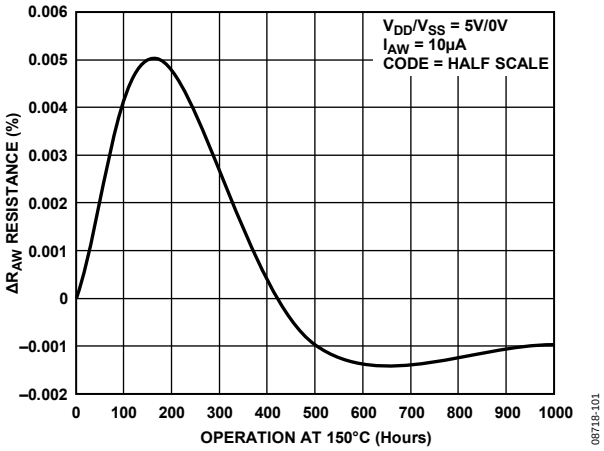



Figure 20. Long-Term Drift Accelerated Average by Burn-In

# TEST CIRCUITS

Figure 21 to Figure 25 define the test conditions used in the Specifications section.

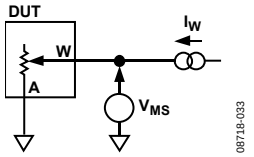



*Figure 21. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)*

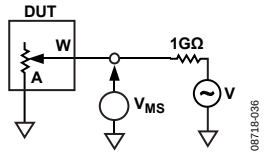



*Figure 24. Gain vs. Frequency*

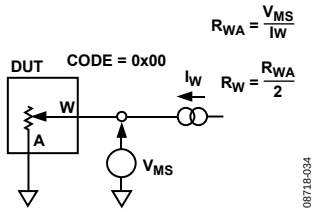



*Figure 22. Wiper Resistance*

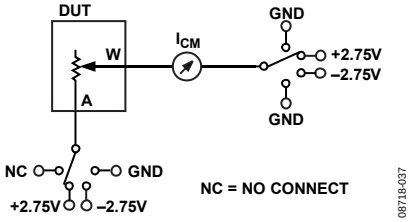



*Figure 25. Common Leakage Current*

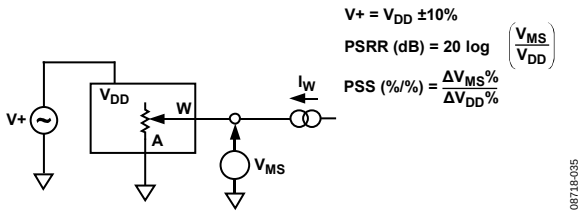



*Figure 23. Power Supply Sensitivity (PSS, PSRR)*

# THEORY OF OPERATION

The AD5174 is designed to operate as a true variable resistor for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The RDAC register contents determine the resistor wiper position. The RDAC register acts as a scratchpad register, which allows unlimited changes of resistance settings. The RDAC register can be programmed with any position setting by using the SPI interface. When a desirable wiper position is found, this value can be stored in a 50-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-ups. The storing of 50-TP data takes approximately 350 ms; during this time, the AD5174 locks to prevent any changes from taking place.

The AD5174 also feature a patented 1% end-to-end resistor tolerance. This simplifies precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

## SERIAL DATA INTERFACE

The AD5174 contains a serial interface ($\overline{SYNC}$, SCLK, DIN, and SDO) that is compatible with SPI interface standards, as well as most DSPs. This device allows writing of data via the serial interface to every register.

## SHIFT REGISTER

The shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of two unused bits, which should be set to 0, followed by four control bits and 10 RDAC data bits. Data is loaded MSB first (Bit D9). The four control bits determine the function of the software command as listed in Table 6. Figure 3 shows a timing diagram of a typical AD5174 write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. The $\overline{SYNC}$ pin must be held low until the complete data-word is loaded from the DIN pin. When $\overline{SYNC}$ returns high, the serial data-word is decoded according to the instructions in Table 6. The command bits (Cx) control the operation of the digital potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The AD5174 has an internal counter that counts a multiple of 16 bits (a frame) for proper operation. For example, AD5174 works with a 32-bit word but does not work properly with a 31-bit or 33-bit word. The AD5174 does not require a continuous SCLK when $\overline{SYNC}$ is high. To minimize power consumption in the digital input buffers, operate all serial interface pins close to the $V_{DD}$ supply rails.

## RDAC REGISTER

The RDAC register directly controls the position of the digital rheostat wiper. For example, when the RDAC register is loaded with all 0s, the wiper is connected to Terminal A of the variable resistor. The RDAC register is a standard logic register, and there is no restriction on the number of changes allowed. The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the serial data input register with Command 1 (see Table 6) and with the desired wiper position data.

## 50-TP MEMORY BLOCK

The AD5174 contains an array of 50-TP programmable memory registers, which allow the wiper position to be programmed up to 50 times. Table 10 shows the memory map. When the desired wiper position is determined, the user can load the serial data input register with Command 3 (see Table 6), which stores the wiper position data in a 50-TP memory register. The first address to be programmed is Location 0x01 (see Table 10); the AD5174 increments the 50-TP memory address for each subsequent program until the memory is full. Programming data to 50-TP consumes approximately 4 mA for 55 ms, and takes approximately 350 ms to complete, during which time the shift register locks to prevent any changes from occurring. Bit C2 of the control register can be polled to verify that the fuse program command was completed properly. No change in supply voltage is required to program the 50-TP memory; however, a 1 µF capacitor on the EXT_CAP pin is required (see Figure 28). Prior to 50-TP activation, the AD5174 presets to midscale on power-up.

## WRITE PROTECTION

At power-up, the serial data input register write commands for both the RDAC register and the 50-TP memory registers are disabled. The RDAC write protect bit, C1, of the control register (see Table 8 and Table 9) is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 50-TP memory using the software reset, Command 4 (see Table 6). To enable programming of the RDAC register, the write protect bit (Bit C1), of the control register must first be programmed by loading the serial data input register with Command 7. To enable programming of the 50-TP memory, the program enable bit (Bit C0) of the control register, which is set to 0 by default, must first be set to 1.

## RDAC AND 50-TP READ OPERATION

A serial data output SDO pin is available for readback of the internal RDAC register or 50-TP memory contents. The contents of the RDAC register can be read back through SDO by using Command 2 (see Table 6). Data from the RDAC register is clocked out of the SDO pin during the last 10 clocks of the next SPI operation.

It is possible to read back the contents of any of the 50-TP memory registers through SDO by using Command 5. The lower six LSB bits, D5 to D0 of the data byte, select which memory location is to be read back, as shown in Table 10.

Data from the selected memory location is clocked out of the SDO pin during the next SPI operation. A binary encoded version address of the most recently programmed wiper memory location can be read back using Command 6 (see Table 6). This can be used to monitor the spare memory status of the 50-TP memory block.

Table 7 provides a sample listing for the sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format for a write and read to both the RDAC register and the 50-TP memory (Memory Location 20).

**Table 6. Command Operation Truth Table**

| Command Number | Command[DB13:DB10] | | | | Data[DB9:DB0][1] | | | | | | | | | | Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C3 | C2 | C1 | C0 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | NOP: do nothing. |
| 1 | 0 | 0 | 0 | 1 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write contents of serial register data to RDAC. |
| 2 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | Read contents of RDAC wiper register. |
| 3 | 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | Store wiper setting: store RDAC setting to 50-TP. |
| 4 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | Software reset: refresh RDAC with last 50-TP memory stored value. |
| 5[2] | 0 | 1 | 0 | 1 | X | X | X | X | D5 | D4 | D3 | D2 | D1 | D0 | Read contents of 50-TP from SDO output in the next frame. |
| 6 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | Read address of last 50-TP programmed memory location. |
| 7[3] | 0 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | D1 | D0 | Write contents of serial register data to control register. |
| 8 | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | Read contents of control register. |
| 9 | 1 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | D0 | Software shutdown.<br>D0 = 0; normal mode.<br>D0 = 1; device placed in shutdown mode. |

[1] X is don't care.
[2] See Table 10 for 50-TP memory map.
[3] See Table 9 for bit details.

## SHUTDOWN MODE

The AD5174 can be shut down by executing the software shutdown command, Command 9 (see Table 6), and setting the LSB to 1. This feature places the RDAC in a zero-power-consumption state where Terminal A is open circuited and the wiper terminal, W, remains connected. It is possible to execute any command from Table 6 while the AD5174 is in shutdown mode. The parts can be taken out of shutdown mode by executing Command 9 and setting the LSB to 0 or by a software reset, Command 4 (see Table 6).

## RESET

The AD5174 can be reset through software by executing Command 4 (see Table 6). The reset command loads the RDAC register with the contents of the most recently programmed 50-TP memory location. The RDAC register loads with midscale if no 50-TP memory location has been previously programmed.

**Table 7. Write and Read to RDAC and 50-TP Memory**

| DIN | SDO[1] | Action |
|---|---|---|
| 0x1C03 | 0xXXXX | Enable update of the wiper position and the 50-TP memory contents through the digital interface. |
| 0x0500 | 0x1C03 | Write 0x100 to the RDAC register; wiper moves to ¼ full-scale position. |
| 0x0800 | 0x0500 | Prepares data read from RDAC register. |
| 0x0C00 | 0x100 | Stores RDAC register content into the 50-TP memory. A 16-bit word appears out of SDO, where the last 10 bits contain the contents of the RDAC register (0x100). |
| 0x1800 | 0x0C00 | Prepares data read of the last programmed 50-TP memory monitor location. |
| 0x0000 | 0xXX19 | NOP Instruction 0 sends a 16-bit word out of SDO, where the six LSBs (that is, last six bits) contain the binary address of the last programmed 50-TP memory location, for example, 0x19 (see Table 10). |
| 0x1419 | 0x0000 | Prepares data read from Memory Location 0x19. |
| 0x2000 | 0x0100 | Prepares data read from the control register. Sends a 16-bit word out of SDO, where the last 10 bits contain the contents of Memory Location 0x19. |
| 0x0000 | 0xXXXX | NOP Instruction 0 sends a 16-bit word out of SDO, where the last four bits contain the contents of the control register. If Bit C2 = 1, the fuse program command was successful. |

[1] X is don't care.

**Table 8. Control Register Bit Map**

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | C2 | 0 | C1 | C0 |

**Table 9. Control Register Bit Description**

| Bit Name | Description |
|---|---|
| C0 | 50-TP program enable<br>0 = 50-TP program disabled (default)<br>1 = enable device for 50-TP program |
| C1 | RDAC register write protect<br>0 = wiper position frozen to value in 50-TP memory (default)[1]<br>1 = allow update of wiper position through digital interface |
| C2 | 50-TP memory program success bit<br>0 = fuse program command was unsuccessful (default)<br>1 = fuse program command was successful |

[1] Wiper position frozen to the last value programmed in the 50-TP memory. The wiper is frozen to midscale if the 50-TP memory has not been previously programmed.

**Table 10. Memory Map**

| | Data Byte[DB9:DB0][1] | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Command Number** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Register Contents** |
| 5 | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reserved |
| | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1st programmed wiper location (0x01) |
| | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2nd programmed wiper location (0x02) |
| | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3rd programmed wiper location (0x03) |
| | X | X | X | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4th programmed wiper location (0x04) |
| | … | … | … | … | … | … | … | … | … | … | … |
| | X | X | X | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 10th programmed wiper location (0xA) |
| | … | … | … | … | … | … | … | … | … | … | … |
| | X | X | X | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 20th programmed wiper location (0x14) |
| | … | … | … | … | … | … | … | … | … | … | … |
| | X | X | X | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 30th programmed wiper location (0x1E) |
| | … | … | … | … | … | … | … | … | … | … | … |
| | X | X | X | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 40th programmed wiper location (0x28) |
| | … | … | … | … | … | … | … | … | … | … | … |
| | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 50th programmed wiper location (0x32) |
| | … | … | … | … | … | … | … | … | … | … | … |
| | X | X | X | 0 | 1 | 1 | 1 | 0 | 0 | 1 | MSB resistance tolerance (0x39) |
| | X | X | X | 0 | 1 | 1 | 1 | 0 | 1 | 0 | LSB resistance tolerance (0x3A) |

[1] X is don't care.

## DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes: it can be used to read the contents of the wiper setting and 50-TP values using Command 2 and Command 5, respectively (see Table 6), or the SDO pin can be used in daisy-chain mode. The remaining instructions are valid for daisy chaining multiple devices in simultaneous operations. Data is clocked out of SDO on the rising edge of SCLK. Daisy chaining minimizes the number of port pins required from the controlling IC. The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor if this pin is used. As shown in Figure 26, users need to tie the SDO pin of one package to the DIN pin of the next package. Users may need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO-to-DIN interface may require additional time delay between subsequent devices. When two AD5174 devices are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1. Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

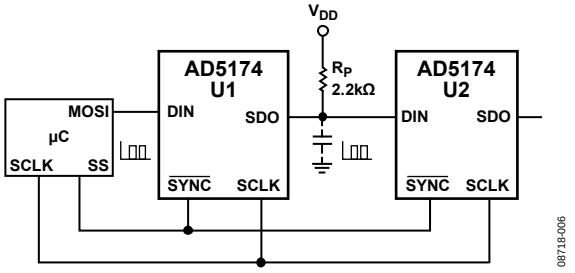



*Figure 26. Daisy-Chain Configuration Using SDO*

## RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5174 employs a three-stage segmentation approach as shown in Figure 27. The AD5174 wiper switch is designed with the transmission gate CMOS topology.

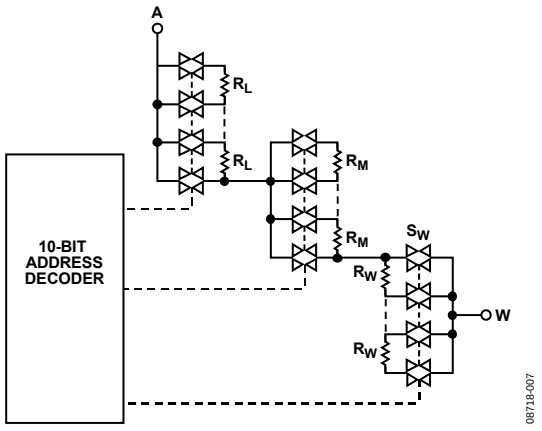



*Figure 27. Simplified RDAC Circuit*

## PROGRAMMING THE VARIABLE RESISTOR

### *Rheostat Operation*

The nominal resistance between Terminal W and Terminal A, $R_{WA}$, is 10 kΩ and has 1024-tap points accessed by the wiper terminal. The 10-bit data in the RDAC latch is decoded to select one of the 1024 possible wiper settings. As a result, the general equation for determining the digitally programmed output resistance between the W terminal and the A terminal is

$$R_{WA}(D) = \frac{D}{1024} \times R_{WA} \quad (1)$$

where:
*D* is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.
$R_{WA}$ is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of which setting the part is operating in, take care to limit the current between Terminal A and Terminal W to the maximum continuous current of ±6 mA or a pulse current specified in Table 3. Otherwise, degradation or possible destruction of the internal switch contact may occur.

### *Calculate the Actual End-to-End Resistance*

The resistance tolerance is stored in the internal memory during factory testing. The actual end-to-end resistance can, therefore, be calculated (which is valuable for calibration, tolerance matching, and precision applications).

The resistance tolerance (in percentage) is stored in fixed-point format, using a 16-bit sign magnitude binary. The sign bit(0 = negative and 1 = positive) and the integer part is located in Address 0x39 as shown in Table 10. Address 0x3A contains the fractional part as shown in Table 11.

That is, if the data readback from Address 0x39 is 0000001010 and data from Address 0x3A is 0010110000, then the end-to-end resistance can be calculated as follows.

For Memory Location 0x39,

DB[9:8]: XX = don't care

DB[7]: 0 = negative

DB[6:0]: 0001010 = 10

For Memory Location 0x3A,

DB[9:8]: XX = don't care

DB[7:0]: 10110000 = $176 \times 2^{-8}$ = 0.6875

Therefore, tolerance = −10.6875% and $R_{WA}$ (1023)= 8.931 kΩ.

**Table 11. End-to-End Resistance Tolerance Bytes**

| | Data Byte[1] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Memory Map Address** | **DB9** | **DB8** | **DB7** | **DB6** | **DB5** | **DB4** | **DB3** | **DB2** | **DB1** | **DB0** |
| 0x39 | X | X | Sign | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| 0x3A | X | X | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ |

[1] X is don't care.

## EXT_CAP CAPACITOR

A 1 µF capacitor to $V_{SS}$ must be connected to the EXT_CAP pin, as shown in Figure 28, on power-up and throughout the operation of the AD5174.

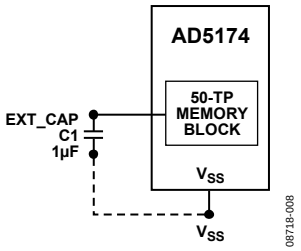



*Figure 28. EXT_CAP Hardware Setup*

## TERMINAL VOLTAGE OPERATING RANGE

The positive $V_{DD}$ and negative $V_{SS}$ power supplies of the AD5174 define the boundary conditions for proper 2-terminal digital resistor operation. Supply signals present on Terminal A and Terminal W that exceed $V_{DD}$ or $V_{SS}$ are clamped by the internal forward-biased diodes (see Figure 29).

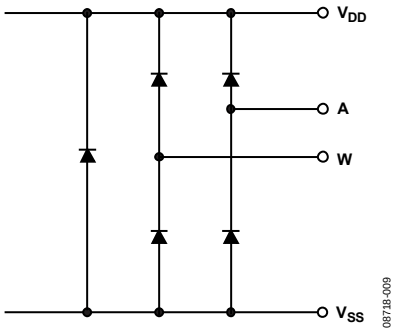



*Figure 29. Maximum Terminal Voltages Set by $V_{DD}$ and $V_{SS}$*

The ground pin of the AD5174 is primarily used as a digital ground reference. To minimize the digital ground bounce, join the AD5174 ground terminal remotely to the common ground. The digital input control signals to the AD5174 must be referenced to the device ground pin (GND) and must satisfy the logic level defined in the Specifications section. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from $V_{SS}$ to $V_{DD}$, regardless of the digital input level.

## POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A and Terminal W (see Figure 29), it is important to power $V_{DD}/V_{SS}$ first before applying any voltage to Terminal A and Terminal W; otherwise, the diode is forward-biased such that $V_{DD}/V_{SS}$ are powered unintentionally. The ideal power-up sequence is $V_{SS}$, GND, $V_{DD}$, digital inputs, $V_A$, and $V_W$. The order of powering $V_A$, $V_W$, and the digital inputs is not important as long as they are powered after $V_{DD}/V_{SS}$.

As soon as $V_{DD}$ is powered, the power-on preset activates, which first sets the RDAC to midscale and then restores the last programmed 50-TP value to the RDAC register.

# OUTLINE DIMENSIONS

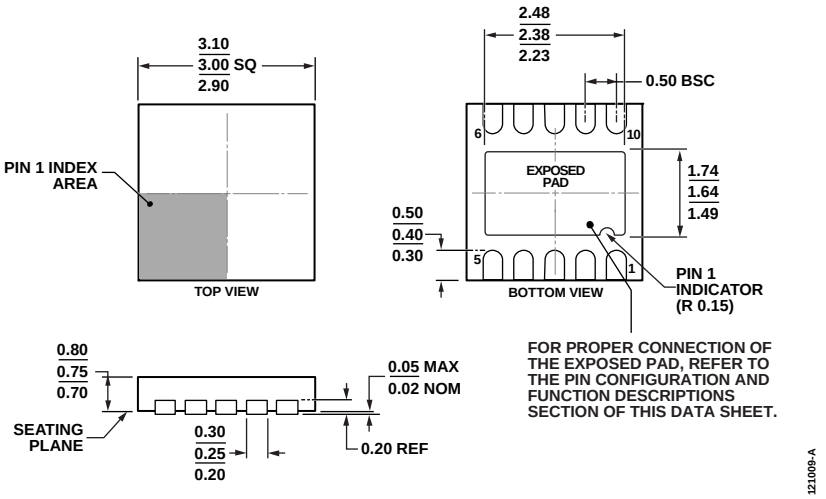
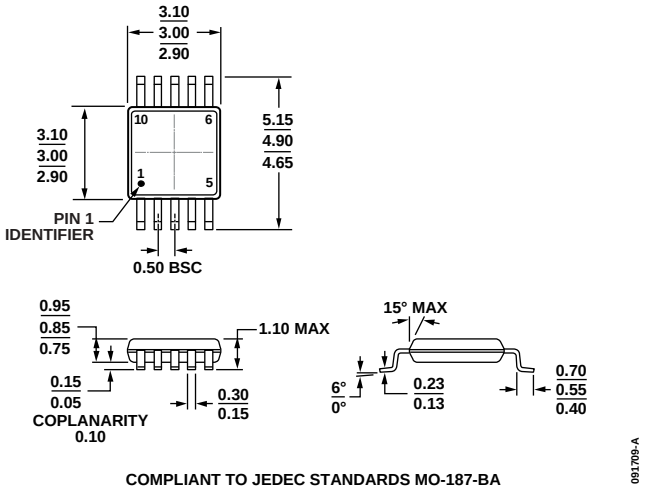



*Figure 30. 10-Lead Frame Chip Scale Package [LFCSP_WD]*
*3 mm × 3mm Body, Very Thin, Dual Lead*
*(CP-10-9)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-187-BA

*Figure 31. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | $R_{AB}$ (kΩ) | Resolution | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| AD5174BRMZ-10 | 10 | 1,024 | −40°C to +125°C | 10-Lead MSOP | RM-10 | DDT |
| AD5174BRMZ-10-RL7 | 10 | 1,024 | −40°C to +125°C | 10-Lead MSOP | RM-10 | DDT |
| AD5174BCPZ-10-R2 | 10 | 1,024 | −40°C to +125°C | 10-Lead LFCSP_WD | CP-10-9 | DEF |
| AD5174BCPZ-10-RL7 | 10 | 1,024 | −40°C to +125°C | 10-Lead LFCSP_WD | CP-10-9 | DEF |

[1] Z = RoHS Compliant Part.

## NOTES

# NOTES


D08718-0-3/10(0)