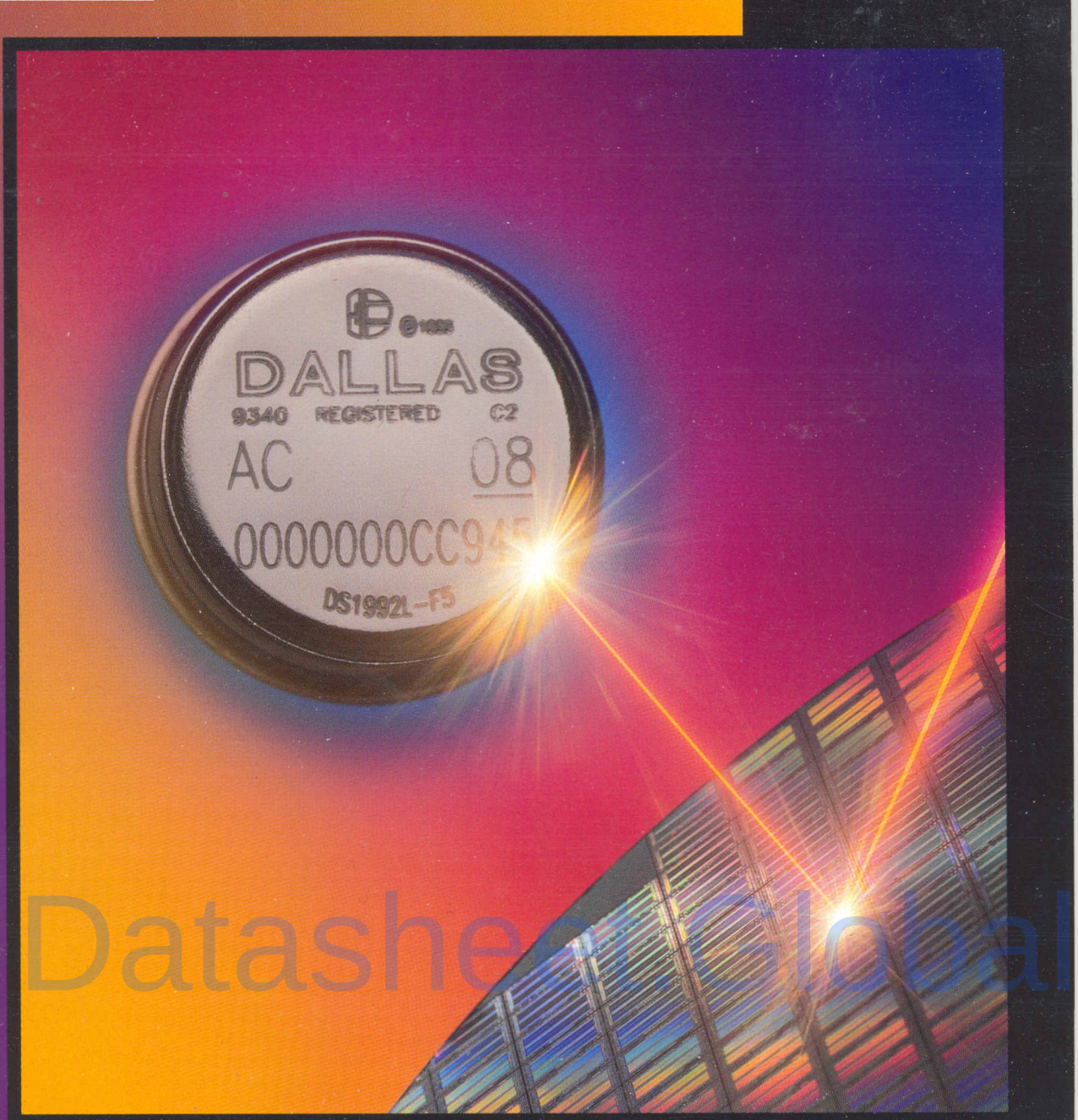

Automatic Identification Data Book

- Touch Memory
- EconoMemories
- Software Authorization

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Circuit diagrams are included to illustrate typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

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GENERAL INFORMATION

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS0620	SOFTWARE	N/A	DS0620	TMEX
DS1000	14–Pin DIP	0 to 70	DS1000–xxx	xxx = 020 to 500 ns
	14–Pin DIP Sheared NC	0 to 70	DS1000K–xxx	xxx = 020 to 500 ns
	8–Pin DIP	0 to 70	DS1000M–xxx	xxx = 020 to 500 ns
	14–Pin GULLWING	0 to 70	DS1000G–xxx	xxx = 020 to 500 ns
	8–Pin GULLWING	0 to 70	DS1000H–xxx	xxx = 020 to 500 ns
	16–Pin SOIC	0 to 70	DS1000S–xxx	xxx = 020 to 500 ns
	8–Pin SOIC	0 to 70	DS1000Z–xxx	xxx = 020 to 500 ns
DS1003	8-Pin DIP	0 to 70	DS1003M–16	
	8–Pin DIP	0 to 70	DS1003M–20	
	8–Pin DIP	0 to 70	DS1003M–25	
	8–Pin DIP	0 to 70	DS1003M–33	
	8–Pin DIP	0 to 70	DS1003M–40	
	8–Pin GULLWING	0 to 70	DS1003H–16	
	8–Pin GULLWING	0 to 70	DS1003H–20	
	8–Pin GULLWING	0 to 70	DS1003H–25	
	8–Pin GULLWING	0 to 70	DS1003H–33	
	8–Pin GULLWING	0 to 70	DS1003H–40	
	14–Pin DIP	0 to 70	DS1003–16	
	14–Pin DIP	0 to 70	DS1003–20	
	14–Pin DIP	0 to 70	DS1003–25	
	14–Pin DIP	0 to 70	DS1003–33	
	14–Pin DIP	0 to 70	DS1003–40	
	14–Pin GULLWING	0 to 70	DS1003G–16	
	14–Pin GULLWING	0 to 70	DS1003G–20	
	14–Pin GULLWING	0 to 70	DS1003G–25	
	14–Pin GULLWING	0 to 70	DS1003G–33	
	14–Pin GULLWING	0 to 70	DS1003G–40	
DS1004	8–Pin DIP	0 to 70	DS1004M–002	13 ns total delay
	8–Pin DIP	0 to 70	DS1004M–003	17 ns total delay
	8–Pin DIP	0 to 70	DS1004M–004	21 ns total delay
	8–Pin DIP	0 to 70	DS1004M–005	25 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–002	13 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–003	17 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–004	21 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–005	25 ns total delay
DS1005	14–Pin DIP	0 to 70	DS1005–xxx	xxx = 060 to 250 ns
	14–Pin DIP Sheared NC	0 to 70	DS1005K–xxx	xxx = 060 to 250 ns
	8–Pin DIP	0 to 70	DS1005M–xxx	xxx = 060 to 250 ns
	14–Pin GULLWING	0 to 70	DS1005G–xxx	xxx = 060 to 250 ns
	8–Pin GULLWING	0 to 70	DS1005H–xxx	xxx = 060 to 250 ns
	16–Pin SOIC	0 to 70	DS1005S–xxx	xxx = 060 to 250 ns
DS1007	16–Pin DIP	0 to 70	DS1007–xxx	xxx = 001 to 014
	16–Pin SOIC	0 to 70	DS1007S–xxx	xxx = 001 to 014

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1010	14–Pin DIP	0 to 70	DS1010–xxx	xxx = 050 to 500 ns
	14–Pin GULLWING	0 to 70	DS1010G–xxx	xxx = 050 to 500 ns
	16–Pin SOIC	0 to 70	DS1010S–xxx	xxx = 050 to 500 ns
DS1012	8–Pin DIP	0 to 70	DS1012M–xxx	
	8–Pin GULLWING	0 to 70	DS1012H–xxx	
	8–Pin SOIC	0 to 70	DS1012Z–xxx	
DS1013	14–Pin DIP	0 to 70	DS1013–xxx	xxx = 010 to 200 ns
	8–Pin DIP	0 to 70	DS1013M–xxx	xxx = 010 to 200 ns
	14–Pin GULLWING	0 to 70	DS1013G–xxx	xxx = 010 to 200 ns
	8–Pin GULLWING	0 to 70	DS1013H–xxx	xxx = 010 to 200 ns
	14–Pin Sheared	0 to 70	DS1013K–xxx	xxx = 010 to 200 ns
	16–Pin SOIC	0 to 70	DS1013S–xxx	xxx = 010 to 200 ns
DS1020	16–Pin DIP	0 to 70	DS1020–15	0.15 ns Steps
	16–Pin DIP	0 to 70	DS1020–25	0.25 ns Steps
	16–Pin DIP	0 to 70	DS1020–50	0.50 ns Steps
	16–Pin DIP	0 to 70	DS1020–100	1.00 ns Steps
	16–Pin DIP	0 to 70	DS1020–200	2.00 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–15	0.15 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–25	0.25 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–50	0.50 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–100	1.00 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–200	2.00 ns Steps
DS1033	8–Pin DIP	0 to 70	DS1033M–xxx	xxx = 008 to 030 ns
	8–Pin SOIC	0 to 70	DS1033Z–xxx	xxx = 008 to 030 ns
	20–Pin TSSOP	0 to 70	DS1033E–xxx	xxx = 008 to 030 ns
DS1035	8–Pin DIP	0 to 70	DS1035M–xxx	xxx = 006 to 030 ns
	8–Pin SOIC	0 to 70	DS1035Z–xxx	xxx = 006 to 030 ns
	20–Pin TSSOP	0 to 70	DS1035E–xxx	xxx = 006 to 030 ns
DS1040	8–Pin DIP	0 to 70	DS1040M–75	75 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–100	100 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–150	150 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–200	200 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–250	250 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–500	500 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–B50	50 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–D60	60 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A15	15 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A20	20 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A32	32.5 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–B40	40 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–D70	70 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–75	75 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–100	100 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–150	150 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–200	200 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–250	250 ns max pulse width

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin GULLWING	0 to 70	DS1040H–500	500 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–B50	50 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–D60	60 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–A15	15 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–A20	20 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–A32	32.5 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–B40	40 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–D70	70 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–75	75 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–100	100 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–150	150 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–200	200 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–250	250 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–500	500 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–B50	50 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–D60	60 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A15	15 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A20	20 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A32	32.5 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–B40	40 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–D70	70 ns max pulse width
DS1044	14–Pin DIP	0 to 70	DS1044–xxx	xxx = 005 to 025 ns
	14–Pin GULLWING	0 to 70	DS1044G–xxx	xxx = 005 to 025 ns
	14–Pin SOIC	0 to 70	DS1044R–xxx	xxx = 005 to 025 ns
DS1045	16–Pin DIP	0 to 70	DS1045–2	2 ns Steps
	16–Pin DIP	0 to 70	DS1045–3	3 ns Steps
	16–Pin DIP	0 to 70	DS1045–4	4 ns Steps
	16–Pin DIP	0 to 70	DS1045–5	5 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–2	2 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–3	3 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–4	4 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–5	5 ns Steps
DS1200	10–Pin DIP	0 to 70	DS1200	
	10–Pin DIP	–40 to +85	DS1200N	
	16–Pin SOIC	0 to 70	DS1200S	
	16–Pin SOIC	–40 to +85	DS1200SN	
DS1201	Electronic Key/Tag	0 to 70	DS1201	
DS1202	8–Pin DIP	0 to 70	DS1202	24 x 8 RAM
	8–Pin DIP	–40 to +85	DS1202N	24 x 8 RAM
	8–Pin SOIC	0 to 70	DS1202S–8	24 x 8 RAM
	16–Pin SOIC	0 to 70	DS1202S	24 x 8 RAM
	16–Pin SOIC	–40 to +85	DS1202SN	24 x 8 RAM
DS1204V	Electronic Key/Tag	0 to +70	DS1204U–G01	Generic Code #1
		0 to +70	DS1204U–G02	Generic Code #2
		0 to +70	DS1204U–G03	Generic Code #3
		0 to +70	DS1204U–G04	Generic Code #4

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
		0 to +70	DS1204U–G05	Generic Code #5
		0 to +70	DS1204U–xxx	xxx = 011 to 999
		0 to +70	DS1204U–G1C	Generic Code #1 w/cap
		0 to +70	DS1204U–G2C	Generic Code #2 w/cap
		0 to +70	DS1204U–G3C	Generic Code #3 w/cap
		0 to +70	DS1204U–G4C	Generic Code #4 w/cap
		0 to +70	DS1204U–G5C	Generic Code #5 w/cap
DS1205S	16–Pin SOIC	0 to +70	DS1205S	
	16–Pin SOIC	–40 to +85	DS1205SN	
DS1205V	Electronic Key/Tag	0 to +70	DS1205U	
DS1206	14–Pin DIP	0 to 70	DS1206	
	14–Pin DIP	–40 to +85	DS1206N	
	16–Pin SOIC	0 to 70	DS1206S	
	16–Pin SOIC	–40 to +85	DS1206SN	
DS1207	Electronic Key/Tag	0 to +70	DS1207–G01	Generic Code #1
		0 to +70	DS1207–G02	Generic Code #2
		0 to +70	DS1207–G03	Generic Code #3
		0 to +70	DS1207–G04	Generic Code #4
		0 to +70	DS1207–G05	Generic Code #5
		0 to +70	DS1207–xxx	xxx = 001 to 999
		0 to +70	DS1207–G1C	Generic Code #1 w/cap
		0 to +70	DS1207–G2C	Generic Code #2 w/cap
		0 to +70	DS1207–G3C	Generic Code #3 w/cap
		0 to +70	DS1207–G4C	Generic Code #4 w/cap
		0 to +70	DS1207–G5C	Generic Code #5 w/cap
DS1210	8–Pin DIP	0 to 70	DS1210	
	8–Pin DIP	–40 to +85	DS1210N	
	16–Pin SOIC	0 to 70	DS1210S	
	16–Pin SOIC	–40 to +85	DS1210SN	
DS1211	20–Pin DIP	0 to 70	DS1211	
	20–Pin DIP	–40 to +85	DS1211N	
	20–Pin SOIC	0 to 70	DS1211S	
	20–Pin SOIC	–40 to +85	DS1211SN	
DS1212	28–Pin DIP	0 to 70	DS1212	
	28–Pin DIP	–40 to +85	DS1212N	
	28–Pin PLCC	0 to 70	DS1212Q	
	28–Pin PLCC	–40 to +85	DS1212QN	
DS1213B	Socket	0 to 70	DS1213B	
DS1213C	Socket	0 to 70	DS1213C	
DS1213D	Socket	0 to 70	DS1213D	
DS1215	16–Pin DIP	0 to 70	DS1215	
	16–Pin DIP	–40 to +85	DS1215N	
	16–Pin SOIC	0 to 70	DS1215S	
DS1216B	28–Pin Socket	0 to 70	DS1216B	16K/64K RAM
DS1216C	28–Pin Socket	0 to 70	DS1216C	64K/256K RAM
DS1216D	32–Pin Socket	0 to 70	DS1216D	256K/1M RAM

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1216E	28–Pin Socket	0 to 70	DS1216E	64K/256K ROM
DS1216F	32–Pin Socket	0 to 70	DS1216F	64K/256K/1M ROM
DS1217A		0 to +70	DS1217A 16K–25	16K Bit Density
		0 to +70	DS1217A 64K–25	64K Bit Density
		0 to +70	DS1217A 128K–25	128K Bit Density
		0 to +70	DS1217A 192K–25	192K Bit Density
		0 to +70	DS1217A 256K–25	256K Bit Density
DS1217M		0 to +70	DS1217M 512–25	512K Bit Density
		0 to +70	DS1217M 1–15	1 Megabit Density
		0 to +70	DS1217M 2–25	2 Megabit Density
		0 to +70	DS1217M 3–25	3 Megabit Density
		0 to +70	DS1217M 4–25	4 Megabit Density
DS1218	8–Pin DIP	0 to 70	DS1218	
	8–Pin SOIC	0 to 70	DS1218S	
DS1220AB/AD	24–Pin Encap. DIP	0 to +70	DS1220AB–200	200 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–150	150 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–120	120 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–100	100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AB–200–IND	200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AB–100–IND	100 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–200	200 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–150	150 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–120	120 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–100	100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AD–200–IND	200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AD–100–IND	100 ns
DS1220Y	24–Pin Encap. DIP	0 to 70	DS1220Y–200	200 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–150	150 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–120	120 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–100	100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220Y–200–IND	200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220Y–100–IND	100 ns
DS1221	16–Pin DIP	0 to 70	DS1221	
	16–Pin DIP	–40 to +85	DS1221N	
	16–Pin SOIC	0 to 70	DS1221S	
	16–Pin SOIC	–40 to +85	DS1221SN	
DS1222	14–Pin DIP	0 to 70	DS1222	
	14–Pin DIP	–40 to +85	DS1222N	
	16–Pin SOIC	0 to 70	DS1222S	
	16–Pin SOIC	–40 to +85	DS1222SN	
DS1225AB/AD	28–Pin Encap. DIP	0 to 70	DS1225AB–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–150–IND	150 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin Encap. DIP	–40 to +85	DS1225AB–70–IND	70 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–150–IND	150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–70–IND	70 ns
DS1225Y	28–Pin Encap. DIP	0 to 70	DS1225Y–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1225Y–170	170 ns
	28–Pin Encap. DIP	0 to 70	DS1225Y–150	150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225Y–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225Y–150–IND	150 ns
DS1228	16–Pin DIP	0 to 70	DS1228	
	16–Pin SOIC	0 to 70	DS1228S	
DS1229	20–Pin DIP	0 to 70	DS1229	
	20–Pin SOIC	0 to 70	DS1229S	
DS1230Y/AB	28–Pin Encap. DIP	0 to 70	DS1230AB–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–120–IND	120 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–70–IND	70 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–120–IND	120 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–70–IND	70 ns
DS1231	8–Pin DIP	0 to 70	DS1231–20	20
	8–Pin DIP	0 to 70	DS1231–35	35
	8–Pin DIP	0 to 70	DS1231–50	50
	8–Pin DIP	–40 to +85	DS1231N–20	20
	8–Pin DIP	–40 to +85	DS1231N–35	35
	8–Pin DIP	–40 to +85	DS1231N–50	50
	8–Pin GULLWING	0 to 70	DS1231G–20	20
	8–Pin GULLWING	0 to 70	DS1231G–35	35
	8–Pin GULLWING	0 to 70	DS1231G–50	50
	8–Pin GULLWING	–40 to +85	DS1231GN–20	20
	8–Pin GULLWING	–40 to +85	DS1231GN–35	35

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin GULLWING	–40 to +85	DS1231GN–50	50
	16–Pin SOIC	0 to 70	DS1231S–20	20
	16–Pin SOIC	0 to 70	DS1231S–35	35
	16–Pin SOIC	0 to 70	DS1231S–50	50
	16–Pin SOIC	–40 to +85	DS1231SN–20	20
	16–Pin SOIC	–40 to +85	DS1231SN–35	35
	16–Pin SOIC	–40 to +85	DS1231SN–50	50
DS1232	8–Pin DIP	0 to 70	DS1232	
	8–Pin DIP	–40 to +85	DS1232N	
	8–Pin GULLWING	0 to 70	DS1232G	
	8–Pin GULLWING	–40 to +85	DS1232GN	
	16–Pin SOIC	0 to 70	DS1232S	
	16–Pin SOIC	–40 to +85	DS1232SN	
DS1232LP	8–Pin DIP	0 to 70	DS1232LP	
	8–Pin DIP	–40 to +85	DS1232LPN	
	8–Pin SOIC	0 to 70	DS1232LPS–2	
	8–Pin SOIC	–40 to _85	DS1232LPSN–2	
	16–Pin SOIC	0 to 70	DS1232LPS	
	16–Pin SOIC	–40 to +85	DS1232LPSN	
DS1233 5V	TO–92	–40 to +85	DS1233–5	5% MONITOR
	TO–92	–40 to +85	DS1233–10	10% MONITOR
	TO–92	–40 to +85	DS1233–15	15% MONITOR
	SOT–223	–40 to +85	DS1233Z–5	5% MONITOR
	SOT–223	–40 to +85	DS1233Z–10	10% MONITOR
	SOT–223	–40 to +85	DS1233Z–15	15% MONITOR
DS1233A 3.3V	TO–92	–40 to +85	DS1233A–10	10% MONITOR
	TO–92	–40 to +85	DS1233A–15	15% MONITOR
	SOT–223	–40 to +85	DS1233AZ–10	10% MONITOR
	SOT–223	–40 to +85	DS1233AZ–15	15% MONITOR
DS1233D 5V	TO–92	–40 to +85	DS1233D–5	5% MONITOR
	TO–92	–40 to +85	DS1233D–10	10% MONITOR
	TO–92	–40 to +85	DS1233D–15	15% MONITOR
	SOT–223	–40 to +85	DS1233DZ–5	5% MONITOR
	SOT–223	–40 to +85	DS1233DZ–10	10% MONITOR
	SOT–223	–40 to +85	DS1233DZ–15	15% MONITOR
DS1234	14–Pin DIP	0 to 70	DS1234	
	16–Pin SOIC	0 to 70	DS1234S	
DS1236	16–Pin DIP	0 to 70	DS1236	10% MONITOR
	16–Pin DIP	0 to 70	DS1236–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236N–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1236S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1236S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN–5	5% MONITOR

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1236A	16–Pin DIP	0 to 70	DS1236A	10% MONITOR
	16–Pin DIP	0 to 70	DS1236A–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236AN	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236AN–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1236AS	10% MONITOR
	16–Pin SOIC	0 to 70	DS1236AS–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236ASN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236ASN–5	5% MONITOR
DS1237	16–Pin DIP	0 to 70	DS1237–x	x = 1 to 8
	16–Pin SOIC	0 to 70	DS1237S–x	x = 1 to 8
DS1238	16–Pin DIP	0 to 70	DS1238	10% MONITOR
	16–Pin DIP	0 to 70	DS1238–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1238N	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238S–5	5% MONITOR
DS1238A	16–Pin DIP	0 to 70	DS1238A	10% MONITOR
	16–Pin DIP	0 to 70	DS1238A–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1238AS	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238AS–5	5% MONITOR
DS1239	16–Pin DIP	0 to 70	DS1239	10% MONITOR
	16–Pin DIP	0 to 70	DS1239–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1239N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1239N–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1239S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1239S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN–5	5% MONITOR
DS1243Y	28–Pin Encap. DIP	0 to 70	DS1243Y	8K x 8 RAM; 200 ns
DS1244Y	28–Pin Encap. DIP	0 to 70	DS1244Y–000	32K x 8 RAM; 200 ns
	28–Pin Encap. DIP	0 to 70	DS1244Y–120	32K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1244Y–150	32K x 8 RAM; 150 ns
DS1245Y/AB	32–Pin Encap. DIP	0 to 70	DS1245AB–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1245AB–120–IND	120 ns
	32–Pin Encap. DIP	–40 to +85	DS1245AB–70–IND	70 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1245Y–120–IND	120 ns
	32–Pin Encap. DIP	–40 to +85	DS1245Y–70–IND	70 ns
DS1248Y	32–Pin Encap. DIP	0 to 70	DS1248Y–000	128K x 8 RAM; 200 ns
	32–Pin Encap. DIP	0 to 70	DS1248Y–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1248y–150	128K x 8 RAM; 150 ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1250		0 to +70	DS1250	
DS1258K	Kit	N/A	DS1258K–001	For CyberCard
	Kit	N/A	DS1258K–002	For CyberKey
DS1259	16–Pin DIP	0 to 70	DS1259	
	16–Pin DIP	–40 to +85	DS1259N	
	16–Pin SOIC	0 to 70	DS1259S	
	16–Pin SOIC	–40 to +85	DS1259SN	
DS1260		0 to 70	DS1260–25	250 mAHr
		0 to 70	DS1260–50	500 mAHr
		0 to 70	DS1260–100	1000 mAHr
DS1267	14–Pin DIP	0 to 70	DS1267–10	10K ohms
	14–Pin DIP	0 to 70	DS1267–50	50K ohms
	14–Pin DIP	0 to 70	DS1267–100	100K ohms
	14–Pin DIP	–40 to +85	DS1267N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1267N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1267N–100	100K ohms
	14–Pin SOIC	0 to 70	DS1267S–10	10K ohms
	14–Pin SOIC	0 to 70	DS1267S–50	50K ohms
	14–Pin SOIC	0 to 70	DS1267S–100	100K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–10	10K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–50	50K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1267E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1267E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1267E–100	100K ohms
DS1275	8–Pin DIP	0 to 70	DS1275	
	8–Pin SOIC	0 to 70	DS1275S	
DS1280	44–Pin Flat Pack	0 to 70	DS1280FP–44	
	80–Pin Flat Pack	0 to 70	DS1280FP–80	
DS1283	28–Pin DIP	0 to 70	DS1283	50 X 8 RAM
	28–Pin DIP	–40 to +85	DS1283N	50 x 8 RAM
	28–Pin SOIC	0 to 70	DS1283S	50 X 8 RAM
	28–Pin SOIC	–40 to +85	DS1283SN	50 x 8 RAM
DS1284	28–Pin DIP	0 to 70	DS1284	50 X 8 RAM
	28–Pin PLCC	0 to 70	DS1284Q	50 X 8 RAM
	28–Pin PLCC	–40 to +85	DS1284QN	50 X 8 RAM
DS1285	24–Pin DIP	0 to 70	DS1285	50 X 8 RAM
	24–Pin DIP	–40 to +85	DS1285N	50 x 8 RAM
	28–Pin PLCC	0 to 70	DS1285Q	50 X 8 RAM
	28–Pin PLCC	–40 to +85	DS1285QN	50 X 8 RAM
DS1286	28–Pin Encap. DIP	0 to 70	DS1286	50 X 8 RAM
DS1287	24–Pin Encap. DIP	0 to 70	DS1287	50 X 8 RAM
DS1287A	24–Pin Encap. DIP	0 to 70	DS1287A	50 X 8 RAM
DS129X	16–Pin Encap. DIP	0 to 70	DS1290	
	16–Pin DIP	0 to 70	DS1291	
	16–Pin DIP	–40 to +85	DS1291N	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	24–Pin Encap. DIP	0 to 70	DS1292	
	24–Pin DIP	0 to 70	DS1293	
	24–Pin DIP	–40 to +85	DS1293N	
DS1302	8–Pin DIP	0 to 70	DS1302	31 x 8 RAM
	8–Pin DIP	–40 to +85	DS1302N	31 x 8 RAM
	8–Pin SOIC	0 to 70	DS1302S	31 x 8 RAM
	8–Pin SOIC	–40 to +85	DS1302SN	31 x 8 RAM
	8–Pin SOIC (150 mils)	0 to 70	DS1302Z	31 x 8 RAM
	8–Pin SOIC (150 mils)	–40 to +85	DS1302ZN	31 x 8 RAM
DS1330Y/AB	34–Pin LPM	0 to 70	DS1330ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1330ABLPM–70	70 ns
	34–Pin LPM	0 to 70	DS1330YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1330YLPM–70	70 ns
DS1336	16–Pin DIP	0 to 70	DS1336	
	16–Pin DIP	–40 to +85	DS1336N	
	16–Pin SOIC	0 to 70	DS1336S	
	16–Pin SOIC	–40 to +85	DS1336SN	
DS1345Y/AB	34–Pin LPM	0 to 70	DS1345ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1345ABLPM–70	70 ns
	34–Pin LPM	0 to 70	DS1345YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1345YLPM–70	70 ns
DS1350Y/AB	34–Pin LPM	0 to 70	DS1350ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1350ABLPM–70	70 ns
	34–Pin LPM	0 to 70	DS1350YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1350YLPM–70	70 ns
DS1380	24–Pin DIP	0 to 70	DS1380	
	24–Pin SOIC	0 to 70	DS1380S	
DS1381	24–Pin Encap. DIP	0 to 70	DS1381	
DS1385	24–Pin DIP	0 to 70	DS1385	4K x 8 RAM
	28–Pin SOIC	0 to 70	DS1385S	4K x 8 RAM
DS1386	32–Pin Encap. DIP	0 to 70	DS1386–8–120	8K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1386–8–150	8K x 8 RAM; 150 ns
	32–Pin Encap. DIP	0 to 70	DS1386–32–120	32K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1386–32–150	32K x 8 RAM; 150 ns
DS1387	24–Pin Encap. DIP	0 to 70	DS1387	4K x 8 RAM
DS1395	28–Pin DIP	0 to 70	DS1395	4K x 8 RAM
	28–Pin SOIC	0 to 70	DS1395S	4K x 8 RAM
DS1397	28–Pin Encap. DIP	0 to 70	DS1397	4K x 8 RAM
DS1401			DS1401–xx	xx = 04 to 24, Nr. of Button ports
DS1402			DS1402RP4	RJ–11/Probe, 1.2m (4 feet)
			DS1402BB4	Two Buttons, 1.2m (4 feet)
			DS1402BP4	Button/Probe, 1.2m (4 feet)

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
			DS1402BR4	Button/RJ–11, 1.2m (4 feet)
DS1410	Button Holder/Parallel	0 to 70	DS1410	
DS1412	Button Holder/Serial	0 to 70	DS1412	
DS1414	Button Holder/Network	0 to 70	DS1414	
DS1420	F50	–40 to +85	DS1420L–F50	
DS1422	D50	–40 to +85	DS14220–F50	
DS1425	F50	–40 to +70	DS1425L–F50	
DS1427	F50	–40 to +70	DS1427L–F50	
DS1485	24–Pin DIP	0 to 70	DS1485	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1485S	8K x 8 RAM
DS1486	32–Pin Encap. DIP	0 to 70	DS1486–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1486–150	128K x 8 RAM; 150 ns
DS1488	24–Pin Encap. DIP	0 to 70	DS1488	8K x 8 RAM
DS1494	Touch Memory	–40 to +70	DS1494L–F5	F5 MicroCan
DS1495	28–Pin DIP	0 to 70	DS1495	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1495S	8K x 8 RAM
DS1497	28–Pin Encap. DIP	0 to 70	DS1497	8K x 8 RAM
DS1585	28–Pin DIP	0 to 70	DS1585	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1585S	8K x 8 RAM
DS1587	28–Pin Encap. DIP	0 to 70	DS1587	8K x 8 RAM
	34–Pin Encap. LPM	0 to 70	DS1587L	8K x 8 RAM
DS1589	28–Pin DIP	0 to 70	DS1589	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1589S	8K x 8 RAM
DS1593	28–Pin Encap. DIP	0 to 70	DS1593	8K x 8 RAM
DS1602	8–Pin DIP	0 to 70	DS1602	
	8–Pin SOIC	0 to 70	DS1602S	
DS1603	7–Pin Encap. SIP	0 to 70	DS1603	
DS1609	24–Pin DIP	–40 to +85	DS1609	
	24–Pin SOIC	–40 to +85	DS1609S	
DS1610	16–Pin DIP	0 to 70	DS1610	
	16–Pin DIP	–40 to +85	DS1610N	
	16–Pin SOIC	0 to 70	DS1610S	
	16–Pin SOIC	–40 to +85	DS1610SN	
DS1611	16–Pin DIP	0 to 70	DS1611	
	16–Pin DIP	–40 to +85	DS1611N	
	16–Pin SOIC	0 to 70	DS1611S	
	16–Pin SOIC	–40 to +85	DS1611SN	
	20–Pin TSSOP	0 to 70	DS1611E	
	20–Pin TSSOP	–40 to +85	DS1611EN	
DS1612	16–Pin DIP	0 to 70	DS1612	
	16–Pin DIP	–40 to +85	DS1612N	
	16–Pin SOIC	0 to 70	DS1612S	
	16–Pin SOIC	–40 to +85	DS1612SN	
	20–Pin TSSOP	0 to 70	DS1612E	
	20–Pin TSSOP	–40 to +85	DS1612EN	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1613C	Socket	0 to 70	DS1613C	
DS1613D	Socket	0 to 70	DS1613D	
DS1620	8–Pin DIP	–55 to +125	DS1620	
	8–Pin SOIC	–55 to +125	DS1620S	
DS1630Y/AB	28–Pin Encap. DIP	0 to 70	DS1630AB–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1630AB–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1630ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1630ABLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1630ABLPM–70–IND	70 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1630Y–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1630YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1630YLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1630YLPM–70–IND	70 ns
DS1632	16–Pin DIP	0 to 70	DS1632	
	16–Pin DIP	–40 to +85	DS1632N	
	16–Pin SOIC	0 to 70	DS1632S	
	16–Pin SOIC	–40 to +85	DS1632SN	
DS1633	3–Pin TO–220	–40 to +85	DS1633XX	See data sheet for complete specifications.
DS1640	16–Pin DIP	0 to 70	DS1640	
	16–Pin DIP	–40 to +85	DS1640N	
	16–Pin SOIC	0 to 70	DS1640S	
	16–Pin SOIC	–40 to +85	DS1640SN	
	16–Pin DIP	0 to 70	DS1640C	Consumer Grade
	16–Pin SOIC	0 to 70	DS1640SC	Consumer Grade
DS1642	24–Pin Encap. DIP	0 to 70	DS1642–120	2K x 8 RAM; 120 ns
	24–Pin Encap. DIP	0 to 70	DS1642–150	2K x 8 RAM; 150 ns
DS1643	28–Pin Encap. DIP	0 to 70	DS1643–120	8K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1643–150	8K x 8 RAM; 150 ns
	26–Pin Encap. LPM	0 to 70	DS1643L–120	8K x 8 RAM; 120 ns
	26–Pin Encap. LPM	0 to 70	DS1643L–150	8K x 8 RAM; 150 ns
DS1644	28–Pin Encap. DIP	0 to 70	DS1644–120	32K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1644–150	32K x 8 RAM; 150 ns
	34–Pin Encap. LPM	0 to 70	DS1644L–120	32K x 8 RAM; 120 ns
	34–Pin Encap. LPM	0 to 70	DS1644L–150	32K x 8 RAM; 150 ns
DS1645Y/AB	32–Pin Encap. DIP	0 to 70	DS1645AB–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–70	70 ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	32–Pin Encap. DIP	–40 to +85	DS1645AB–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1645ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1645ABLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1645ABLPM–70–IND	70 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645Y–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1645YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1645YLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1645YLPM–70–IND	70 ns
DS1645EE	32–Pin Encap. DIP	0 to 70	DS1645EE–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1645EE–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1645EE–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645EE–70–IND	70 ns
DS1646	32–Pin Encap. DIP	0 to 70	DS1646–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1646–150	128K x 8 RAM; 150 ns
	34–Pin Encap. LPM	0 to 70	DS1646L–120	128K x 8 RAM; 120 ns
	34–Pin Encap. LPM	0 to 70	DS1646L–150	128K x 8 RAM; 150 ns
DS1650Y/AB	32–Pin Encap. DIP	0 to 70	DS1650AB–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1650AB–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1650AB–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1650AB–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1650ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1650ABLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1650ABLPM–70–IND	70 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1650Y–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1650YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1650YLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1650YLPM–70–IND	70 ns
DS1651	8–Pin DIP	–25 to +85	DS1651	
	8–Pin SOIC	–25 to +85	DS1651S	
DS1652	8–Pin DIP	–25 to +85	DS1652	
	8–Pin SOIC	–25 to +85	DS1652S	
DS1653	16–Pin DIP	–25 to +85	DS1653	
	16–Pin SOIC	–25 to +85	DS1653S	
DS1658Y/AB	40–Pin Encap. DIP	0 to 70	DS1658AB–100	100 ns
	40–Pin Encap. DIP	0 to 70	DS1658AB–70	70 ns
	40–Pin Encap. DIP	–40 to +85	DS1658AB–70–IND	70 ns
	40–Pin Encap. DIP	0 to 70	DS1658Y–100	100 ns
	40–Pin Encap. DIP	0 to 70	DS1658Y–70	70 ns
	40–Pin Encap. DIP	–40 to +85	DS1658Y–70–IND	70 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1666	14–Pin DIP	0 to 70	DS1666–10	10K ohms
	14–Pin DIP	0 to 70	DS1666–50	50K ohms
	14–Pin DIP	0 to 70	DS1666–100	100K ohms
	14–Pin DIP	–40 to +85	DS1666N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1666N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1666N–100	100K ohms
	16–Pin SOIC	0 to 70	DS1666S–10	10K ohms
	16–Pin SOIC	0 to 70	DS1666S–50	50K ohms
	16–Pin SOIC	0 to 70	DS1666S–100	100K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–10	10K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–50	50K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–100	100K ohms
DS1667	20–Pin DIP	0 to 70	DS1667–10	10K ohms
	20–Pin DIP	0 to 70	DS1667–50	50K ohms
	20–Pin DIP	0 to 70	DS1667–100	100K ohms
	20–Pin DIP	–40 to +85	DS1667N–10	10K ohms
	20–Pin DIP	–40 to +85	DS1667N–50	50K ohms
	20–Pin DIP	–40 to +85	DS1667N–100	100K ohms
	20–Pin SOIC	0 to 70	DS1667S–10	10K ohms
	20–Pin SOIC	0 to 70	DS1667S–50	50K ohms
	20–Pin SOIC	0 to 70	DS1667S–100	100K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–10	10K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–50	50K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–100	100K ohms
DS1668	6–Pin Pushbutton	0 to 70	DS1668–10	10K ohms
	6–Pin Pushbutton	0 to 70	DS1668–50	50K ohms
	6–Pin Pushbutton	0 to 70	DS1668–100	100K ohms
DS1669	8–Pin DIP	0 to 70	DS1669–10	10K ohms
	8–Pin DIP	0 to 70	DS1669–50	50K ohms
	8–Pin DIP	0 to 70	DS1669–100	100K ohms
	8–Pin DIP	–40 to +85	DS1669N–10	10K ohms
	8–Pin DIP	–40 to +85	DS1669N–50	50K ohms
	8–Pin DIP	–40 to +85	DS1669N–100	100K ohms
	8–Pin SOIC	0 to 70	DS1669S–10	10K ohms
	8–Pin SOIC	0 to 70	DS1669S–50	50K ohms
	8–Pin SOIC	0 to 70	DS1669S–100	100K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–10	10K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–50	50K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–100	100K ohms
DS1689	28–Pin DIP	0 to 70	DS1689	114 x 8 RAM
	28–Pin SOIC	0 to 70	DS1689S	114 x 8 RAM
DS1693	28–Pin Encap. DIP	0 to 70	DS1693	114 x 8 RAM
DS1710	16–Pin DIP	0 to 70	DS1710	
	16–Pin DIP	–40 to +85	DS1710N	
	16–Pin SOIC	0 to 70	DS1710S	
	16–Pin SOIC	–40 to +85	DS1710SN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	20–Pin TSSOP	0 to 70	DS1710E	
	20–Pin TSSOP	–40 to +85	DS1710EN	
DS1730Y	32–Pin Encap. DIP	0 to 70	DS1730Y–200	200 ns
	32–Pin Encap. DIP	0 to 70	DS1730Y–150	150 ns
	32–Pin Encap. DIP	–40 to +85	DS1730Y–150–IND	150 ns
	34–Pin LPM	0 to 70	DS1730YLPM–200	200 ns
	34–Pin LPM	0 to 70	DS1730YLPM–150	150 ns
	34–Pin LPM	–40 to +85	DS1730YLPM–150–IND	150 ns
DS1745Y	32–Pin Encap. DIP	0 to 70	DS1745Y–200	200 ns
	32–Pin Encap. DIP	0 to 70	DS1745Y–150	150 ns
	32–Pin Encap. DIP	–40 to +85	DS1745Y–150–IND	150 ns
	34–Pin LPM	0 to 70	DS1745YLPM–200	200 ns
	34–Pin LPM	0 to 70	DS1745YLPM–150	150 ns
	34–Pin LPM	–40 to +85	DS1745YLPM–150–IND	150 ns
DS1750Y	32–Pin Encap. DIP	0 to 70	DS1750Y–200	200 ns
	32–Pin Encap. DIP	0 to 70	DS1750Y–150	150 ns
	32–Pin Encap. DIP	–40 to +85	DS1750Y–150–IND	150 ns
	34–Pin LPM	0 to 70	DS1750YLPM–200	200 ns
	34–Pin LPM	0 to 70	DS1750YLPM–150	150 ns
	34–Pin LPM	–40 to +85	DS1750YLPM–150–IND	150 ns
DS1758Y/AB	40–Pin Encap. DIP	0 to 70	DS1758Y–200	200 ns
	40–Pin Encap. DIP	0 to 70	DS1758Y–150	150 ns
	40–Pin Encap. DIP	–40 to +85	DS1758Y–150–IND	150 ns
DS1802	20–Pin DIP	0 to 70	DS1802	50K ohms
	20–Pin SOIC	0 to 70	DS1802S	50K ohms
	20–Pin TSSOP	0 to 70	DS1802E	50K ohms
DS1820	PR–35	–55 to +125	DS1820	
	8–Pin SOIC	–55 to +125	DS1820S	
DS1821	PR–35	–55 to +125	DS1821	
	8–Pin SOIC	–55 to +125	DS1821S	
	TO–220	–55 to +125	DS1821T	
DS1833	TO–92	–40 to +85	DS1833–5	5% MONITOR
	TO–92	–40 to +85	DS1833–10	10% MONITOR
	TO–92	–40 to +85	DS1833–15	15% MONITOR
	SOT–223	–40 to +85	DS1833Z–5	5% MONITOR
	SOT–223	–40 to +85	DS1833Z–10	10% MONITOR
	SOT–223	–40 to +85	DS1833Z–15	15% MONITOR
DS1837	TO–220	0 to 70	DS1837	
	D–PAK	0 to 70	DS1837S	
DS1867	14–Pin DIP	0 to 70	DS1867–10	10K ohms
	14–Pin DIP	0 to 70	DS1867–50	50K ohms
	14–Pin DIP	0 to 70	DS1867–100	100K ohms
	16–Pin SOIC	0 to 70	DS1867S–10	10K ohms
	16–Pin SOIC	0 to 70	DS1867S–50	50K ohms
	16–Pin SOIC	0 to 70	DS1867S–100	100K ohms

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	20–Pin TSSOP	0 to 70	DS1867E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1867E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1867E–100	100K ohms
DS1868	14–Pin DIP	0 to 70	DS1868–10	10K ohms
	14–Pin DIP	0 to 70	DS1868–50	50K ohms
	14–Pin DIP	0 to 70	DS1868–100	100K ohms
	16–Pin DIP	0 to 70	DS1868S–10	10K ohms
	16–Pin DIP	0 to 70	DS1868S–50	50K ohms
	16–Pin DIP	0 to 70	DS1868S–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1868E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1868E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1868E–100	100K ohms
DS1869	8–Pin DIP	0 to 70	DS1869–10	10K ohms
	8–Pin DIP	0 to 70	DS1869–50	50K ohms
	8–Pin DIP	0 to 70	DS1869–100	100K ohms
	8–Pin SOIC	0 to 70	DS1869S–10	10K ohms
	8–Pin SOIC	0 to 70	DS1869S–50	50K ohms
	8–Pin SOIC	0 to 70	DS1869S–100	100K ohms
DS12885	24–Pin DIP	0 to 70	DS12885	114 X 8 RAM
	24–Pin SOIC	0 to 70	DS12885S	114 x 8 RAM
	28–Pin PLCC	0 to 70	DS12885Q	114 X 8 RAM
	28–Pin PLCC	–40 to +85	DS12885QN	114 x 8 RAM
	32–Pin TQFP	0 to 70	DS12885T	114 x 8 RAM
DS12887	24–Pin Encap. DIP	0 to 70	DS12887	114 X 8 RAM
DS12887A	24–Pin Encap. DIP	0 to 70	DS12887A	114 X 8 RAM
DS1920	Touch Memory	–55 to +100	DS1920–F3	F3 MicroCan
	Touch Memory	–55 to +100	DS1920–F5	F5 MicroCan
DS1982	Touch Memory	–40 to +85	DS1982–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1982–F5	F5 MicroCan
DS1985	Touch Memory	–40 to +85	DS1985–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1985–F5	F5 MicroCan
DS1986	Touch Memory	–40 to +85	DS1986–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1986–F5	F5 MicroCan
DS1990A	Touch Memory	–40 to +85	DS1990A–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1990A–F5	F5 MicroCan
DS1991	Touch Memory	–40 to +70	DS1991L–F5	F5 MicroCan
DS1992	Touch Memory	–40 to +70	DS1992L–F5	F5 MicroCan
DS1993	Touch Memory	–40 to +70	DS1993L–F5	F5 MicroCan
DS1994	Touch Memory	–40 to +70	DS1994L–F5	F5 MicroCan
DS1995	Touch Memory	–40 to +70	DS1995L–F5	F5 MicroCan
DS1996	Touch Memory	–40 to +70	DS1996L–F5	F5 MicroCan
DS2009	28–Pin DIP (600 MIL)	0 to 70	DS2009–35	35 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–120	120 ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin DIP (600 MIL)	–40 to +85	DS2009N–35	35 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2009N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–35	35 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–35	35 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2009R–35	35 ns
	32–Pin PLCC	0 to 70	DS2009R–50	50 ns
	32–Pin PLCC	0 to 70	DS2009R–65	65 ns
	32–Pin PLCC	0 to 70	DS2009R–80	80 ns
	32–Pin PLCC	0 to 70	DS2009R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2009RN–35	35 ns
	32–Pin PLCC	–40 to +85	DS2009RN–50	50 ns
DS2010	28–Pin DIP (600 MIL)	0 to 70	DS2010–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2010R–50	50 ns
	32–Pin PLCC	0 to 70	DS2010R–65	65 ns
	32–Pin PLCC	0 to 70	DS2010R–80	80 ns
	32–Pin PLCC	0 to 70	DS2010R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2010RN–50	50 ns
DS2011	28–Pin DIP (600 MIL)	0 to 70	DS2011–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2011R–50	50 ns
	32–Pin PLCC	0 to 70	DS2011R–65	65 ns
	32–Pin PLCC	0 to 70	DS2011R–80	80 ns
	32–Pin PLCC	0 to 70	DS2011R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2011RN–50	50 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2012	28–Pin DIP (600 MIL)	0 to 70	DS2012–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N–50	50 ns
	32–Pin PLCC	0 to 70	DS2012R–50	50 ns
	32–Pin PLCC	0 to 70	DS2012R–65	65 ns
	32–Pin PLCC	0 to 70	DS2012R–80	80 ns
	32–Pin PLCC	0 to 70	DS2012R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2012RN–50	50 ns
DS2013	28–Pin DIP (600 MIL)	0 to 70	DS2013–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N–50	50 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–50	50 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–65	65 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–80	80 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–120	120 ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN–50	50 ns
DS2016	24–Pin DIP	–40 to +85	DS2016	
	24–Pin SOIC	–40 to +85	DS2016S	
DS2064	28–Pin DIP	–40 to +85	DS2064	
	28–Pin SOIC	–40 to +85	DS2064S	
DS2223	TO–92	–40 to +85	DS2223	
	SOT–223	–40 to +85	DS2223Z	
DS2224	TO–92	–40 to +85	DS2224	
	SOT–223	–40 to +85	DS2224Z	
DS2227	STIK	0 to 70	DS2227–120	120 ns
	STIK	0 to 70	DS2227–100	100 ns
	STIK	0 to 70	DS2227–70	70 ns
DS2229	STIK	0 to 70	DS2229–85	85 ns
DS22B57	28–Pin DIP	–40 to +85	DS22B57	
	28–Pin SOIC	–40 to +85	DS22B57S	
DS2401	TO–92	–40 to +85	DS2401	
	SOT–223	–40 to +85	DS2401Z	
	6–Lead TSOC	–40 to +85	DS2401P	
DS2404	16–Pin DIP	0 to 70	DS2404	512 x 8 RAM
	16–Pin SOIC	0 to 70	DS2404S	512 x 8 RAM
	16–Pin SSOP	0 to 70	DS2404B	512 x 8 RAM
DS2404S–C01	16–Pin SOIC	–40 to +85	DS2404S–C01	Custom 001/Dual Port
DS2405	TO–92	–40 to +85	DS2405	
	SOT–223	–40 to +85	DS2405Z	
	6–Lead TSOC	–40 to +85	DS2405P	
DS2430	TO–92	0 to 70	DS2430	
	TO–92	–40 to +85	DS2430N	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin SOIC	0 to 70	DS2430Z	
	8–Pin SOIC	–40 to +85	DS2430ZN	
	20–Pin TSSOP	0 to 70	DS2430E	
	20–Pin TSSOP	–40 to +85	DS2430EN	
DS2434	PR–35	–40 to +85	DS2434	
DS2435	PR–35	–40 to +85	DS2435	
DS2502	TO–92	–40 to +85	DS2502	
	8–Pin SOIC	–40 to +85	DS2502S	
	6–Lead TSOC	–40 to +85	DS2502P	
DS2505	TO–92	–40 to +85	DS2505	
	6–Lead TSOC	–40 to +85	DS2505P	
DS2506	PR–35	–40 to +85	DS2506	
DS620X		0 to 70	DS6200	
		0 to 70	DS6201	
		0 to 70	DS6204U	Generic Code #1
		0 to 70	DS6207	Generic Code #1
DS6417		0 to 70	DS6417–001	1 Megabit Density
		0 to 70	DS6417–002	2 Megabit Density
		0 to 70	DS6417–004	4 Megabit Density
		0 to 70	DS6417–256	256K–bit Density
		0 to 70	DS6417–512	512K–bit Density2
		0 to 70	DS6417P–001	1 Megabit Density
		0 to 70	DS6417P–002	2 Megabit Density
		0 to 70	DS6417P–004	4 Megabit Density
		0 to 70	DS6417P–256	256K–bit Density
		0 to 70	DS6417P–512	512K–bit Density
DS9000			DS9000	
DS9002			DS9002	
DS9003			DS9003	
DS9005			DS9005	
DS9006			DS9006	
DS908x			DS9080V	Cyber Key Flushmount–Vertical
			DS9080A	Cyber Key Flushmount–Angled
			DS9081V	Cyber Key Recessed–Vertical
			DS9081A	Cyber Key Recessed–Angled
			DS9082V	Cyber Card Flushmount–Vertical
			DS9082A	Cyber Card Flushmount–Angled
			DS9084V	Cyber Card EV Recessed–Vertical, Beige

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
			DS9084V–001	Cyber Card EV Recessed–Vertical, Black
			DS9084A	Cyber Card EV Recessed–Angled, Beige
			DS9084A–001	Cyber Card EV Recessed–Angled, Black
			DS9085A–001	Cyber Card, Cyber Key
			DS9085V–001	Cyber Card, Cyber Key
DS9092			DS9092	Panel–mount Probe
			DS9092T	Panel–mount Probe with Tactile Pin
			DS9092GT	Hand–Grip with Tactile Pin
DS9092K	Kit		DS9092K	
DS9092R	tabbed MicroCan		DS9092R–000	Standard
	tabbed MicroCan		DS9092R–L00	with Logo
DS9093			DS9093F	Snap–in Fob
			DS9093P	Perm. Mount, One Screw
			DS9093S	Perm. Mount, Two Screws
			DS9093RA	Lock Ring
			DS9093RB	Flange Enlargement
DS9094			DS9094F	Thru–Hole Mount, F5
			DS9094FS	Surface Mount, F5
DS9096P			DS9096P	Permanent Bond
DS9097			DS9097	Standard
			DS9097E	Enhanced for EPROM
DS9098			DS9098	Retainer for F5 MicroCan
			DS9098T	Tube Packaging
DS9099	Kit		DS9099K	Dev. Kit with Software
			DS9099	Chip Set Only
DS9100			DS9100A	Touch & Hold, Outer Part
			DS9100B	Touch & Hold, Center Part
DS9101			DS9101	Standard Clip
			DS9101S	Snap Fastener Version
DS9102K	Kit		DS9102K	
DS9103K	Kit		DS9103K	

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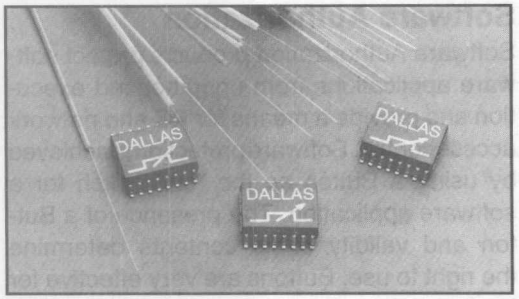
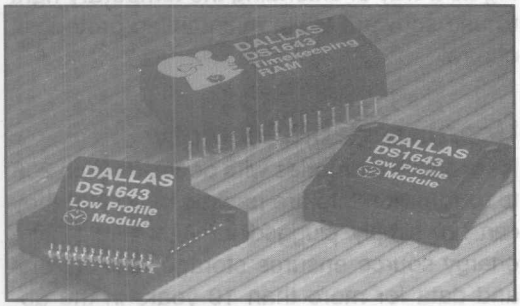


Silicon Timed Circuits

Silicon Timed Circuits (often referred to as delay lines) are chips that make subtle adjustments to the timing of high-performance electronics so that they will perform optimally. Because of the precision that lasers provide, some Silicon Timed Circuits can make timing adjustments down to a fraction of a nanosecond, which is the time it takes light to travel about a foot. For more information, call our Timing Problem Hotline at (214) 450-5348.

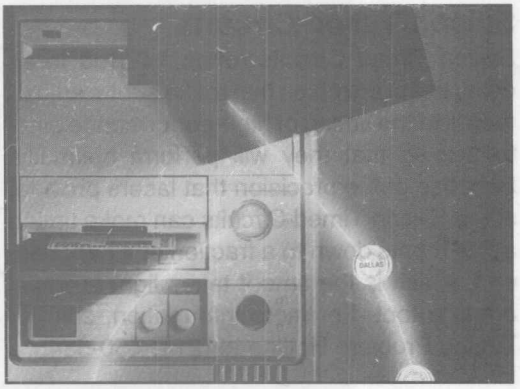


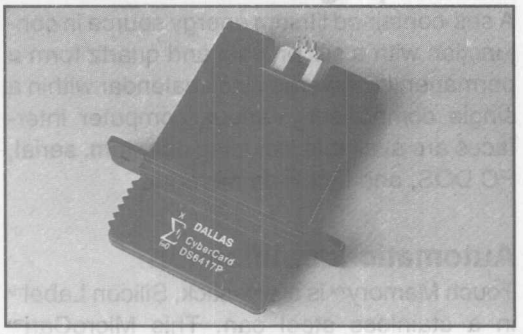
Timekeeping

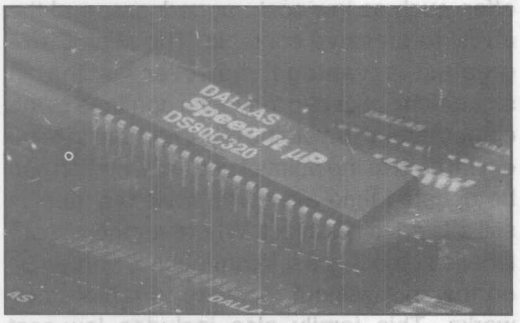
A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, serial, PC DOS, and bytewide memory.

Automatic Identification

Touch Memory™ is a self-stick, Silicon Label™ in a stainless steel can. This MicroCan™ provides all the advantages canning has to offer, such as low cost, ruggedness, and the ability to preserve contents. The MicroCan's greatest advantage, however, is that a standalone chip can leave the confines of the computer and travel virtually anywhere to bring digital data to the point of use. Information can be updated time after time while the label is still affixed to its object. Wherever the silicon-labelled object goes, information is served up on the spot without recourse to remote networks. This family also includes low-cost memory chips in T0-92 packages.







Software Authorization

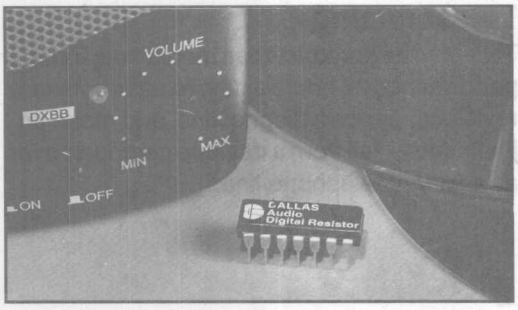
Software Authorization products protect software applications from unauthorized execution and provide a means for PC and network access control. Software protection is achieved by using a Button as the "on" switch for a software application. The presence of a Button and validity of its contents determine the right to use. Buttons are very effective for implementing time- or count-based metering as a way of extending the temporary right to use software while maintaining protection control.

User-Insertable Memory

Nonvolatile memories with densities from 256 to four million bits are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. Applications for such products include portable data carrier, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling workrecords. All products can be read or written by a PC.

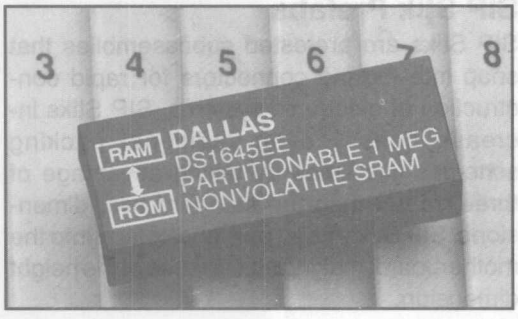
Microcontrollers

The DS80C320 High-Speed Micro is an 8051 family device that offers the highest performance in the industry for an 8-bit microcontroller. Pin- and instruction set-compatible with the standard 80C32, the High-Speed Micro uses only 4 clocks per instruction, as compared with 12 on other 8051's. Our DS500x Soft Micros convert industry-standard bytewide SRAM into high-performance, nonvolatile read/write storage.



System Extension

These products add a variety of special features to systems without encumbering design. A digital potentiometer is an all-silicon version of an electrical element used in almost all electronic equipment. Whereas mechanical pots are usually brought up to the surface of the equipment and adjusted with a dial, digital pots can be set remotely while they are in a system. CPU supervisors monitor vital conditions for a microprocessor.

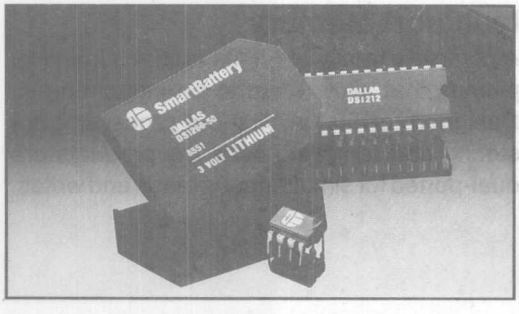


Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for more than 10 years in the absence of main power. When power goes out of tolerance, the built-in lithium energy source automatically switches on and write protection guards data from garbling during power loss.

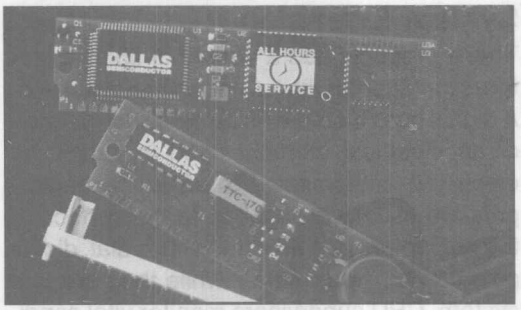
Telecommunications

A comprehensive product family addresses the requirements of high-speed, digital voice/data transmission and monitoring in T1, CEPT, or Primary Rate ISDN networks. ADPCM processors double or quadruple the capacity of voice communication channels through DSP compression techniques.



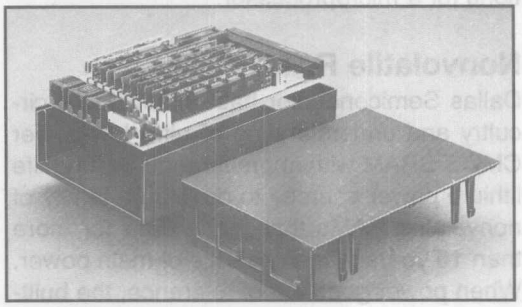
Battery Backup & Chargers

The Battery Backup chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred. Battery Chargers contain all the circuitry needed to recharge a 3-cell NiCad or lithium battery pack in a 3-pin package.



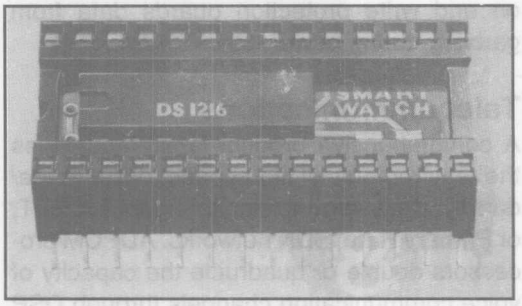
Teleservicing

Teleservicing products can monitor equipment performance 24 hours a day, release software revisions, perform diagnostics, and make adjustments — all from a desktop computer over an ordinary telephone line.



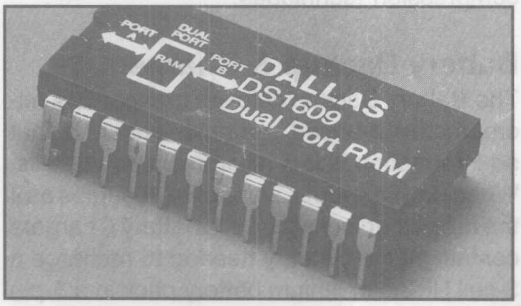
SIP Stik Prefabs

SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.



Intelligent Sockets

Intelligent Sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.



Multiport Memory

A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out processing for storing and retrieving data, the products are dual-ported for simultaneous reads and writes.

Dallas Semiconductor Corporation designs, manufactures, and markets electronic chips and chip-based subsystems. Founded in 1984, the Company uses customer problems as an entry point to develop products with widespread applications. The Company is committed to new product development as a means to increase future revenues and to diversify its markets, products, and customers.

Advanced technologies have given the Company a competitive edge over traditional approaches to semiconductors. Combining lithium energy cells with low-power CMOS chips powers chips for the useful life of the equipment. Direct laser writing enhances chip capabilities with high levels of precision and unique identities.

In its 10-year history, Dallas Semiconductor has developed 190 base products with over 1,000 variations shipped to more than 8,000 customers worldwide. A direct sales force and distribution network sell to original equipment manufacturers (OEMs) in personal computers and workstations, scientific and medical equipment, industrial controls, automatic identification, telecommunications, consumer electronics, and other markets.

Sales for 1993 totaled $156,860,000. Dallas Semiconductor has 748 employees. On March 19, 1990, the Company started trading on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions—dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon is made possible by lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

As of January 7, 1994, the Company owns 309,000 square feet of building space and 22.9 acres of land in Dallas. The Company's wafer fabrication facility is a model of efficiency and is capable of producing all of its requirements. An expansion of that facility will begin production in mid-1994. When fully equipped, this facility will more than double the Company's fabrication capacity and make available the latest technology, permitting the design of circuits with geometries as small as 0.5 microns.

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL–STD–105.
- *In–Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- *In–Process Sample Tests:* In order to guarantee the accuracy and completeness of in–process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL–STD–105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state–of–the–art environmental facility allows accelerated stresses to be performed and monitored in–house. In addition, a metallurgical laboratory has been equipped to perform real-time x–ray, x–ray florescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer–based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production–ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- *Prototype or Engineering Sample:* Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- *Prequal:* Prequal products meet prototype requirements and are characterized to all data sheet limits. Final test and all processes used to manufacture the product are stable and under manufacturing control. Qualification of the product has started.
- *Fully Qualified:* Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

Tables 1, 2 and 3 list the tests which a Dallas Semiconductor product must pass in order to be classified as fully qualified.

RELIABILITY MONITOR PROGRAM

In order to maintain continuous qualification status on all products, Dallas Semiconductor has implemented an extensive Reliability Monitor Program (RMP). The RMP monitors all design, wafer fabrication, and assembly processes in the qualified products database. Product is selected monthly from finished goods and subjected to a series of reliability tests similar to those used in the original qualification. Any failures generated from these tests require analysis to root cause and corrective action.

Data from the RMP is published quarterly and is available on demand.

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUIT PRODUCTS Table 1

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
High Temperature Operating Life	125°C, 5.5V	1000 Hr.	*0.4%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	*0.4%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	1.0%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	–55°C to +125°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Bond Pull	MIL–STD–883 Method 2011	Premold	1.5%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%
ESD	MIL–STD–883 Method 3015		> ±1000 volts
Latch–up	JEDEC Std. 17		> 100 mW/pin

* Combined high voltage life and operating life requirement.

FULL QUALIFICATION REQUIREMENTS FOR MODULE PRODUCTS Table 2

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Temperature Storage	85°C, No Bias	1000 Hr.	2.0%
*Temperature Humidity Bias	85°C/85% RH, 5.5V	959 Hr.	1.0%
Temperature Cycle	–40°C to +85°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%

* Selected products.

FULL QUALIFICATION REQUIREMENTS FOR SIPSTICK AND TOUCH MEMORY PRODUCTS Table 3

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
High Temperature Storage	85°C, No Bias	1000 Hr.	7.0%
Temperature Humidity	60°C/90% RH	288 Hr.	7.0%
Temperature Cycle	–40°C to +85°C	500 cycle	7.0%

AUTOMATIC IDENTIFICATION

Although human–readable labels have been used for ages, it was the advent of computer–readable labels that quickly revolutionized the way grocery stores operate and made possible the overnight delivery of packages. When error–prone — and time consuming — key entry was replaced by bar codes, it became convenient to build large databases to help in making accurate and timely decisions.

In the next step in the evolution of labelling technology, ink–on–paper bar codes are surpassed by silicon media. With Dallas Semiconductor's automatic identification technology, a chip becomes the label that can serve as a standalone data base. Attached to an object or carried by a person, the chip identifies and carries relevant information available instantly with little or no human intervention. People access secure areas with convenience, health care professionals accurately create records, and workers efficiently track items as they travel along the assembly line.

Three distinct limitations of bar codes are overcome by chips:

- They hold significantly more information.
- Information on the chip can be changed; chips can be updated via computer while affixed to their object.
- Cost of access points, that is the communication with computers, is drastically lower because of direct, chip–to–chip digital data transfers.

LABELLING WITH SILICON

The concept of labelling is simple. Information accompanies an object to supply on–the–spot data to whomever needs it. Computer–readable labels offer even greater value because of the speed and accuracy with which information can be read. However, the need to keep information current on the labels in a dynamic process begs for a more powerful medium than paper labels, which must be removed, re–printed, and replaced in order to be updated. Just as word processing has revolutionized the writing process by facilitating editing and subsequent communication, silicon will change the role of labels in the design of a modern data collection system. Chip–based labels become instant sources of digital information that is directly associated with the escorted object.

In order to put memory chips into smaller, less costly, and more durable packages, Dallas Semiconductor has reduced the number of wires required for a chip to communicate with another chip. Whereas most chips require eight or more connections for two–way communications, a minimalist design of one conductor plus ground was devised to expand silicon's role into the realm of labelling.

The chip–based labels are available in two very different forms. Packaged in small stainless steel "MicroCANs", they are called Touch Memories. The same silicon parts put into transistor packages or surface–mount packages are generally called solder–mount products.

It's About the Size of a Dime

MICROCANS

The lowest cost method of making a chip into a computer–readable label is to reduce its many minute conductors to just one and extend it to a larger easy–to–contact point. The simplest arrangement is a single data conductor plus a ground contact. In this way, a two–piece stainless steel container called a MicroCan™ serves both as protective housing and electrical contacts: lid (data) and rim (ground). Its circular shape guides a simple, cup–shaped probe over its rounded surfaces even if struck with significant misalignment. The 16 mm button shape serves all Touch Memories.

While Touch Memories share some of the characteristics of bar codes, these chip–based data carriers have many advantages over ink–on–paper technology:

- Touch Memories can be read without expensive electro–optical equipment.
- Touch Memories can hold up to 1600 times the data of bar codes, with larger capacities in development.
- Each Touch Memory proves its identity by its unique registration number.

- The registration number of a Touch Memory acts as node address to access the device as part of an unlimited network.
- The contents of the chip data carriers can be changed while attached to an object.
- Touch Memories accommodate over one million changes.
- A clam–shell, steel container called a MicroCan is better suited to harsh operating environments.
- Hand–held equipment can be made smaller, lighter, and less expensive since virtually no energy is needed to read or write.

All communication with Touch Memories is reduced to a single signal plus ground. Long and short pulses encode the binary 1's and 0's. Because Touch Memories are digital circuits, they talk directly to other chips in a computer, resulting in minimal cost interface using one CMOS/TTL logic signal. A reader/writer for Touch Memories can be implemented with just one spare I/O line of a microcomputer, often a free resource in a system. The signalling rate of Touch Memory was chosen so that a computer's serial port (UART) operating at 115.2k bits per second (bps) can supply the timing by sending a bit for a byte (115.2 divided by 8 is 14.4k bps).

ATTACHMENT METHODS

Silicon chips haven't been able to attach to anything except printed circuit boards. Touch Memory, by contrast, can be attached to just about anything. A fundamental bond is established between an object and its digital data.

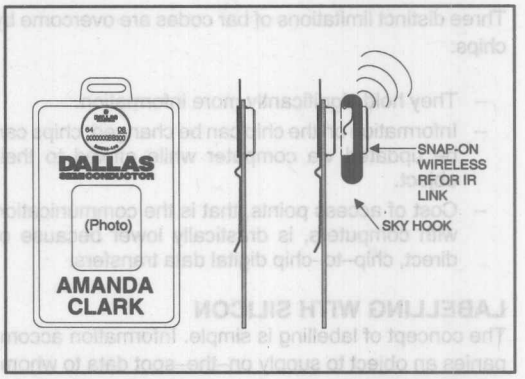
IDENTIFICATION BY TOUCH

A memory chip enclosed in a button–shaped, stainless steel package called MicroCan™ provides all the advantages canning has to offer such as low cost, ruggedness, and the ability to preserve contents. But perhaps the MicroCan's greatest advantage is that a standalone chip can leave the confines of the computer and travel virtually anywhere to bring digital data to the point of use.

In addition to protecting the silicon chip, the MicroCan is the touch point for electrical contact, a placard for the human–readable engravings, and a fastener for attaching the enclosed chip to an object. The attachment methods include pressure–sensitive adhesive, press–fit, grooved clip, etc.

Data is transferred between this stick–on memory chip and a computer with a quick electrical contact to the case. Using electrical conductivity, data flows to and from the enclosed memory chip through the lid of the can using its rim as the ground return.

Once mounted, the MicroCan can accept a snap–on fastener that sustains the electrical contact for communication. This communication link can be wired or a wireless Skyhook™ if the snap–on incorporates a radio or IR transceiver.



A Skyhook snaps on the Touch Memory Button to communicate by proximity.

The 16mm diameter of the MicroCan provides sufficient area for much larger silicon chips than are currently supplied – one million bits and beyond. Other considerations for the MicroCan design included handling and the ergonomics of touching. The 16mm size is slightly smaller than the minimum coin size, the lock core face on door knobs, and the 19mm button spacing of IBM AT computer keyboards.

An optimum system design will rely on one or more of the following advantages of Silicon Labels™:

- **High capacity**: Printer's ink is no match for the density of a microchip.
- **Re–usable**: Change the data, not the label; Touch Memory can be recycled over and over again.
- **Durable**: Chips are encased in stainless steel.
- **Legible**: Information is written in digital form, making "print quality" absolute; every read is totally tested for data integrity.
- **Low Cost of Access**: Readers consist of inexpensive metallic conductors rather than more complicated, power–consuming equipment. Those same metal contacts are also writers; no printers are required. A Silicon Label communicates directly with the other silicon chips inside equipment.
- **Mounting Options**: Touch Memory can be affixed with its self–stick adhesive backing, latched by its flange, or locked with a ring pressed on to its rim.
- **Action at a Distance**: Read or write > 100 meters away by simple extension of conductive surfaces.
- **Selectivity**: Data files are pinpointed with an on–chip directory, then randomly accessed.
- **Group Access**: Multiple Touch Memories sharing the same conductive surfaces are individually addressed even though they form a group. Location is precisely determined by the specificity of the contact surface.
- **Traceable**: Each Silicon Label™ has a passively readable, never–duplicated registration number. This number is engraved on the steel MicroCan as well as on the silicon chip inside.
- **Authenticity**: The permanent registration number is impractical to counterfeit and guaranteed to be unique.
- **Digital Continuum**: Stores any symbology, including ASCII, for hardware– and software–independence.

Data is stored in Touch Memories using a file structure very similar to floppy disks. This file structure uses packetized data and scratchpad verification prior to writing so that Touch Memories can operate with data integrity even when electrical contact is intermittent and highly resistive. A sector of a floppy roughly corresponds to a page of Touch Memory. A directory on each chip tells what packetized files are stored, where each file is located, and how many pages each file occupies. In this way, CRC–checked information can be randomly accessed for quick response.

An extension of the conductive surfaces can be arranged so that the Touch Memory need not be "touched" directly. Instead, an extended surface contacting the MicroCan can be touched with a reader/writer for wider alignment tolerances, often with little or no worker involvement.

READY FOR NETWORKING

Silicon labels are inherently network–ready for digital communications. They can be written as easily as they can be read, and they have the lowest access point cost of any computer–readable media. Touch Memories transport digital data in two ways: 1) as the objects to which they are attached move, and 2) by accepting and distributing data to computers and their networks. The sources of information can always be pin pointed because of the globally unique address (registration number) is permanently lasered in each silicon chip.

Each Touch Memory has a built–in network controller so that many devices can be grouped on a single master 1–Wire bus to form what is called a MicroLAN. This further reduces the cost of an access point by supporting clusters of Touch Memories with a single 1–wire bus for point to multi–point communication.

The user need not worry about conflicting node addresses in a multi–point environment because the unique lasered registration number is used to specify the node. The contact range between the master and individual Touch Memory can reach out 300 meters using twisted pair cable commonly used for telephones (30pF/m, 24 gauge).

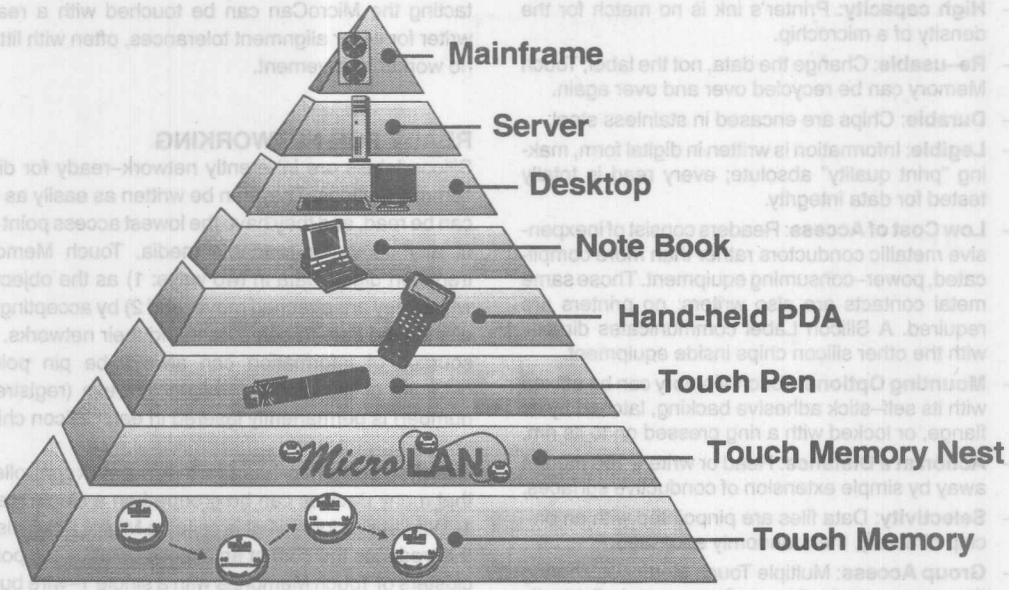
Wherever the silicon–labeled object goes, information is served up on the spot without recourse to remote networks. Objects that carry digital data form a multipoint communication system – a subnetwork– that moves information to every point of activity and feeds computer networks.

BOOK OF DS19XX STANDARDS

Dallas Semiconductor has published a set of standards that allows Touch Memory to operate with all hardware and software platforms. An implementation of this standard, Touch Memory EXecutive™ (TMEX), is included with the DS0620 upgrade to the DS9092K Touch Memory Starter Kit for MicroSoft Windows™ based PCs.

SILICON FOOD CHAIN

Chip to chip to chip . . .



MOVING BEYOND PAPER

Writing on paper developed as an extension of the human memory. In much the same way, Touch Memory extends the computer's memory. But the similarities between paper and silicon don't stop there. Just as paper accepts the characters of any language, Touch Memory can store any computer symbologies, including ASCII characters. Forms were invented to give structure to data so that information can be communicated efficiently. With Touch Memory, data is structured, in conjunction with software, using on–chip directories and files in a manner similar to floppy disks. Like self–stick notes, whose popularity derives from the fact that they attach with ease, Touch Memory is available with adhesive backing. However, there are many other mounting options to allow Touch Memory to attach to metal, plastic, fabric – virtually anything.

The silicon chip with sub–micron photolithography packs many orders of magnitude more information in a given area than ink on paper. Once written, paper is difficult to re–use. Touch Memory can be updated on demand and used over and over again. Paper is a burden because it requires human intervention to do virtually anything with it. Touch Memory, by contrast, is read with no transcription errors and has packetized digital data that is computer network–ready.

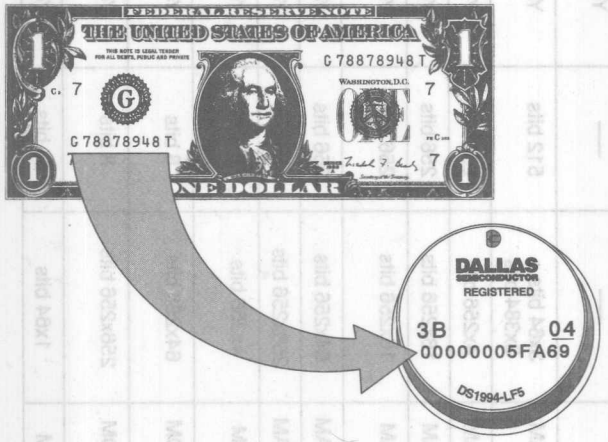
Data is rarely created – it's most often copied or re–arranged and combined with other information. Take for example your name, birth date, and social security number. They are created once and you copy them throughout your life. Or consider the constant need for photocopying machines that never create data, only copy it. With Touch Memory, the functionality of the copying machine is built into the silicon medium. Making copies of copies eventually makes paper unreadable. Silicon contrasts with paper media in that the millionth copy is as good as the original because of digital recording. If copying is undesirable, lock bits, add–only memory, passwords and encryption can be employed.

Paper forms are often numbered to insure completeness and to reference in the future. Touch Memory has a permanent registration number engraved into each chip. The registration number is a credential that authenticates its membership in the registry of the sourcing company. In this way, Touch Memory can be

tracked and non–registered numbers can be excluded from a particular application.

Finally, paperwork plays an important role in bridging islands of automation, carrying instructions and records about objects to which they are attached. Labels are forward messengers to the next system. Silicon Labels extend the reach of computing by forming digital conduits between isolated computer networks.

EVERY TOUCH MEMORY IS REGISTERED



THE MAKING OF UNIQUENESS

Each chip with MicroLAN interface is permanently engraved with a laser prior to canning. Dallas Semiconductor's procedure for lasering chips is tightly controlled so that the unalterable registration number is guaranteed to be unique. By selectively removing 3–micron polysilicon links with a very precise laser beam, a digital number is etched using the binary pattern of the open or closed links. The links are then sealed with a protective layer of glass so that any tampering attempts would be evident.

The never–duplicated registration number is in a passively–powered portion of the chip. This Read Only Memory (ROM) has its power supplied from the 1–Wire signalling and is not affected by power conditions in the rest of the chip. The chip's number is also engraved on the lid of the stainless MicroCan as a human–readable marking. Even if the electrical circuit were inoperative and the package marking was not legible, the registration number could be recovered directly from the chip under high magnification.

The uniqueness and absolute traceability of the number results from the technology employed and special procedures. First, a link that's open can't be reformed, and any attempt to open a link would require breaking the protective layer of glass. Strict internal controls include special access control to the room where the chips are lasered, software that regulates the process, and a Cyclic Redundancy Check (CRC) that verifies numbers have been assigned correctly. Attempts to modify the registration number will cause the CRC to become incorrect, providing additional evidence of tampering. And finally, the large 10^{17} number pool assures an ample supply of codes.

In systems, the unique number serves as a reference number just like a license plate number, phone number, network node address, serial number, or social security number. Other applications benefit by using the never–duplicated number to seed an encryption algorithm to protect the other memory on the chip from unauthorized decryption.

AUTOMATIC IDENTIFICATION PRODUCTS

TOUCH FAMILY

Part	Description	Registration #	Memory	Organization	Scratchpad	MicroLAN	Family Code
DS1990A F3/F5	Touch Serial Number	8+48+8 bits ROM	—	—	—	Yes	01H
DS1991L F5	Touch MultiKey, 3 secure partitions	8+48+8 bits ROM	1,344 bits NV RAM	3x64 bits + 3x384 bits	512 bits	Yes	02H
DS1992L F5	Touch Memory	8+48+8 bits ROM	1,024 bits NV RAM	4x256 bits	256 bits	Yes	08H
DS1993L F5	Touch Memory	8+48+8 bits ROM	4,096 bits NV RAM	16x256 bits	256 bits	Yes	06H
DS1994L F5	Touch Memory Plus Time	8+48+8 bits ROM	4,096 bits NV RAM	16x256 bits	256 bits	Yes	04H
DS1995L F5	Touch Memory	8+48+8 bits ROM	16,384 bits NV RAM	64x256 bits	256 bits	Yes	0AH
DS1996L F5	Touch Memory	8+48+8 bits ROM	65,536 bits NV RAM	256x256 bits	256 bits	Yes	0CH
DS1982 F3/F5	Add–Only Touch Memory	8+48+8 bits ROM	1,024 bits EPROM	4x256 bits	8 bits	Yes	09H
DS1985 F3/F5	Add–Only Touch Memory	8+48+8 bits ROM	16,384 bits EPROM	64x256 bits	8 bits	Yes	0BH
DS1986 F3/F5	Add–Only Touch Memory	8+48+8 bits ROM	65,536 bits EPROM	256x256 bits	8 bits	Yes	0FH
DS1920 F3/F5	Touch Thermometer	8+48+8 bits ROM	16 bits EEPROM	1x64 bits	64 bits	Yes	10H

AUTOMATIC IDENTIFICATION PRODUCTS

SOLDER MOUNT PRODUCTS

Part	Description	Registration #	Memory	Organization	Scratchpad	MicroLAN	Family Code
DS2401	Silicon Serial Number	8+48+8 bits ROM	—	—	—	Yes	01H
DS2502	Add–Only Memory	8+48+8 bits ROM	1,024 bits EPROM	4x256 bits	8 bits	Yes	09H
DS2505	Add–Only Memory	8+48+8 bits ROM	16,384 bits EPROM	64x256 bits	8 bits	Yes	0BH
DS2506	Add–Only Memory	8+48+8 bits ROM	65,536 bits EPROM	256x256 bits	8 bits	Yes	0FH
DS2405	Addressable Switch	8+48+8 bits ROM	—	—	—	Yes	05H
DS2404S–C01	Dual–Port Memory Plus Time	8+48+8 bits ROM	4,096 bits RAM	16x256 bits	256 bits	Yes	84H
DS2223	EconoRAM	—	256 bits RAM	1x256 bits	—	—	N/A
DS2224	EconoRAM Plus ROM	32 bits ROM	224 bits RAM	1x256 bits	—	—	N/A

ACCESSORIES FOR TOUCH MEMORY APPLICATIONS

Part	Category	Description
DS9093F	mount	Snap–In fob for flanged MicroCan
DS9093P	mount	Permanent mount for F5 MicroCan, 1 screw
DS9093S	mount	Permanent mount for F5 MicroCan, 2 screws
DS9093RA	mount	Lock Ring
DS9093RB	mount	Flange Enlargement
DS9096P	mount	Adhesive Pad
DS9101	mount	Multi–Purpose Clip
DS1401	link	Font Panel Button Holder
DS1402BB	link	Button to Button Cord
DS1402BP	link	Button to Cup Coiled Cord
DS1402BR	link	Button to RJ–11 Cord
DS1402RP	link	RJ–11 to Cup Coiled Cord
DS9092	link	Panel–Mount Probe
DS9092GT	link	Hand–Grip Probe with tactile feedback
DS9092R–000	link	Touch Port, tabbed MicroCan
DS9092R–L00	link	Touch Port, tabbed MicroCan with logo
DS9092T	link	Panel–Mount Probe with tactile feedback
DS9094F	link	Clip for F5 MicroCan, Through–Hole Solder Mount
DS9094FS	link	Clip for F5 MicroCan for Surface Solder Mount
DS9098	link	MicroCan Retainer for Surface Solder Mount
DS9100A	link	Touch and Hold Probe Stampings, Ground Contact
DS9100B	link	Touch and Hold Probe Stampings, Data Contact
DS9097	interface	Touch COM Port Adapter
DS9097E	interface	Touch COM Port Adapter, EPROM Upgraded Version
DS0620	kit	TMEX Professional Software Developer's Upgrade of DS9092K
DS9092K	kit	Touch Memory Starter Kit
DS9099	kit	Touch Pen Chip Set
DS9099K	kit	Touch Pen Prototype Development Kit
DS9102K	kit	Touch Memory Electronic Lock Demo Kit
DS9103K	kit	Touch Memory Access Control Demo Kit

DS1990A
Touch Serial Number

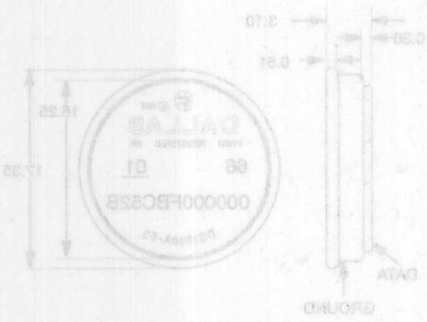
DS1990A SPECIAL FEATURES

- Upgrade of DS1990 allows multiple Touch Serial Numbers to reside on a common bus
- Unique 48–bit serial number
- Low–cost electronic key for access control
- 8–bit CRC for checking data integrity
- Can be read in less than 5 ms
- Operating temperature range of –40°C to +85°C

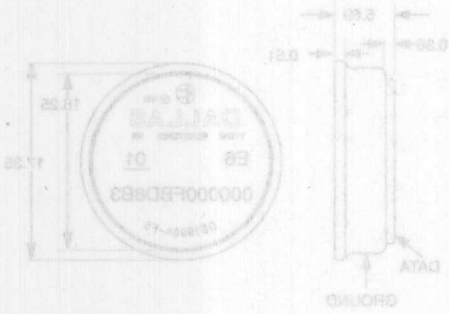
COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tested) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to an object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Ed.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D locations

F3 MICROCAN™



F5 MICROCAN™



All dimensions shown in millimeters

ORDERING INFORMATION

DS1990A–F3	F3 MicroCan
DS1990A–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9092P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

DALLAS SEMICONDUCTOR

DS1990A
Touch Serial Number

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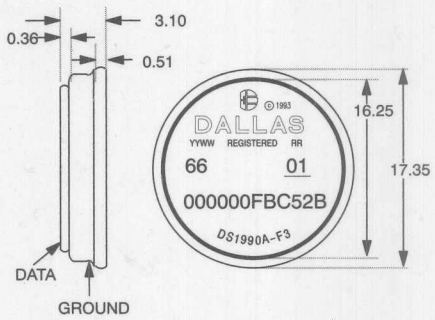
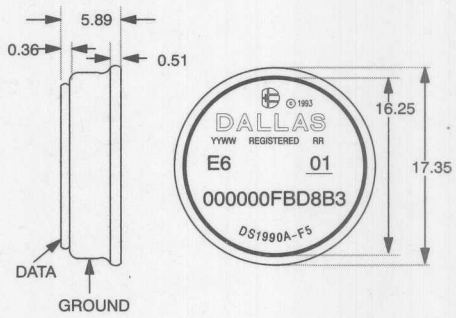
- Digital identification by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to an object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D locations

F3 MICROCAN™



F5 MICROCAN™



All dimensions shown in millimeters

ORDERING INFORMATION

DS1990A–F3	F3 MicroCan
DS1990A–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1990A Touch Memory Button™ is a rugged data carrier that acts as an electronic registration number for automatic identification. The DS1990A consists of a factory–lasered, 64–bit ROM that includes a unique 48–bit serial number, an 8–bit CRC and an 8–bit Family Code (01h). Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return. The DS1990A is fully compatible with the DS1990 Touch Serial Number but provides the additional 1–Wire protocol capability that allows the Search ROM command to be interpreted by the DS1990A and therefore allows multiple DS1990A devices to reside on a single data line.

The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture and shock. Its compact coin–shaped profile is self–aligning with mating receptacles, allowing the DS1990A to be used easily by human operators. Accessories permit the DS1990A to be mounted on plastic key tabs, photo ID badges, printed circuit boards or any smooth surface of an object. Applications include access control, work–in–progress tracking, tool management and inventory control.

OPERATION

The DS1990A's internal ROM is accessed via a single data line. The 48–bit serial number, 8–bit family code and 8–bit CRC are retrieved using the Dallas 1–Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

1–WIRE BUS SYSTEM

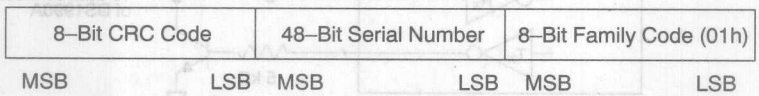
The 1–Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS1990A is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal type and timing). For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

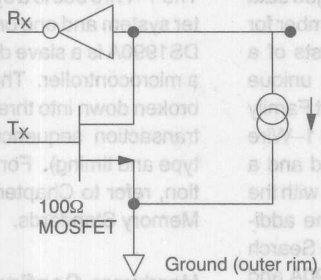
The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS1990A is an open drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second.

The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 μs, one or more of the devices on the bus may be reset.

DS1990A MEMORY MAP Figure 1

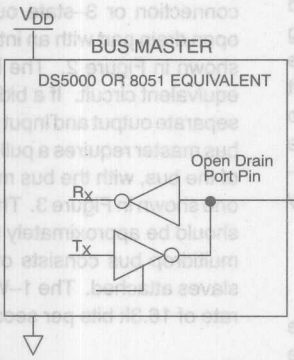


DS1990A EQUIVALENT CIRCUIT Figure 2

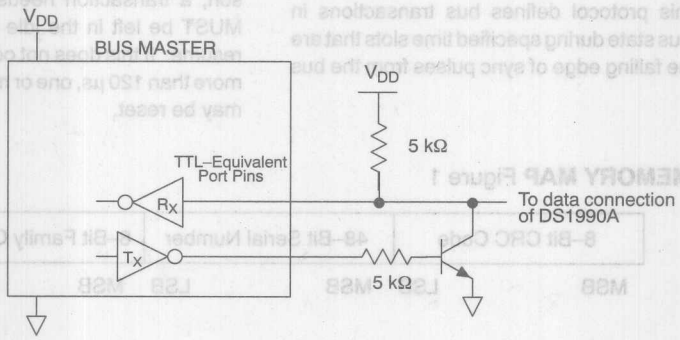


BUS MASTER CIRCUIT Figure 3

A) Open Drain



B) Standard TTL



TRANSACTION SEQUENCE

The sequence for accessing the DS1990A via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1990A is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 4):

Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS1990A's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1990A on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The DS1990A Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS1990, which will only respond to a 0Fh command word with its 64–bit ROM data.

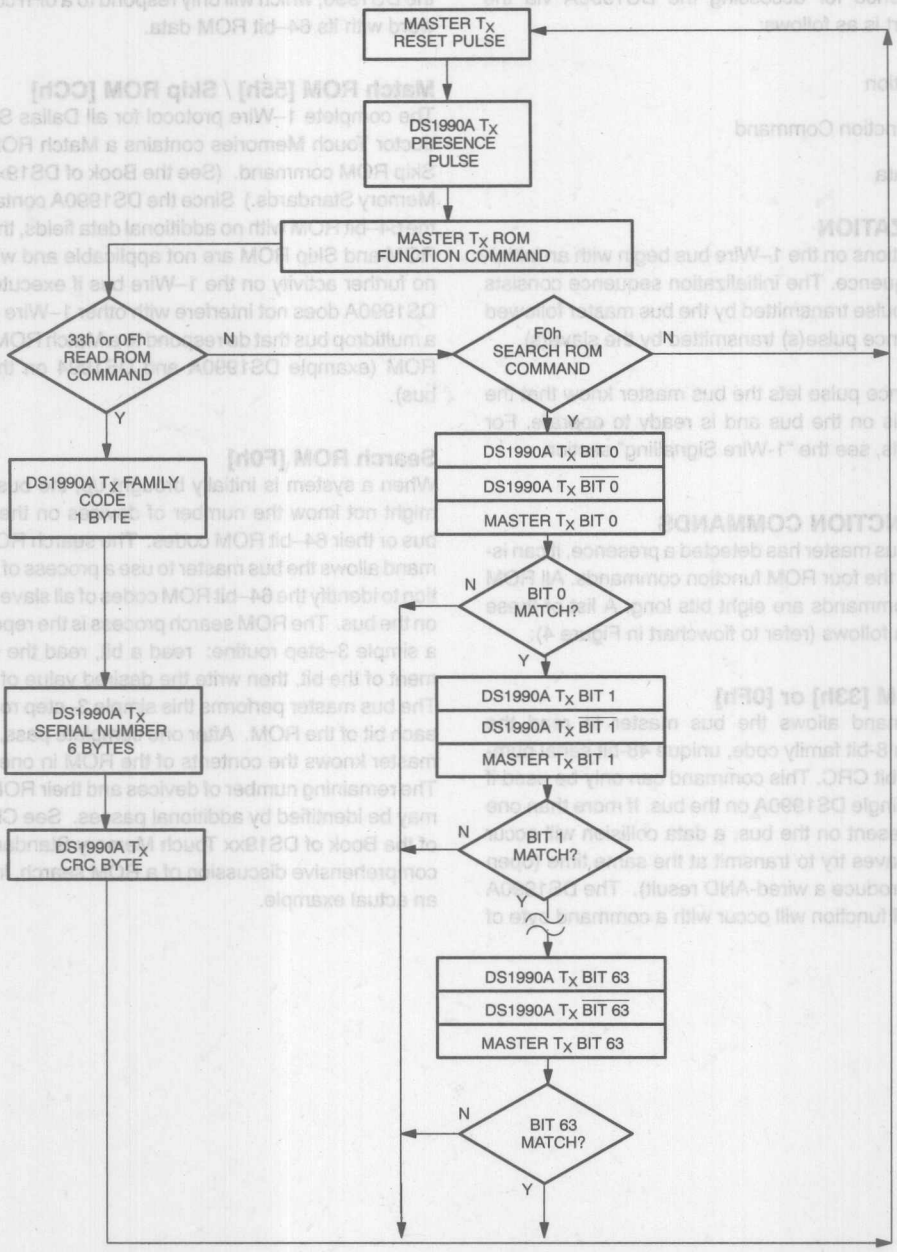
Match ROM [55h] / Skip ROM [CCh]

The complete 1–Wire protocol for all Dallas Semiconductor Touch Memories contains a Match ROM and a Skip ROM command. (See the Book of DS19xx Touch Memory Standards.) Since the DS1990A contains only the 64–bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1–Wire bus if executed. The DS1990A does not interfere with other 1–Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (example DS1990A and DS1994 on the same bus).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM search, including an actual example.

ROM FUNCTIONS FLOW CHART Figure 4



1–WIRE SIGNALLING

The DS1990A requires strict protocols to insure data integrity. The protocol consists of four types of signalling on one line: Reset sequence with Reset Pulse and Presence Pulse, write 0, write 1 and read data. All these signals except presence pulse are initiated by the bus master.

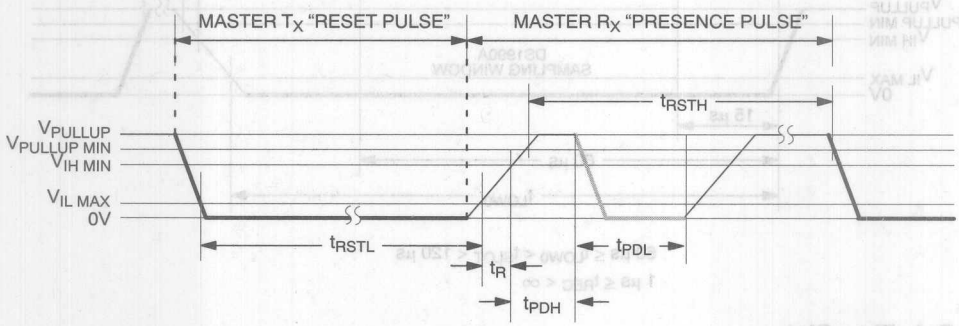
The initialization sequence required to begin any communication with the DS1990A is shown in Figure 5. A Reset Pulse followed by a Presence Pulse indicates the DS1990A is ready to send or receive data given the correct ROM command.

The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1–Wire bus is pulled to a high state via the 5 kΩ pull-up resistor. After detecting the rising edge on the data contact, the DS1990A waits (t_{PDH}, 15-60 µs) and then transmits the presence pulse (t_{PDL}, 60-240 µs).

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1990A to the master by triggering a delay circuit in the DS1990A. During write time slots, the delay circuit determines when the DS1990A will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1990A will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

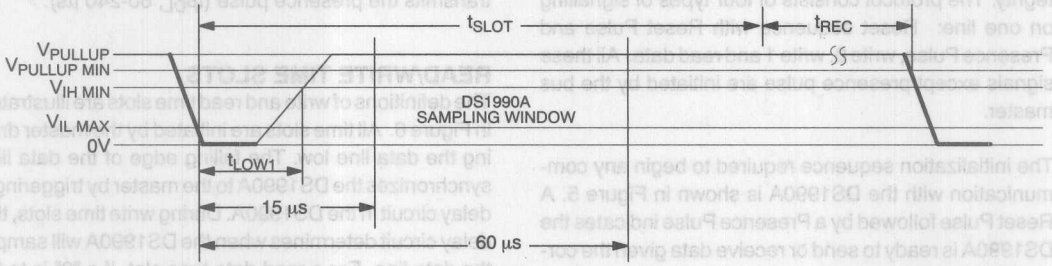
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



* In order not to mask interrupt signalling by other devices on the 1–Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

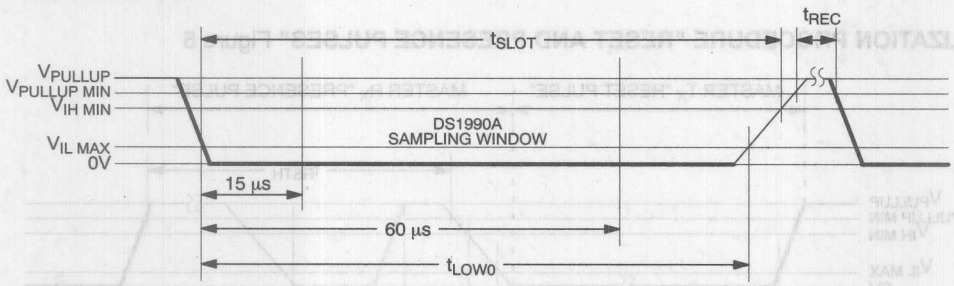
READ/WRITE TIMING DIAGRAM Figure 6

Write–One Time Slot



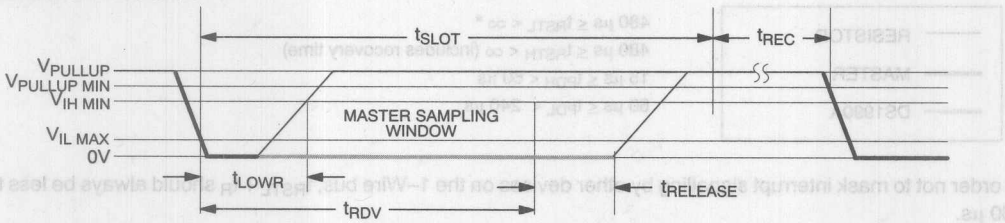
60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

Write–Zero Time Slot



60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs
1 µs ≤ t_{REC} < ∞

Read–Data Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOWR} < 15 µs
0 ≤ $t_{RELEASE}$ < 45 µs
1 µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs

CRC ASSEMBLY LANGUAGE PROCEDURE Table 1

```
DO_CRC:     PUSH    ACC         ; save the accumulator
            PUSH    B           ; save the B register
            PUSH    ACC         ; save bits to be shifted
            MOV     B,#8        ; set shift=8bits
            ;
CRC_LOOP:   XRL     A,CRC       ; calculate CRC
            RRC     A           ; move it to the carry
            MOV     A,CRC       ; get the last CRC value
            JNC     ZERO        ; skip if data=0
            XRL     A,#18H      ; update the CRC value
            ;
ZERO:       RRC     A           ; position the new CRC
            MOV     CRC,A       ; store the new CRC
            POP     ACC         ; get the remaining bits
            RR      A           ; position the next bit
            PUSH    ACC         ; save the remaining bits
            DJNZ    B,CRC_LOOP  ; repeat for eight bits
            POP     ACC         ; clean up the stack
            POP     B           ; restore the B register
            POP     ACC         ; restore the accumulator
            RET
```

CRC GENERATION

To validate the data transmitted from the DS1990A, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1990A. The bus master computes the CRC over the 8–bit family code and all 48 ID number data bits, but *not* over the stored CRC value itself. If the two CRC values match, the transmission is error–free.

An example of how to generate the CRC using assembly language software is shown in Table 1. This assembly language code is written for the DS5000 Soft microcontroller which is compatible with the 8031/51 Microcontroller family. The procedure DO_CRC calculates the cumulative CRC of all the bytes passed to it in the accumulator. It should be noted that the variable CRC needs to be initialized to 0 before the procedure is executed. Each byte of the data is then placed in the accumulator and DO–CRC is called to update the CRC variable. After all the data has been passed to DO_CRC, the variable CRC will contain the result. The equivalent polynomial function of this software routine is:

$$CRC = x^8 + x^5 + x^4 + 1$$

For more details, see the Book of DS19xx Touch Memory Standards.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	9

AC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	10
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the I/O line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signalling, otherwise, it could mask or conceal interrupt pulses if this device is used in parallel with a DS1994.

DALLAS SEMICONDUCTOR

DS1991
Touch MultiKey

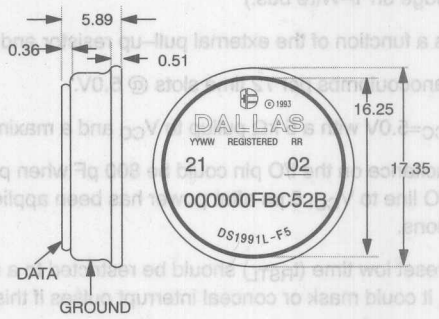
SPECIAL FEATURES

- 1,152–bit secure read/write, nonvolatile memory
- Secure memory cannot be deciphered without matching 64–bit password
- Memory is partitioned into 3 blocks of 384 bits each
- 64–bit password and ID fields for each memory block
- 512–bit scratchpad ensures data transfer integrity
- Operating temperature range: –40°C to +70°C
- Over 10 years of data retention

COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations

F5 MICROCAN™



All dimensions shown in millimeters

ORDERING INFORMATION

DS1991L–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1991 Touch Memory Button™ is a rugged read/write data carrier that acts as three separate electronic keys, offering 1,152 bits of secure, nonvolatile memory. Each key is 384 bits long with distinct 64–bit password and public ID fields (Figure 1). The password field must be matched in order to access the secure memory. Data is transferred serially via the 1–Wire protocol, which requires only a single data lead and a ground return. The 512–bit scratchpad serves to ensure integrity of data transfers to secure memory. Data should first be written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the secure memory. This process insures data integrity when modifying the memory. A 48–bit serial number is factory lasered into each DS1991 to provide a guaranteed unique identity which allows for absolute traceability. The family code for the DS1991 is 02h. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture and shock. Its compact button–shaped profile is self–aligning with mating receptacles, allowing the DS1991 to be easily used by human operators. Accessories permit the DS1991 to be mounted on plastic key fobs, photo–ID badges, printed–circuit boards or any smooth surface of an object. Applications include secure access control, debit tokens, work–in–progress tracking, electronic travelers and proprietary data.

OPERATION

The DS1991 is accessed via a single data line using the 1–Wire protocol. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 9. After a ROM Function Command is successfully executed, the memory functions that operate on the secure memory and the scratchpad become accessible and the bus master may issue any one of the six Memory Function Commands specific to the DS1991. The protocol for these Memory Function Commands is described in Figure 5. All data is read and written least significant bit first.

64–BIT LASERED ROM

Each DS1991 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (Figure 2.)

The 1–Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards.

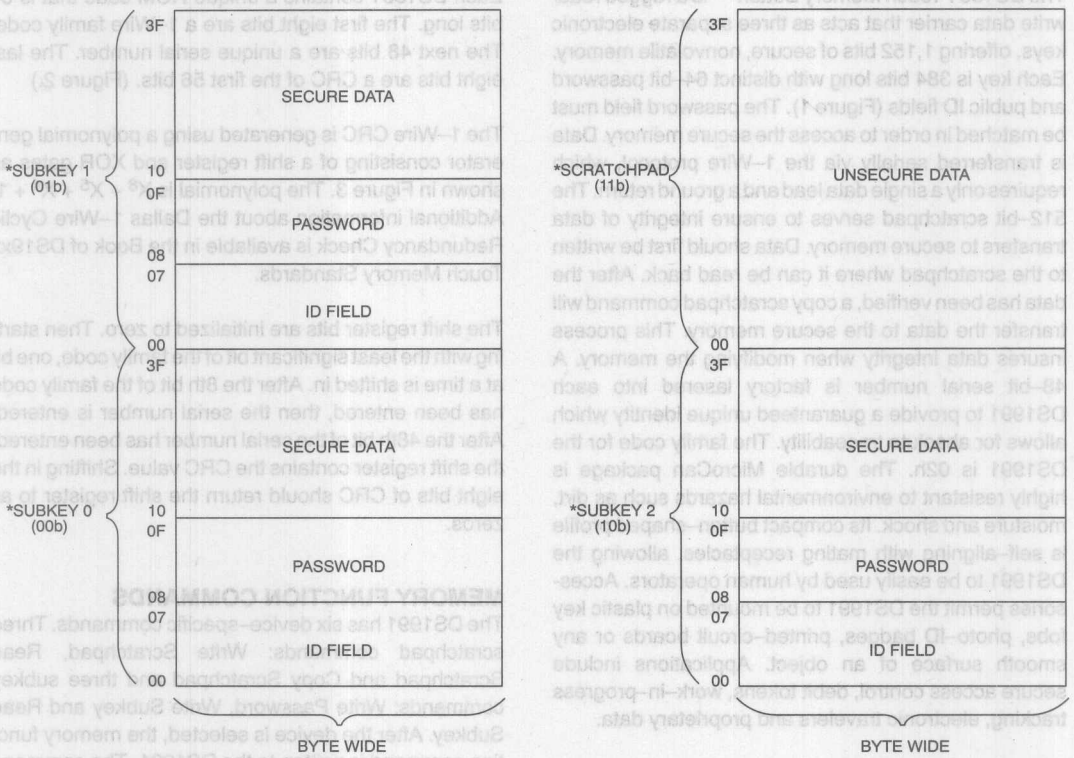
The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

MEMORY FUNCTION COMMANDS

The DS1991 has six device–specific commands. Three scratchpad commands: Write Scratchpad, Read Scratchpad and Copy Scratchpad and three subkey commands: Write Password, Write Subkey and Read Subkey. After the device is selected, the memory function command is written to the DS1991. The command is comprised of three fields, each one byte long. The first byte is the function code field. This field defines the six commands that can be executed. The second byte is the address field. The first six bits of this field define the starting address of the command. The last two bits of this field are the subkey address code. The third byte of the command is a complement of the second byte (Figure 4).

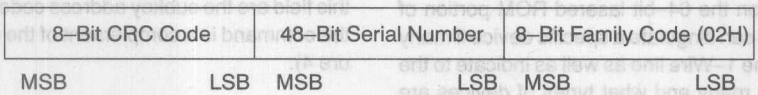
For the first use, since the passwords actually stored in the device are unknown, the DS1991 needs to be initialized. This is done by directly writing (i. e., not through the scratchpad) the new identifier and password for the selected subkey using the Write Password command. As soon as the new identifier and password are stored in the device, further updates should be done through the scratchpad.

MEMORY MAP Figure 1

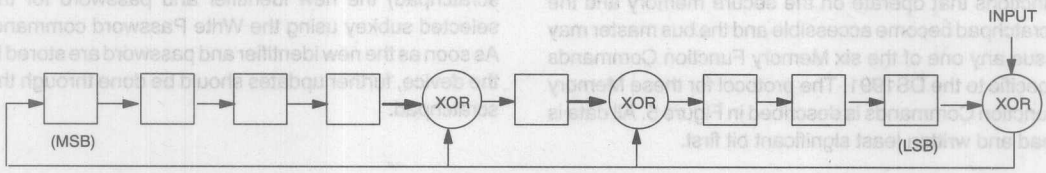


* Each subkey or the scratchpad has its own unique address.

64–BIT LASERED ROM Figure 2



1-WIRE CRC GENERATOR Figure 3



DS1991 COMMAND STRUCTURE Figure 4

Command	1st byte	2nd byte							3rd byte
		B7	B6	B5	B4	B3	B2	B1	B0	
write scratchpad	96H	1	1	any value						ones complement of 2nd byte
read scratchpad	69H			00H to 3FH						
copy scratchpad	3CH	Sub–Key Nr.: 0 0 or 0 1 or 1 0		0	0	0	0	0	0	
read SubKey	66H			any value						
write SubKey	99H			10H to 3FH						
write password	5AH			0	0	0	0	0	0	

SCRATCHPAD COMMANDS

The 64–byte read/write scratchpad of the DS1991 is not password–protected. Its normal use is to build up a data structure to be verified and then copied to a secure subkey.

Write Scratchpad [96H]

The Write Scratchpad command is used to enter data into the scratchpad. The starting address for the write sequence is specified in the command. Data can be continuously written until the end of the scratchpad is reached or until the DS1991 is reset. The command sequence is shown in Figure 5, first page, left column.

Read Scratchpad [69H]

The Read Scratchpad command is used to retrieve data from the scratchpad. The starting address is specified in the command word. Data can be continuously read until the end of the scratchpad is reached or until the DS1991 is reset. The command sequence is shown in Figure 5, first page, center column.

Copy Scratchpad [3CH]

The Copy Scratchpad command is used to transfer specified data blocks from the scratchpad to a selected subkey. This command should be used when data verification is required before storage in a secure subkey. Data can be transferred in single 8–byte blocks or in one large 64–byte block. There are nine valid block selector codes that are used to specify which block is to be transferred (Figure 6). As a further precaution against accidental erasure of secure data, the 8–byte password of the destination subkey must be entered. If the password does not match, the operation is terminated. After the block of data is transferred to the secure subkey, the original data in the corresponding block of the scratchpad is erased. The command sequence is shown in Figure 5, first page, right column.

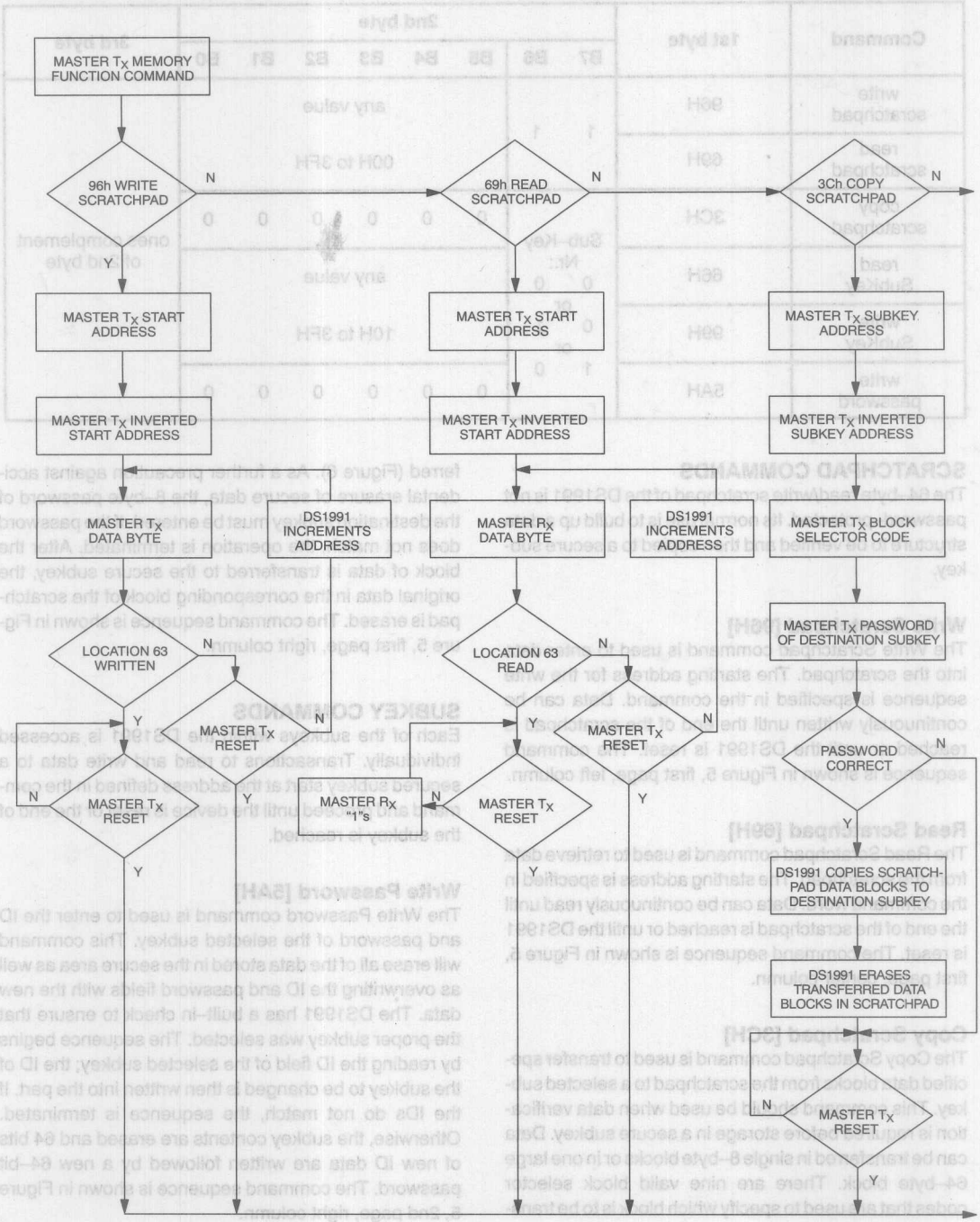
SUBKEY COMMANDS

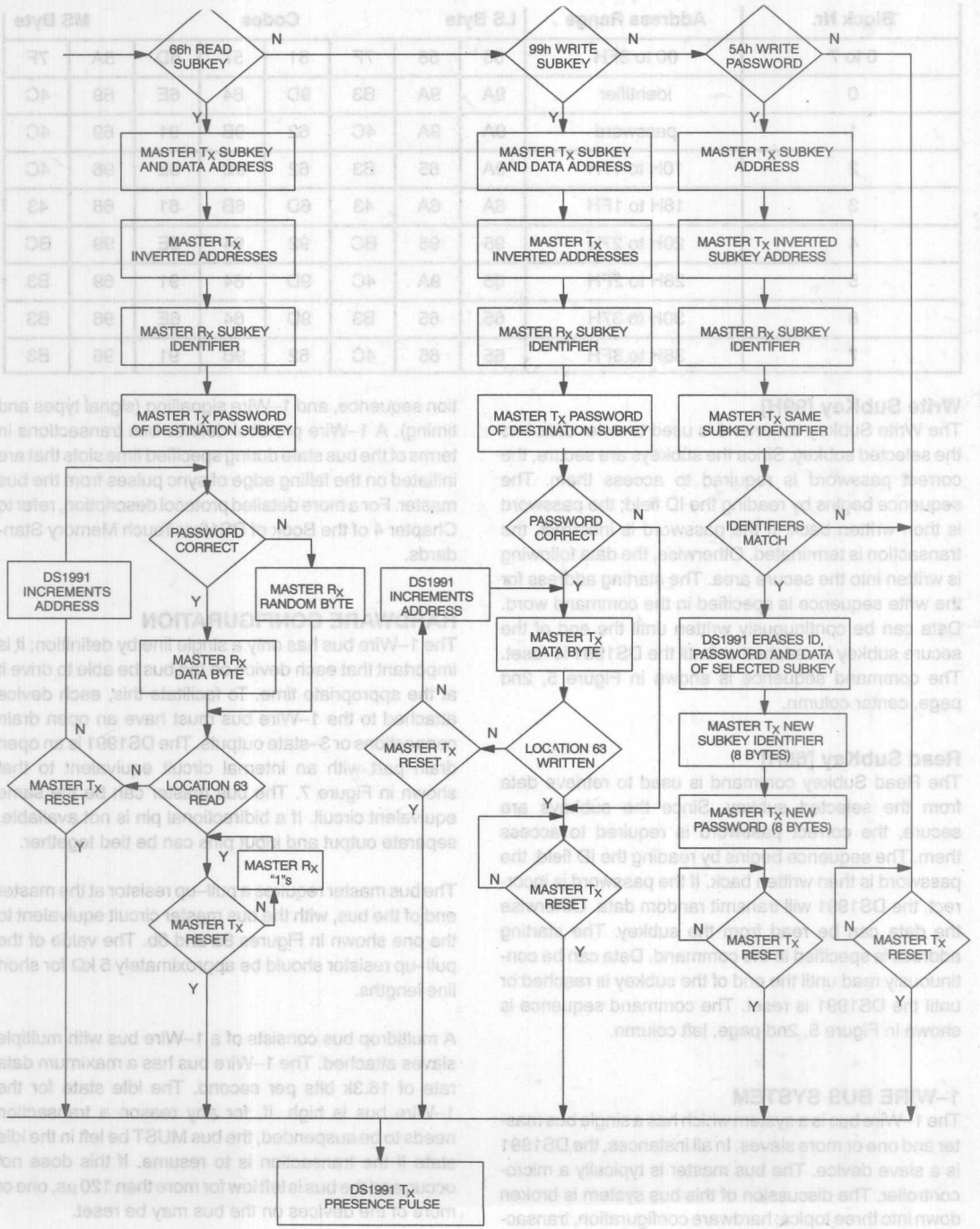
Each of the subkeys within the DS1991 is accessed individually. Transactions to read and write data to a secured subkey start at the address defined in the command and proceed until the device is reset or the end of the subkey is reached.

Write Password [5AH]

The Write Password command is used to enter the ID and password of the selected subkey. This command will erase all of the data stored in the secure area as well as overwriting the ID and password fields with the new data. The DS1991 has a built–in check to ensure that the proper subkey was selected. The sequence begins by reading the ID field of the selected subkey; the ID of the subkey to be changed is then written into the part. If the IDs do not match, the sequence is terminated. Otherwise, the subkey contents are erased and 64 bits of new ID data are written followed by a new 64–bit password. The command sequence is shown in Figure 5, 2nd page, right column.

MEMORY FUNCTIONS FLOW CHART Figure 5




66h READ SUBKEY
99h WRITE SUBKEY
5Ah WRITE PASSWORD
MASTER Tx SUBKEY AND DATA ADDRESS
MASTER Tx INVERTED ADDRESSES
MASTER Rx SUBKEY IDENTIFIER
MASTER Tx PASSWORD OF DESTINATION SUBKEY
MASTER Tx SUBKEY ADDRESS
MASTER Tx INVERTED SUBKEY ADDRESS
MASTER Tx SAME SUBKEY IDENTIFIER
PASSWORD CORRECT
IDENTIFIERS MATCH
DS1991 INCREMENTS ADDRESS
MASTER Rx RANDOM BYTE
MASTER Rx DATA BYTE
MASTER Tx DATA BYTE
DS1991 ERASES ID, PASSWORD AND DATA OF SELECTED SUBKEY
MASTER Tx NEW SUBKEY IDENTIFIER (8 BYTES)
MASTER Tx NEW PASSWORD (8 BYTES)
MASTER Tx RESET
LOCATION 63 READ
LOCATION 63 WRITTEN
MASTER Rx "1"s
DS1991 Tx PRESENCE PULSE
N
Y

BLOCK SELECTOR CODES OF THE DS1991 Figure 6

Block Nr.	Address Range	LS Byte			Codes				MS Byte
0 to 7	00 to 3FH	56	56	7F	51	57	5D	5A	7F
0	identifier	9A	9A	B3	9D	64	6E	69	4C
1	password	9A	9A	4C	62	9B	91	69	4C
2	10H to 17H	9A	65	B3	62	9B	6E	96	4C
3	18H to 1FH	6A	6A	43	6D	6B	61	66	43
4	20H to 27H	95	95	BC	92	94	9E	99	BC
5	28H to 2FH	65	9A	4C	9D	64	91	69	B3
6	30H to 37H	65	65	B3	9D	64	6E	96	B3
7	38H to 3FH	65	65	4C	62	9B	91	96	B3

Write SubKey [99H]

The Write Subkey command is used to enter data into the selected subkey. Since the subkeys are secure, the correct password is required to access them. The sequence begins by reading the ID field; the password is then written back. If the password is incorrect, the transaction is terminated. Otherwise, the data following is written into the secure area. The starting address for the write sequence is specified in the command word. Data can be continuously written until the end of the secure subkey is reached or until the DS1991 is reset. The command sequence is shown in Figure 5, 2nd page, center column.

Read SubKey [66H]

The Read Subkey command is used to retrieve data from the selected subkey. Since the subkeys are secure, the correct password is required to access them. The sequence begins by reading the ID field; the password is then written back. If the password is incorrect, the DS1991 will transmit random data. Otherwise the data can be read from the subkey. The starting address is specified in the command. Data can be continuously read until the end of the subkey is reached or until the DS1991 is reset. The command sequence is shown in Figure 5, 2nd page, left column.

1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS1991 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signalling (signal types and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

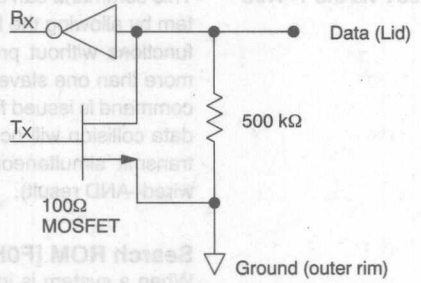
HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connections or 3–state outputs. The DS1991 is an open drain part with an internal circuit equivalent to that shown in Figure 7. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

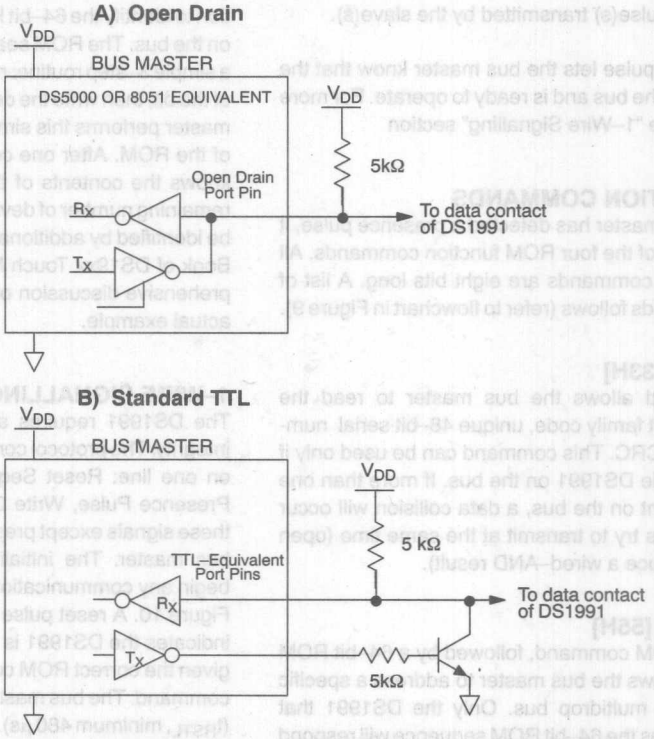
The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 8a and 8b. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths.

A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second. The idle state for the 1–Wire bus is high. If, for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur, and the bus is left low for more than 120 μs, one or more of the devices on the bus may be reset.

EQUIVALENT CIRCUIT Figure 7



BUS MASTER CIRCUIT Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS1991 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1991 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section

ROM FUNCTION COMMANDS

Once the bus master has detected a presence pulse, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9).

Read ROM [33H]

This command allows the bus master to read the DS1991's 8–bit family code, unique 48–bit serial number and 8–bit CRC. This command can be used only if there is a single DS1991 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result).

Match ROM [55H]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS1991 on a multidrop bus. Only the DS1991 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain will produce a wired–AND result).

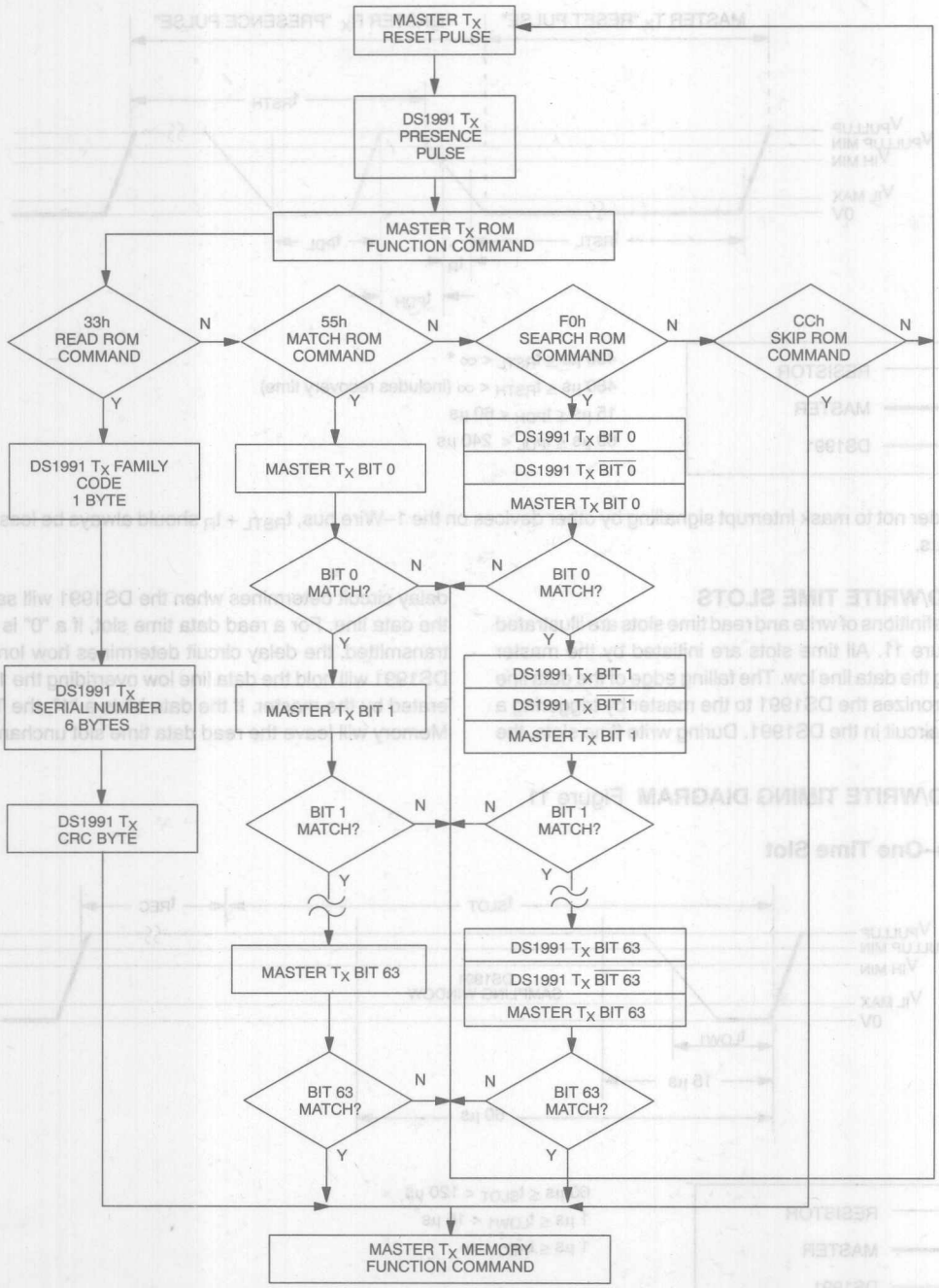
Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a search ROM, including an actual example.

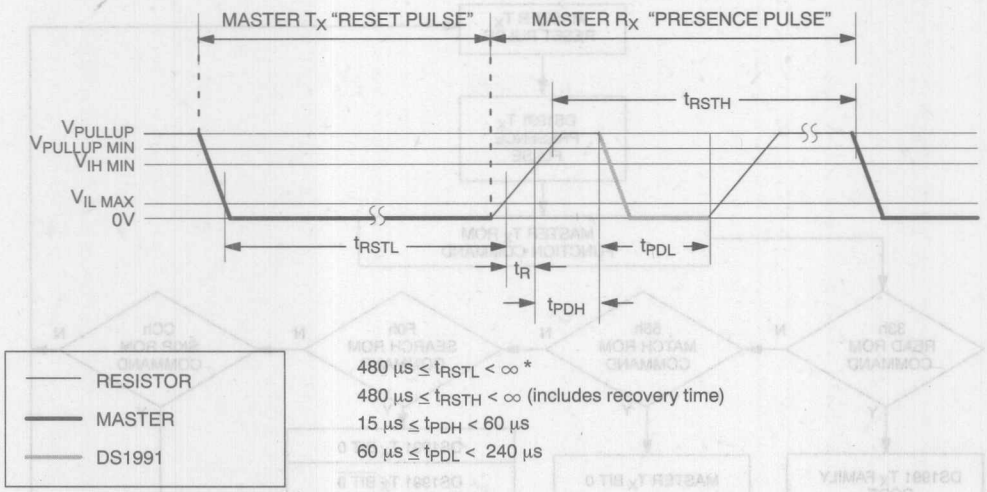
1–WIRE SIGNALLING

The DS1991 requires strict protocols to insure data integrity. The protocol consists of four types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS1991 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1991 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data pin, the DS1991 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

ROM FUNCTIONS FLOW CHART Figure 9



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



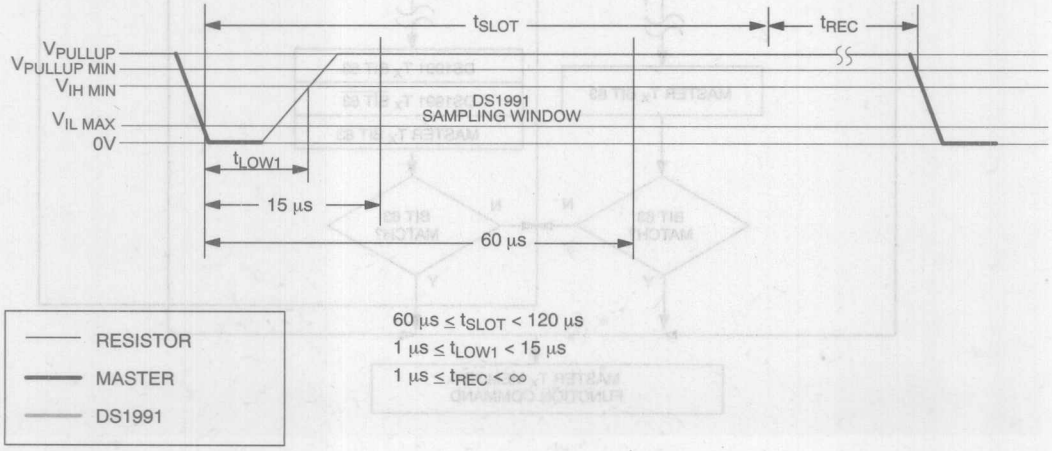
* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1991 to the master by triggering a delay circuit in the DS1991. During write time slots, the delay circuit determines when the DS1991 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1991 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

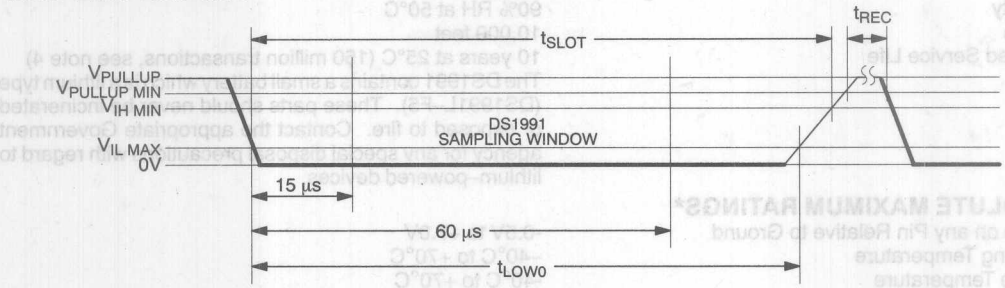
READ/WRITE TIMING DIAGRAM Figure 11

Write–One Time Slot



READ/WRITE TIMING DIAGRAM (cont'd) Figure 11

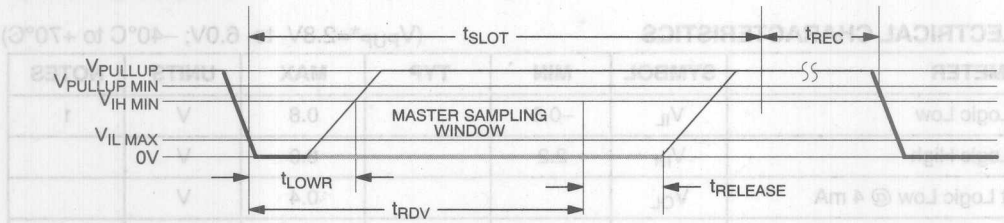
Write–Zero Time Slot

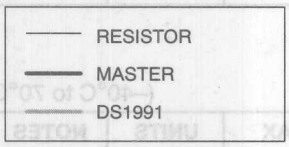


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–Data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C (150 million transactions, see note 4)
Safety	The DS1991 contains a small battery which is a lithium type (DS1991L–F5). These parts should never be incinerated or exposed to fire. Contact the appropriate Government agency for any special disposal precautions with regard to lithium–powered devices.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–40°C to +70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}*=2.8V to 6.0V; –40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	–0.3		0.8	V	1
Input Logic High	V_{IH}	2.2		6.0	V	
Output Logic Low @ 4 mA	V_{OL}			0.4	V	
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Resistance	R_I		500		kΩ	3

* V_{PUP} = external pull–up voltage

AC ELECTRICAL CHARACTERISTICS

(–40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot Period	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Low Time	t_{RSTL}	480			µs	
Reset High Time	t_{RSTH}	480			µs	4
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

2. V_{PUP} = external pull–up voltage to system supply.
3. Input pulldown resistance to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)

DALLAS SEMICONDUCTOR

DS1992/DS1993
1Kbit/4Kbit Touch Memory
DS1994
4Kbit Plus Time Touch Memory

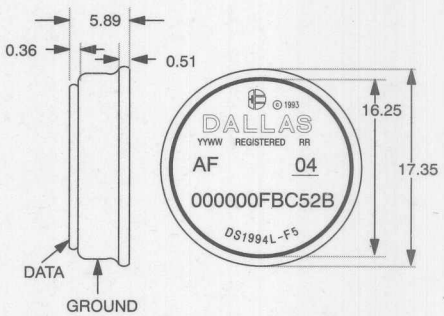
SPECIAL FEATURES

- 4096 bits of read/write nonvolatile memory (DS1993 and DS1994)
- 1024 bits of read/write nonvolatile memory (DS1992)
- 256–bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256–bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Contains real time clock/calendar in binary format (DS1994)
- Interval timer can automatically accumulate time when power is applied (DS1994)
- Programmable cycle counter can accumulate the number of system power–on/off cycles (DS1994)
- Programmable alarms can be set to generate interrupts for interval timer, real time clock, and/or cycle counter (DS1994)
- Write protect feature provides tamper–proof time data (DS1994)
- Programmable expiration date that will limit access to SRAM and timekeeping (DS1994)
- Clock accuracy is better than ±2 minute/month at 25°C (DS1994)
- Operating temperature range from –40°C to +70°C
- Over 10 years of data retention

COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations

F5 MICROCAN™



All dimensions shown in millimeters.

ORDERING INFORMATION

DS1992L–F5	F5 MicroCan
DS1993L–F5	F5 MicroCan
DS1994L–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1992/DS1993/DS1994 Touch Memory Button™ (hereafter referred to as DS199X) is a rugged read/write data carrier that acts as a localized database that can be easily accessed with minimal hardware. The nonvolatile memory and optional timekeeping capability offer a simple solution to storing and retrieving vital information pertaining to the object to which the Touch Memory is attached. Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory. A 48–bit serial number is factory lasered into each DS199X to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact coin–shaped profile is self–aligning with mating receptacles, allowing the DS199X to be easily used by human operators. Accessories permit the DS199X to be mounted on almost any surface including plastic key fobs, photo–ID badges and printed circuit boards.

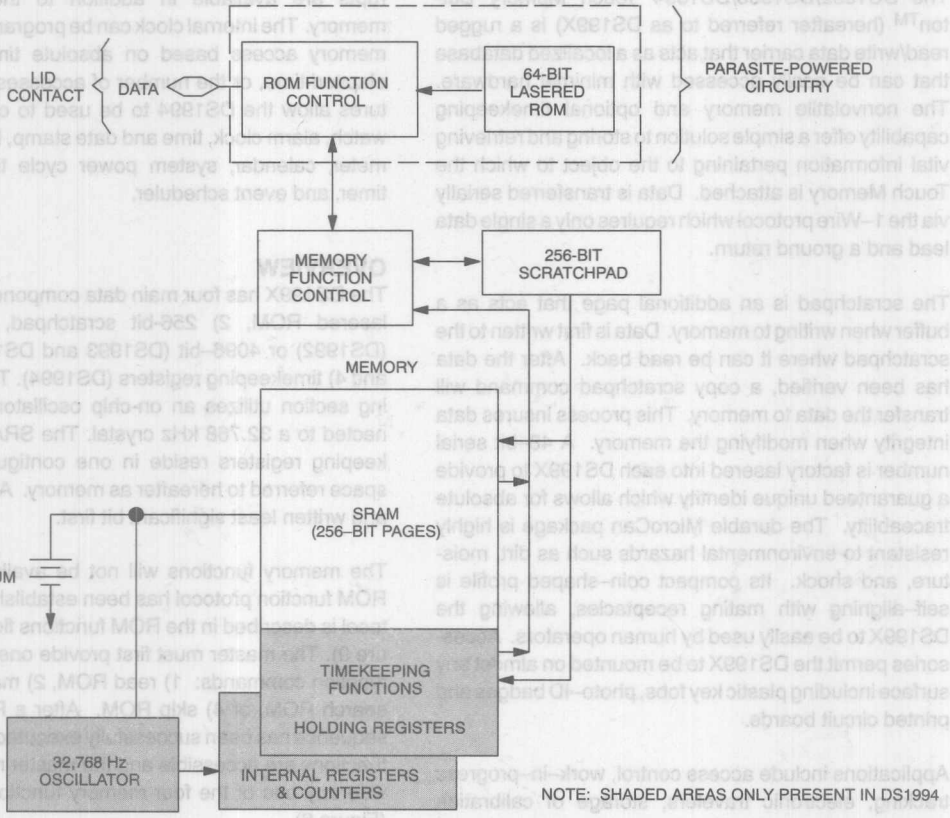
Applications include access control, work–in–progress tracking, electronic travelers, storage of calibration constants, and debit tokens. With the optional timekeeping functions (DS1994), a real time clock/calendar, interval timer, cycle counter, and programmable interrupts are available in addition to the nonvolatile memory. The internal clock can be programmed to deny memory access based on absolute time/date, total elapsed time, or the number of accesses. These features allow the DS1994 to be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, interval timer, and event scheduler.

OVERVIEW

The DS199X has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 1024–bit (DS1992) or 4096–bit (DS1993 and DS1994) SRAM, and 4) timekeeping registers (DS1994). The timekeeping section utilizes an on-chip oscillator that is connected to a 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

The memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands (Figure 6).

DS199X BLOCK DIAGRAM Figure 1



PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the data input is high. The data line will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved and 2) if the lithium is exhausted for any reason, the ROM may still be read normally.

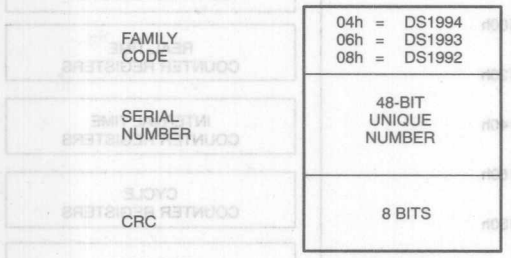
64-BIT LASERED ROM

Each DS199X contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

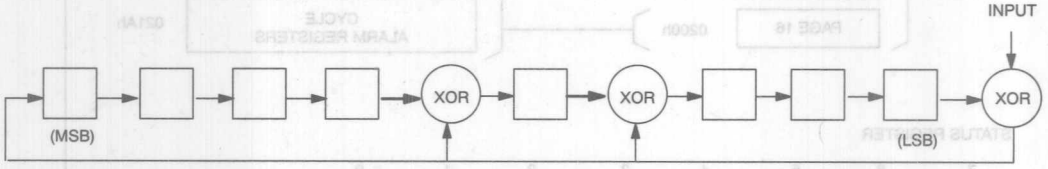
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards.

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

64-BIT LASERED ROM Figure 2

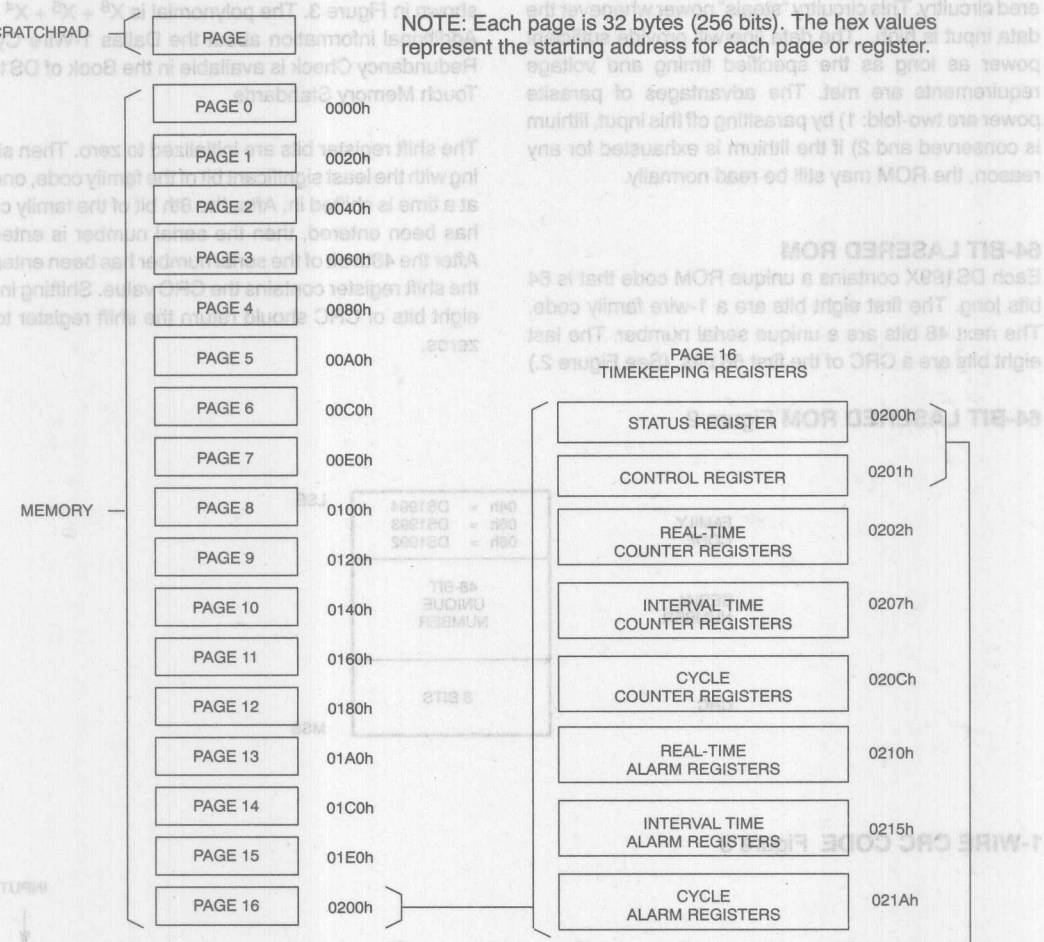


1-WIRE CRC CODE Figure 3



DS1994 MEMORY MAP Figure 4a

NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.



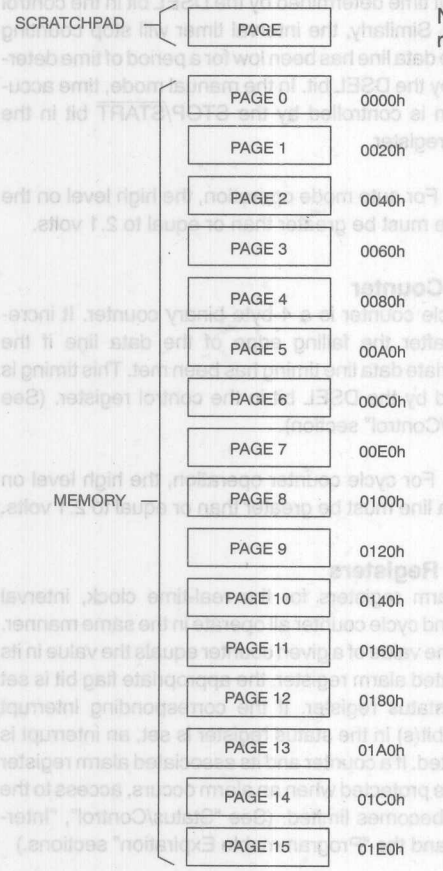
STATUS REGISTER

7	6	5	4	3	2	1	0	
X	X	$\overline{CCE}$	$\overline{ITE}$	$\overline{RTE}$	CCF	ITF	RTF	0200h

CONTROL REGISTER

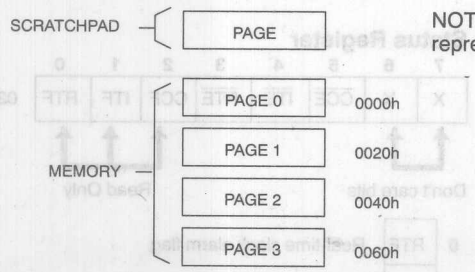
7	6	5	4	3	2	1	0	
DSEL	$\frac{STOP}{START}$	$\frac{AUTO}{MAN}$	OSC	RO	WPC	WPI	WPR	0201h

DS1993 MEMORY MAP Figure 4b



NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

DS1992 MEMORY MAP Figure 4c



NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

MEMORY

The memory map in Figure 4 shows a 32–byte page called the scratchpad and additional 32–byte pages called memory. The DS1992 contains pages 0 though 3 which make up the 1024–bit SRAM. The DS1993 and DS1994 contain pages 0 through 15 which make up the 4096–bit SRAM. The DS1994 also contains page 16 which has only 30 bytes that contain the timekeeping registers.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING (DS1994)

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer and cycle counter to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the data line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the data line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the data line must be greater than or equal to 2.1 volts.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the data line if the appropriate data line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the data line must be greater than or equal to 2.1 volts.

Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

STATUS/CONTROL REGISTERS (DS1994)

The status and control registers are the first two bytes of page 16 (see "Memory Map", Figure 4).

Status Register

7	6	5	4	3	2	1	0	
X	X	$\overline{\text{CCE}}$	$\overline{\text{ITE}}$	$\overline{\text{RTE}}$	CCF	ITF	RTF	0200h

Don't care bits — Read Only

0	RTF	Real-time clock alarm flag
1	ITF	Interval timer alarm flag
2	CCF	Cycle counter alarm flag

When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3	$\overline{RTE}$	Real-time interrupt enable
4	$\overline{ITE}$	Interval timer interrupt enable
5	$\overline{CCE}$	Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register

7	6	5	4	3	2	1	0	
DSEL	STOP/$\overline{START}$	AUTO/$\overline{MAN}$	OSC	RO	WPC	WPI	WPR	0201h

0	WPR	Write protect real-time clock/alarm registers
1	WPI	Write protect interval timer/alarm registers
2	WPC	Write protect cycle counter/alarm registers

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

3	RO	Read Only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS1994 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

4	OSC	Oscillator Enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

5	AUTO/$\overline{MAN}$	Automatic/$\overline{Manual}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the data line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{START}$ bit.

6	STOP/$\overline{START}$	Stop/$\overline{Start}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7	DSEL	Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the data line. When this bit is set to a logic 1, the delay time is 123 $\pm$ 2 ms. This delay allows communication on the data line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 $\pm$ 0.5 ms.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A logic 0 will be transmitted after the data has been copied until a reset pulse is issued by the user. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

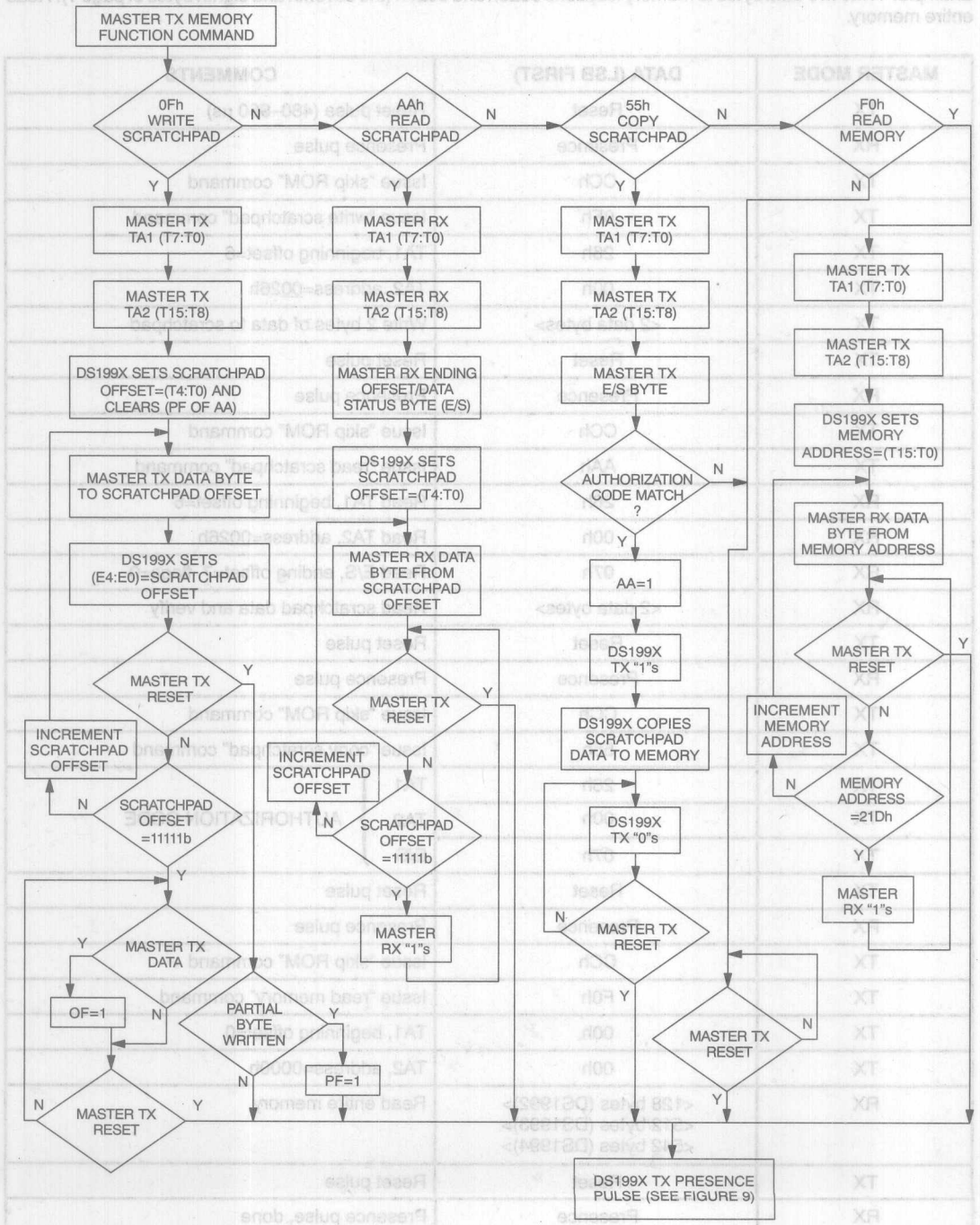
The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1992/DS1993/DS1994 provides a means to accomplish error–free writing to the memory section. To safeguard reading data in the 1–Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16–bit CRC with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the Book of DS19xx Touch Memory Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment.)

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 1). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<128 bytes (DS1992)> <512 bytes (DS1993)> <542 bytes (DS1994)>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

WRITE PROTECT/PROGRAMMABLE EXPIRATION (DS1994)

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS1994 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protect their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm WPR WPI WPC RO OSC*	Interval Timer Interval Time Alarm WPR WPI WPC RO OSC* STOP/$\overline{\text{START}}$** AUTO/$\overline{\text{MAN}}$	Cycle Counter Cycle Counter Alarm WPR WPI WPC RO OSC* DSEL

* Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".
** Forced to a logic "0".

1-WIRE BUS SYSTEM

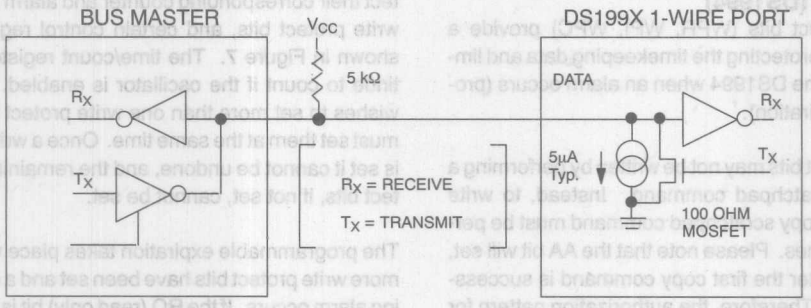
The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS199X behaves as a slave. The exception is when the DS1994 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3–state outputs. The 1-wire port of the DS199X is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1-wire bus has a maximum data rate of 16.3k bits per second and requires a pull-up resistor of approximately 5 kΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS199X via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS199X is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33h]

This command allows the bus master to read the DS199X's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS199X on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48–bit serial number will usually result in a mismatch of the CRC.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS199X on a multidrop bus. Only the DS199X that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

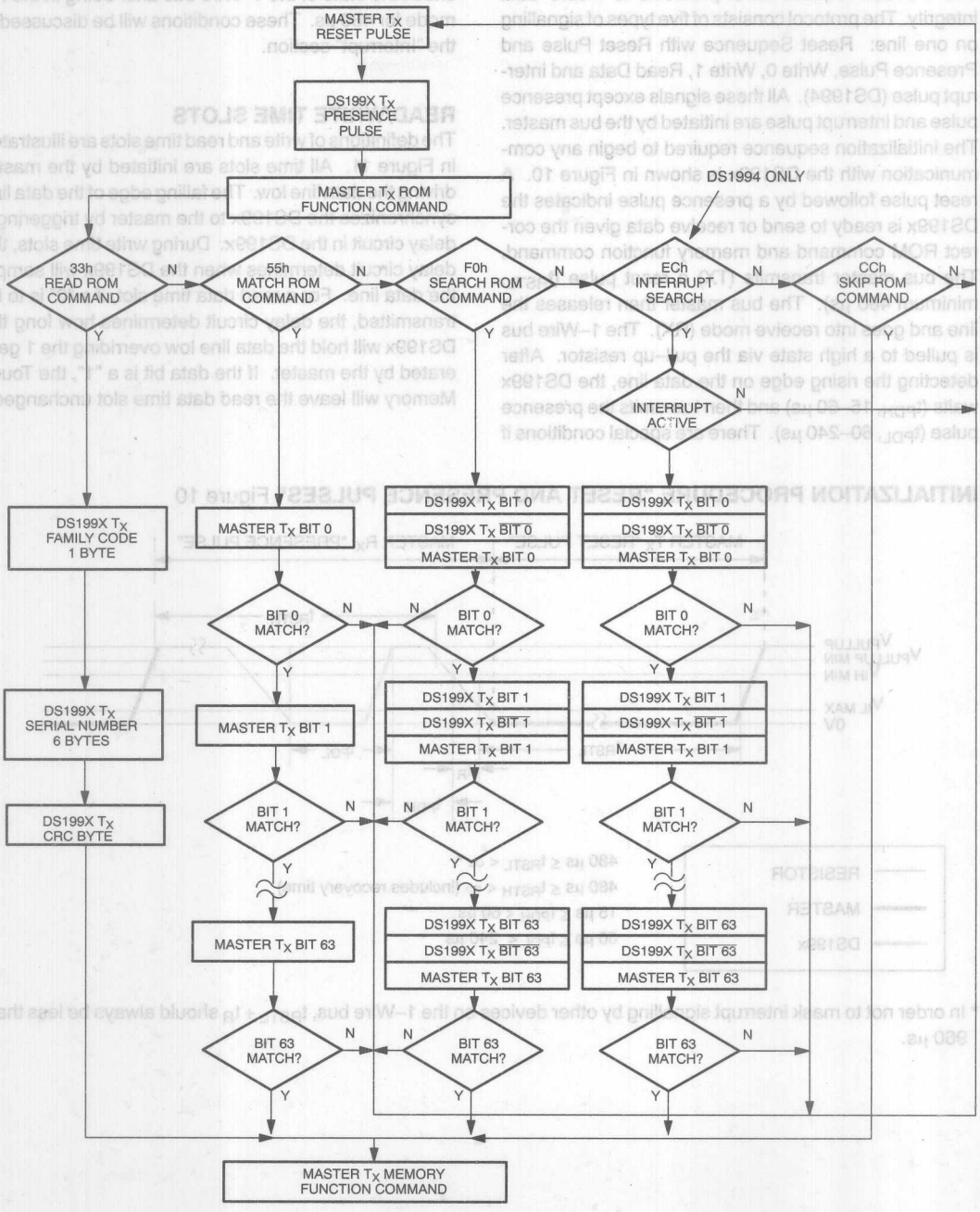
Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a search ROM, including an actual example.

Search Interrupt [ECh] (DS1994)

This ROM command works exactly as the normal ROM Search, but it will identify only devices with interrupts that have not yet been acknowledged.

ROM FUNCTIONS FLOW CHART Figure 9



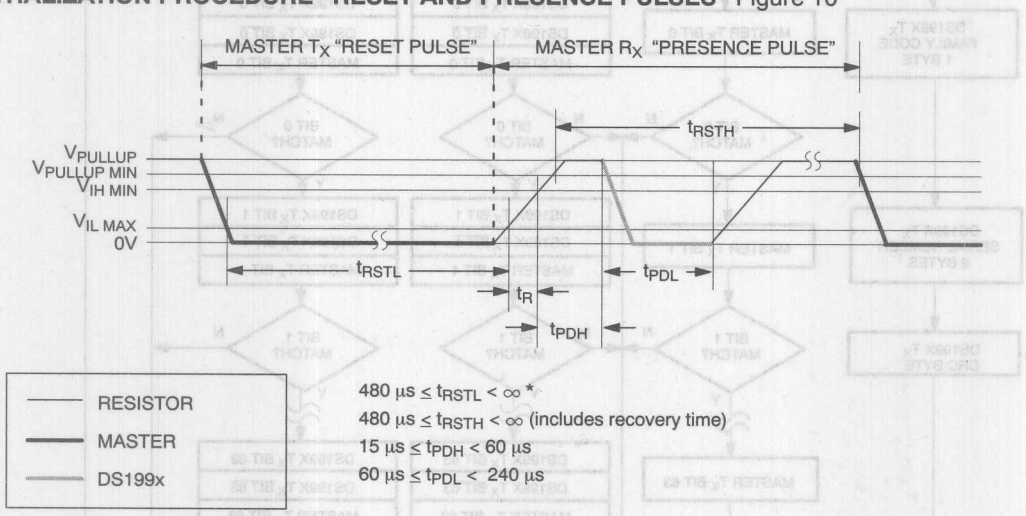
1–WIRE SIGNALLING

The DS199x requires strict protocols to insure data integrity. The protocol consists of five types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and interrupt pulse (DS1994). All these signals except presence pulse and interrupt pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS199x is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS199x is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data line, the DS199x waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1–Wire bus after being in the RX mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS199x to the master by triggering a delay circuit in the DS199x. During write time slots, the delay circuit determines when the DS199x will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS199x will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

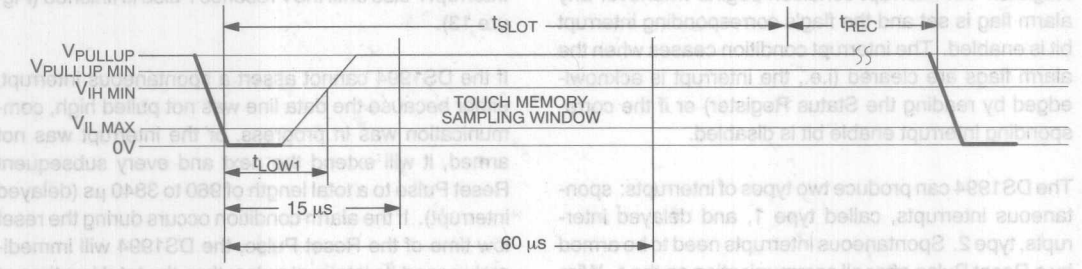
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



* In order not to mask interrupt signalling by other devices on the 1–Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

READ/WRITE TIMING DIAGRAM Figure 11

Write–One Time Slot

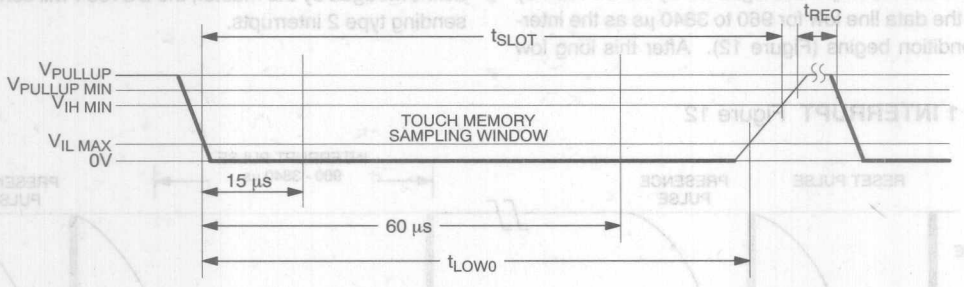


$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOW1} < 15\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

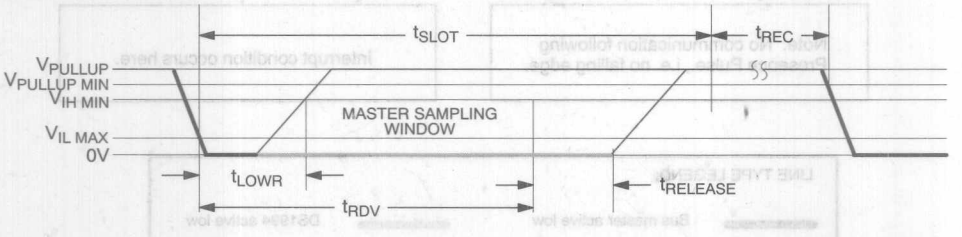
Write–Zero Time Slot

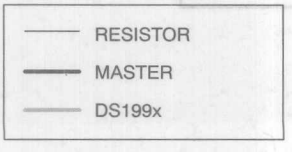


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–Data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

Interrupts (DS1994)

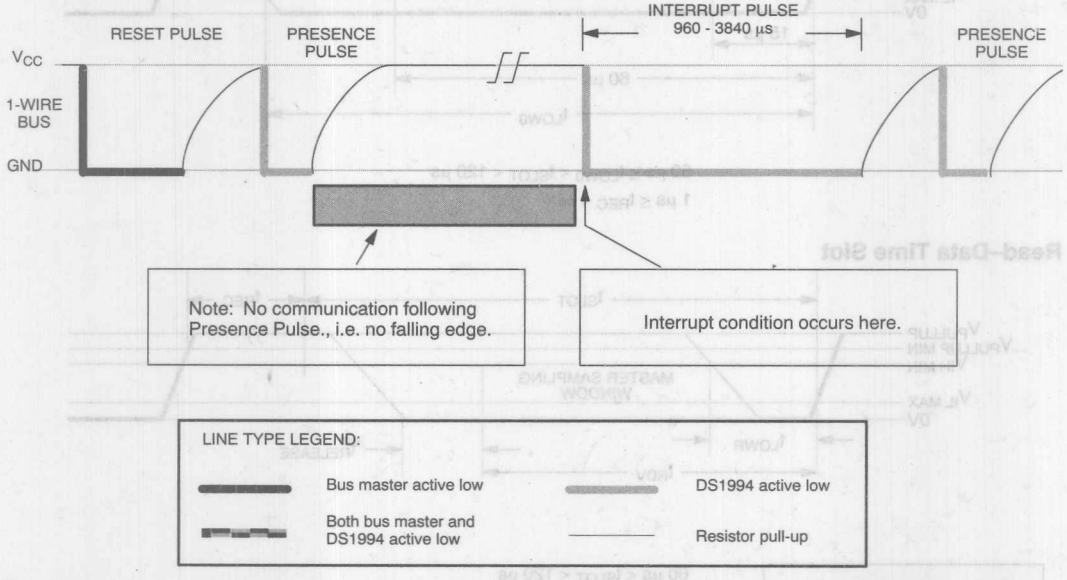
If the DS1994 detects an alarm condition, it will automatically set the corresponding alarm flag in the Status Register. An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the interrupt is acknowledged by reading the Status Register) or if the corresponding interrupt enable bit is disabled.

The DS1994 can produce two types of interrupts: spontaneous interrupts, called type 1, and delayed interrupts, type 2. Spontaneous interrupts need to be armed by a Reset Pulse after all communication on the 1–Wire bus has finished. A single falling slope on the 1–Wire bus will disarm this type of interrupt. If an alarm condition occurs while the device is disarmed, type 2 interrupts will be produced.

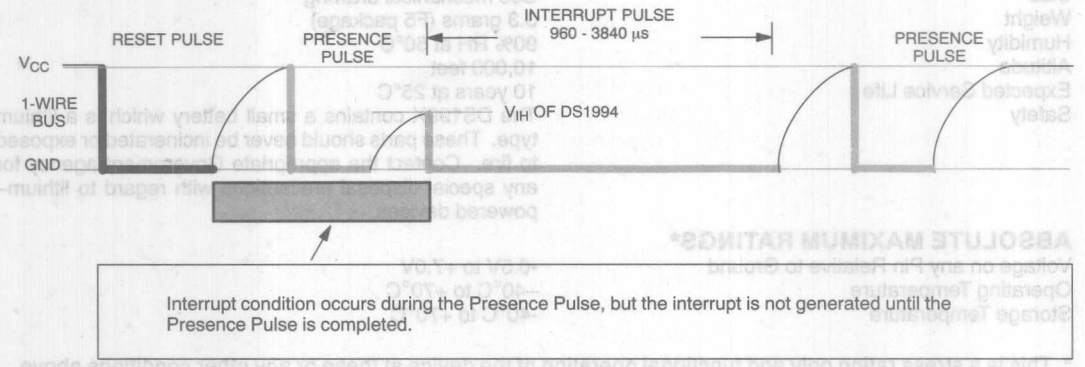
Spontaneous interrupts are signalled by the DS1994 by pulling the data line low for 960 to 3840 µs as the interrupt condition begins (Figure 12). After this long low pulse a Presence Pulse will follow. If the alarm condition occurs just after the master has sent a Reset Pulse, i.e., during the reset high time, the DS1994 will not assert its Interrupt Pulse until the Presence Pulse is finished (Figure 13).

If the DS1994 cannot assert a spontaneous interrupt, either because the data line was not pulled high, communication was in progress, or the interrupt was not armed, it will extend the next and every subsequent Reset Pulse to a total length of 960 to 3840 µs (delayed interrupt). If the alarm condition occurs during the reset low time of the Reset Pulse, the DS1994 will immediately assert its interrupt pulse; thus the total low time of the pulse can be extended up to 4800 µs (Figure 14). If a DS1994 with an active alarm detects a power–on cycle on the 1–Wire bus, it will send a Presence Pulse and wait for the Reset Pulses to signal a delayed interrupt (Figure 15). As long as an interrupt has not been acknowledged by the master, the DS1994 will continue sending type 2 interrupts.

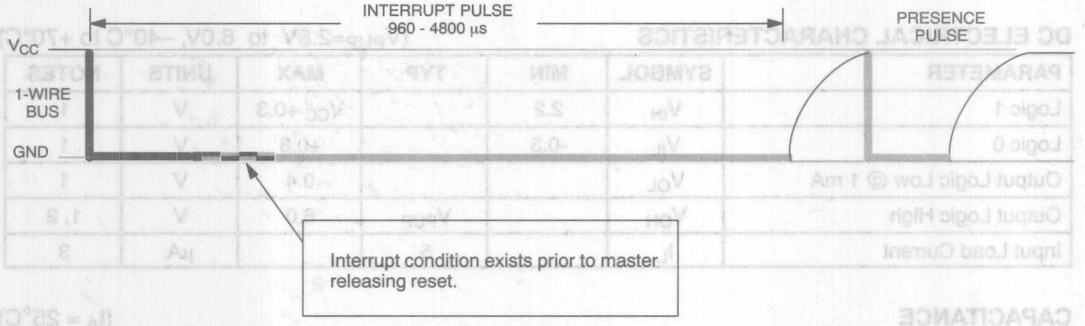
TYPE 1 INTERRUPT Figure 12



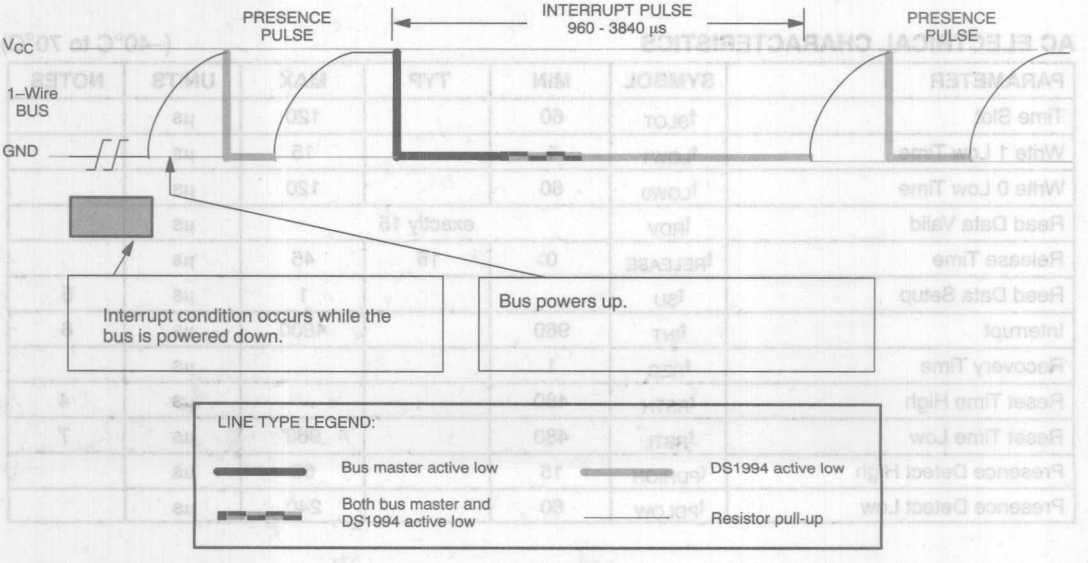
TYPE 1 INTERRUPT (SPECIAL CASE) Figure 13



TYPE 2 INTERRUPT Figure 14



TYPE 2 INTERRUPT (SPECIAL CASE) Figure 15



PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	The DS199X contains a small battery which is a lithium type. These parts should never be incinerated or exposed to fire. Contact the appropriate Government agency for any special disposal precautions with regard to lithium–powered devices.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–40°C to +70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V, –40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @ 1 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

AC ELECTRICAL CHARACTERISTICS

(–40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Interrupt	t_{INT}	960		4800	µs	8
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	7
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. Capacitance on the data line could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull-up the data line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signalling, otherwise, it could mask or conceal interrupt pulses.
8. DS1994 only.

PRELIMINARY

DALLAS SEMICONDUCTOR

DS1995
16Kbit Touch Memory

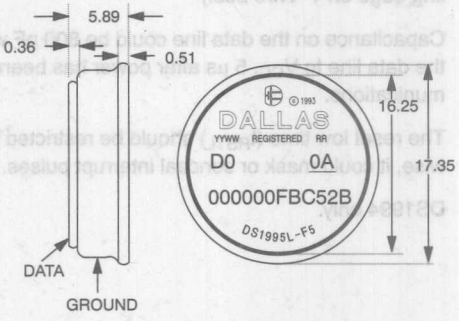
SPECIAL FEATURES

- 16384 bits of read/write nonvolatile memory
- 256–bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256–bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Operating temperature range from –40°C to +70°C
- Over 10 years of data retention

COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

F5 MICROCAN™



All dimensions are shown in millimeters.

ORDERING INFORMATION

DS1995L–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1995 Touch Memory Button™ operates nearly identically to the DS1996. The main differences are: 16K bits of memory organized as 64 pages of 32 bytes and a family code of 0A hexadecimal. For further details please refer to the DS1996 data sheet.

DALLAS SEMICONDUCTOR

DS1996
64Kbit Touch Memory

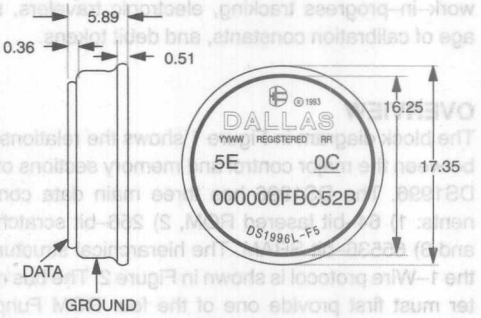
SPECIAL FEATURES

- 65536 bits of read/write nonvolatile memory
- 256–bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256–bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Operating temperature range from –40°C to +70°C
- Over 10 years of data retention

COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

F5 MICROCAN™



All dimensions are shown in millimeters.

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DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1996 Touch Memory Button™ is a rugged read/write data carrier that acts as a localized database that can be easily accessed with minimal hardware. The nonvolatile memory offers a simple solution to storing and retrieving vital information pertaining to the object to which the Touch Memory is attached. Data is transferred serially via the 1–wire protocol which requires only a single data lead and a ground return. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory. A 48–bit serial number is factory

lasered into each DS1996 to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact button–shaped profile is self–aligning with mating receptacles, allowing the DS1996 to be easily used by human operators. Accessories permit the DS1996 to be mounted on almost any surface including plastic key fobs, photo–ID badges and printed circuit boards. Applications include access control, work–in–progress tracking, electronic travelers, storage of calibration constants, and debit tokens.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1996. The DS1996 has three main data components: 1) 64–bit lasered ROM, 2) 256–bit scratchpad and 3) 65536–bit SRAM. The hierarchical structure of the 1–Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. The protocol required for these ROM Function Commands is described in Figure 9. After a ROM Function Command is successfully executed, the memory functions become accessible and the master may provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

PARASITE POWER

The block diagram (Figure 1) shows the parasite–powered circuitry. This circuitry "steals" power whenever the data line is high. The data line will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two–fold: 1) by parasiting off this input, lithium is conserved and 2) if the lithium is exhausted for any reason, the ROM may still be read normally.

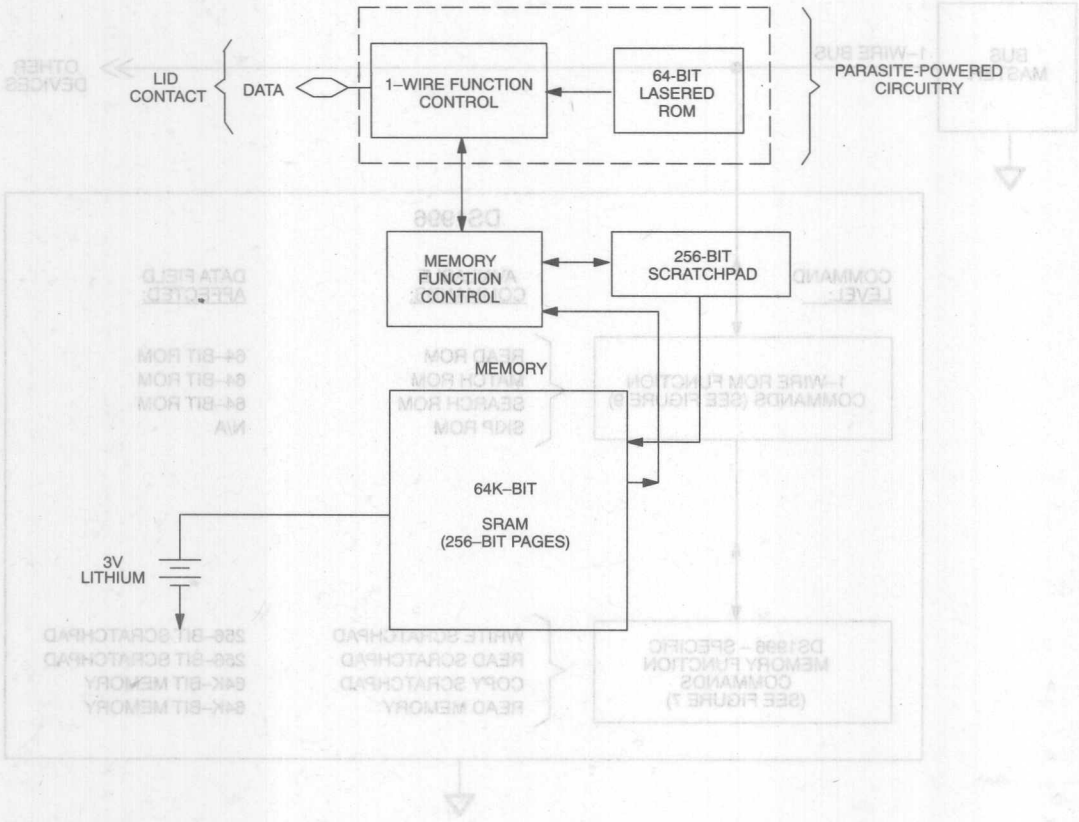
64–BIT LASERED ROM

Each DS1996 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (Figure 3.)

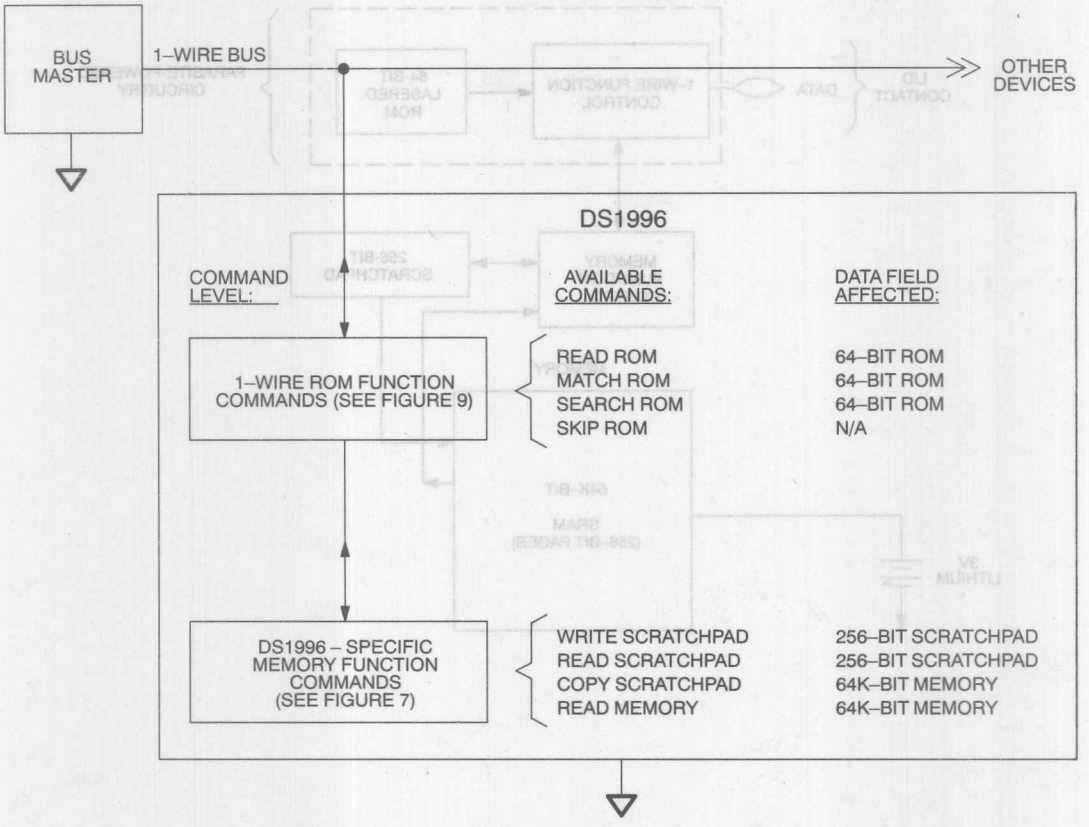
The 1–Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards.

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

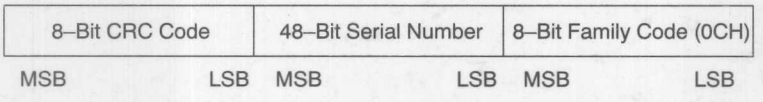
DS1996 BLOCK DIAGRAM Figure 1



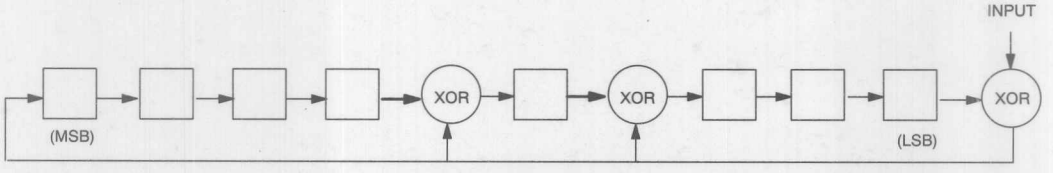
HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2



64–BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



MEMORY

The memory map in Figure 5 shows a 32–byte page called the scratchpad and additional 32–byte pages called memory. The DS1996 contains 256 pages which comprise the 65536–bit SRAM. The scratchpad is an additional page that acts as a buffer when writing to memory.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS1996 employs three address registers, called TA1, TA2 and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower five bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or "partial byte flag," is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6, OF or "Overflow," is set if more bits are sent by the master than can be stored in the scratchpad. Note that the lowest five bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address for a Write command is 13CH for example, then the scratchpad will store incoming data beginning at the byte offset 1CH and will be full after only four bytes. The corresponding ending offset in this example is 1FH. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32–byte capacity of the scratchpad is available, resulting also in the ending offset of 1FH. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial and Overflow Flag is mainly a means to support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

WRITING WITH VERIFICATION

To write data to the DS1996, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1996 sends the requested target address TA1 and TA2 and the contents of the E/S register. If one of the flags OF or PF is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the Touch Memory. If everything went correctly, all three flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S as the master has read them verifying the scratchpad. As soon as the Touch Memory has received these bytes, it will copy the data to the requested location beginning at the target address.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 7) describes the protocols necessary for accessing the memory. An example follows the flowchart.

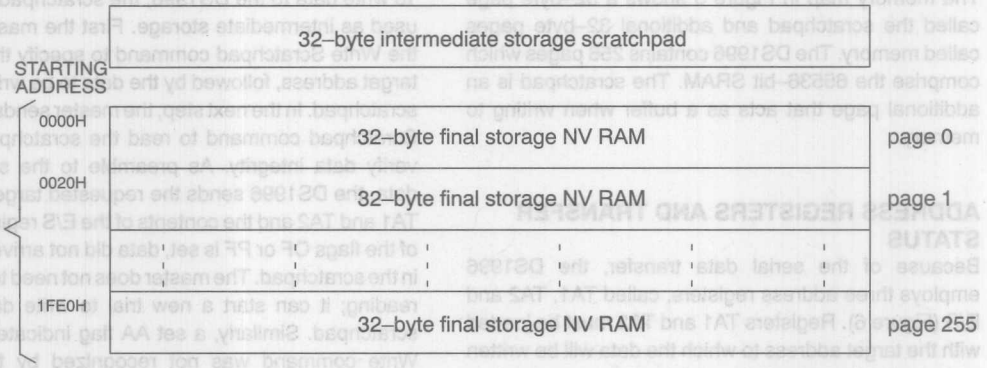
Write Scratchpad Command [0FH]

After issuing the write scratchpad command, the master must first provide the 2–byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the bus master has stopped writing data.

Read Scratchpad Command [AAH]

This command is used to verify scratchpad data and target address. After issuing the read scratchpad command, the master begins reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The master may read data until the end of the scratchpad after which the data read will be all logic 1's.

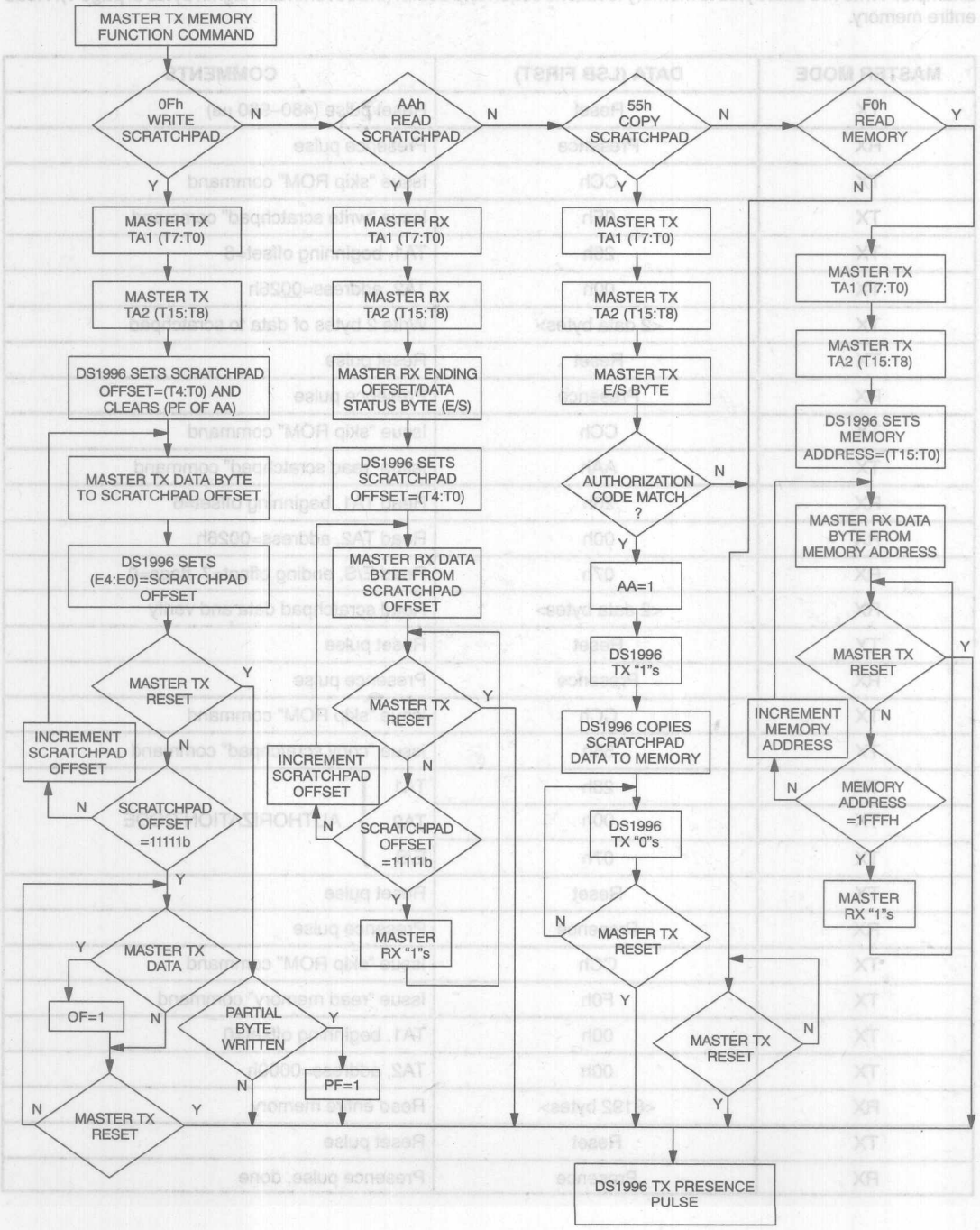
DS1996 MEMORY MAP Figure 5



ADDRESS REGISTERS Figure 6

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

MEMORY FUNCTION FLOW CHART Figure 7



MEMORY FUNCTION EXAMPLES

Example: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 1). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<8192 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

Copy Scratchpad [55H]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the master must provide a 3–byte authorization pattern which is obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A logic 0 will be transmitted after the data has been copied until a reset pulse is issued by the master. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0H]

The read memory command may be used to read the entire memory. After issuing the command, the master must provide the 2–byte target address. After the two bytes, the master reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1996 provides a means to accomplish error–free writing to the memory section. To safeguard reading data in the 1–Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16–bit CRC with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the Book of DS19xx Touch Memory Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment.)

1–WIRE BUS SYSTEM

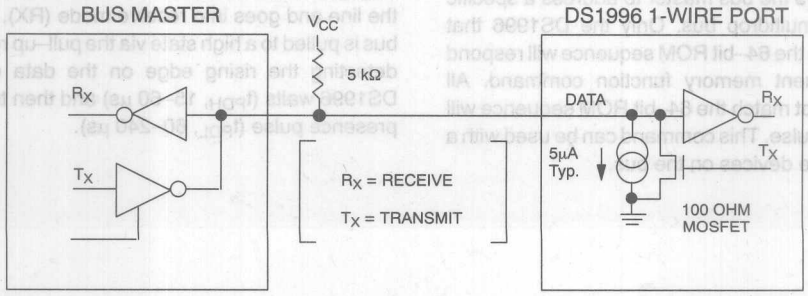
The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS1996 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signalling (signal types and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have open drain connection or 3–state outputs. The 1–Wire port of the DS1996 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second and requires a pull–up resistor of approximately 5 kΩ.

The idle state for the 1–Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS1996 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1996 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9).

Read ROM [33H]

This command allows the bus master to read the DS1996's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can only be used if there is a single DS1996 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result). The resultant family code and 48–bit serial number will usually result in a mismatch of the CRC.

Match ROM [55H]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS1996 on a multidrop bus. Only the DS1996 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

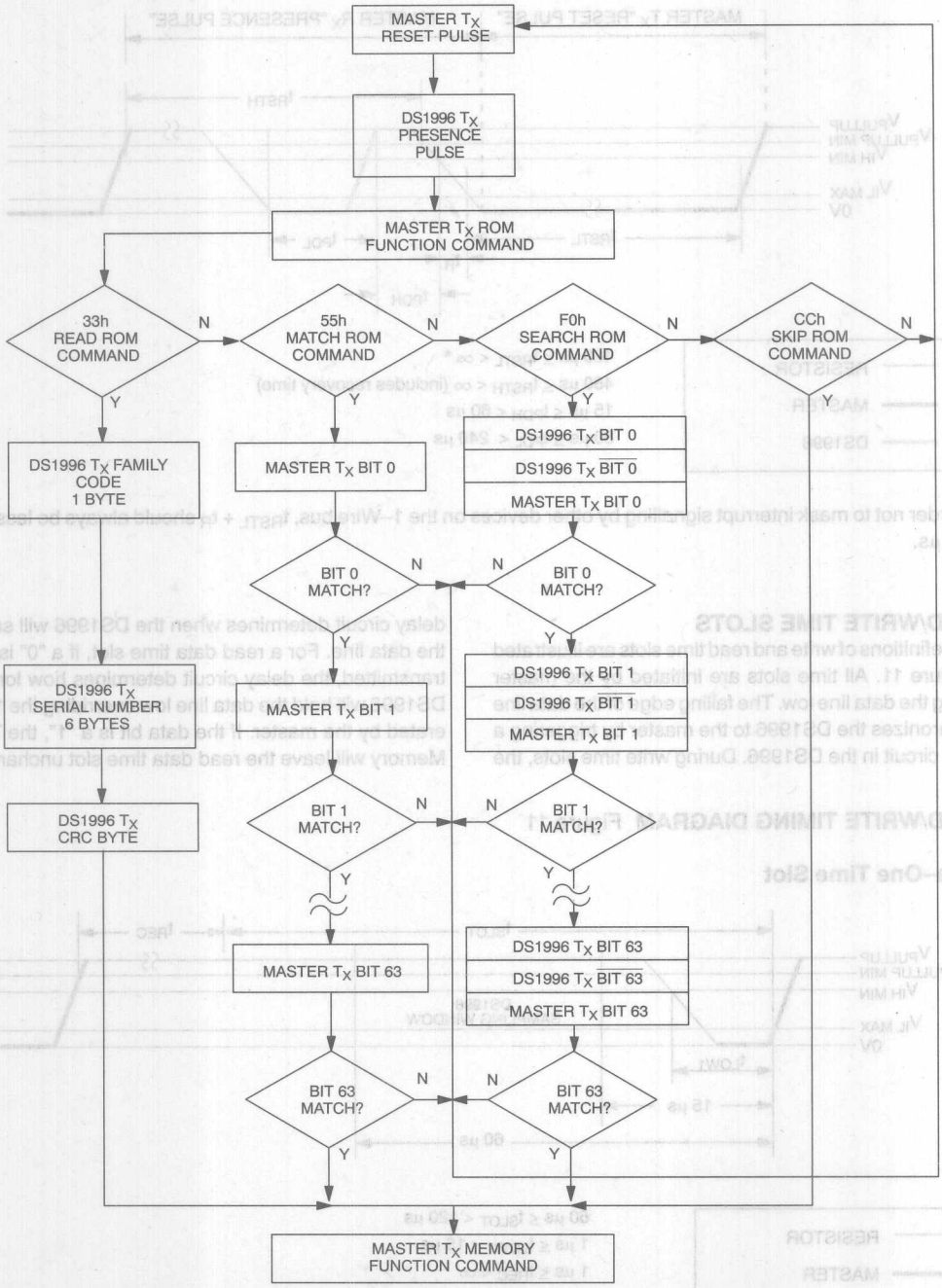
Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a search ROM, including an actual example.

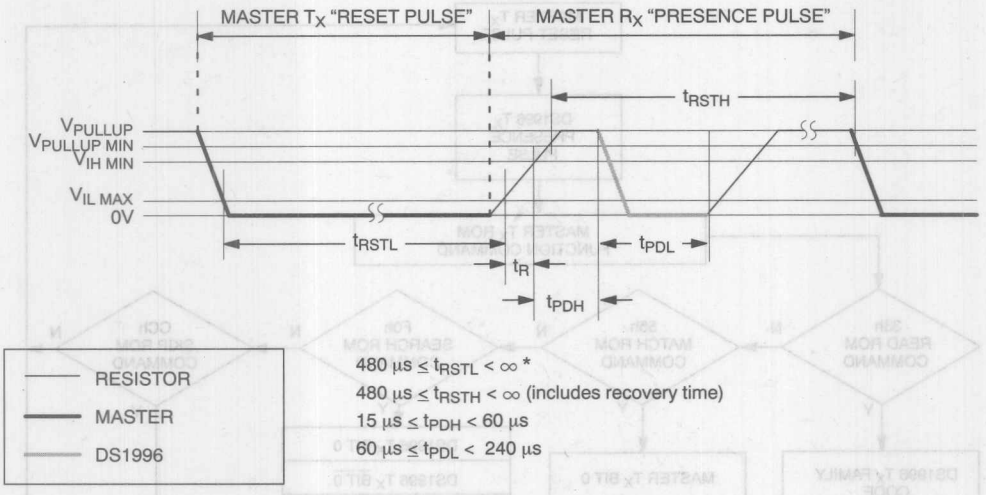
1–WIRE SIGNALLING

The DS1996 requires strict protocols to insure data integrity. The protocol consists of four types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS1996 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1996 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data contact, the DS1996 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

ROM FUNCTIONS FLOW CHART Figure 9



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



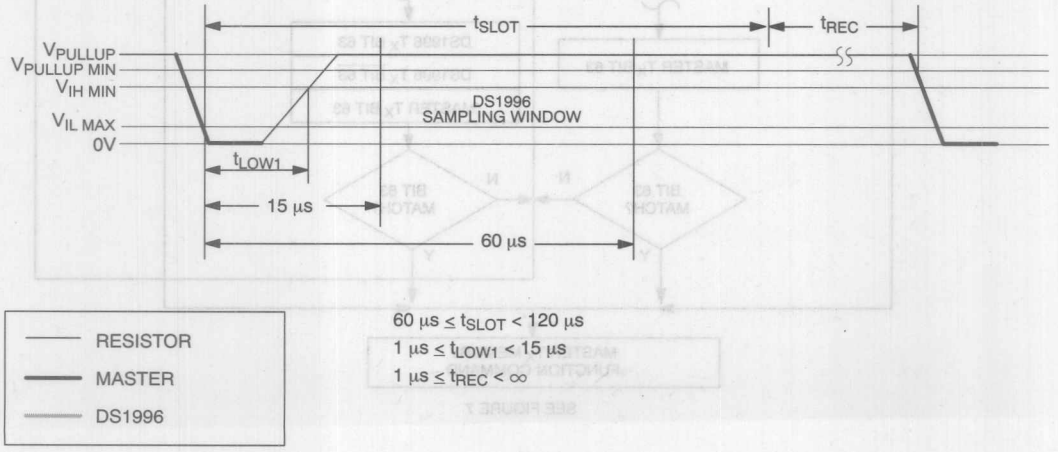
* In order not to mask interrupt signalling by other devices on the 1–Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1996 to the master by triggering a delay circuit in the DS1996. During write time slots, the delay circuit determines when the DS1996 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1996 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

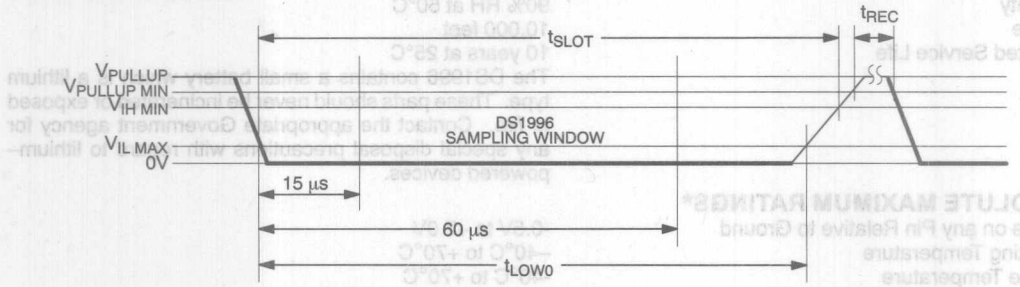
READ/WRITE TIMING DIAGRAM Figure 11

Write–One Time Slot



READ/WRITE TIMING DIAGRAM (cont'd) Figure 11

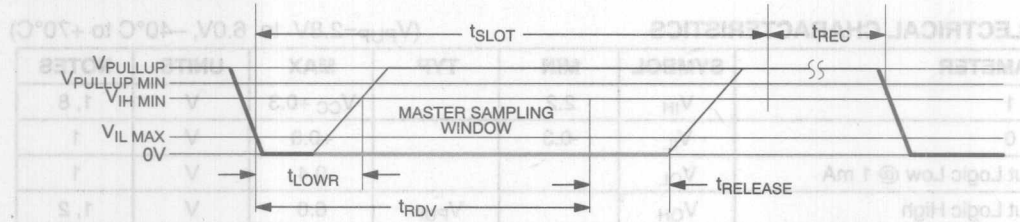
Write–Zero Time Slot

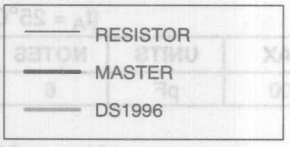


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–Data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	The DS1996 contains a small battery which is a lithium type. These parts should never be incinerated or exposed to fire. Contact the appropriate Government agency for any special disposal precautions with regard to lithium–powered devices.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–40°C to +70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V, –40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 8
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @ 1 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

AC ELECTRICAL CHARACTERISTICS

(–40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	7
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. Capacitance on the data contact could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull-up the data line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signalling, otherwise, it could mask or conceal interrupt pulses.
8. V_{IH} is a function of the external pull–up resistor and the V_{CC} power supply.

DALLAS SEMICONDUCTOR

DS1982
1Kbit Add–Only Touch Memory

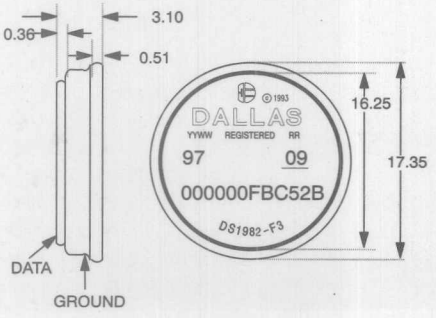
SPECIAL FEATURES

- 1024–bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- EPROM partitioned into four 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- 8–bit family code specifies DS1982 communications requirements to reader
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –40°C to +85°C

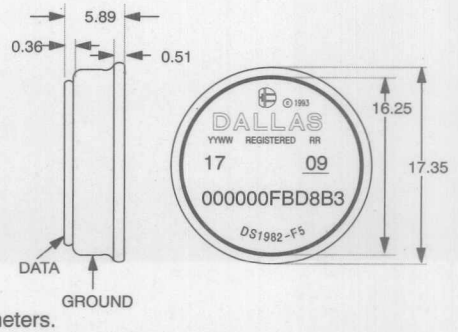
COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

F3 MICROCAN™



F5 MICROCAN™



All dimensions shown in millimeters.

ORDERING INFORMATION

DS1982–F3	F3 MicroCan
DS1982–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1982 1K–bit Touch Memory Button™ is a rugged read/write data carrier that identifies and stores relevant information about the product or person to which it is attached. This information can be accessed with minimal hardware, for example a single port pin of a microcontroller. The DS1982 consists of a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit Family Code (09h) plus 1K–bit of EPROM which is user–programmable. The power to program and read the DS1982 is derived entirely from the 1–Wire communication line. Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write–protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a standalone database. The 48–bit serial number that is factory–lasered into each DS1982 provides a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to harsh environments such as dirt, moisture, and shock. Its compact button–shaped profile is self–aligning with cup–shaped receptacles, allowing the DS1982 to be used easily by human operators or automatic equipment. Accessories permit the DS1982 to be mounted on printed circuit boards, plastic key fobs, photo–ID badges, ID bracelets, and many other objects. Applications include work–in–progress tracking, electronic travelers, access control, storage of calibration constants, and debit tokens.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1982. The DS1982 has three main data components: 1) 64–bit lasered ROM, 2) 1024–bit EPROM, and 3) EPROM Status Bytes. The device derives its power for read operations entirely from the 1–Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1–Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1–Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1–Wire line a special high voltage detect circuit within the DS1982 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1–Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 9. After a ROM Function Command is successfully executed, the memory functions that operate on the EPROM portions of the DS1982 become accessible and the bus master may issue any one of the five Memory Function Commands specific to the DS1982 to read or program the various data fields. The protocol for these Memory Function Commands is described in Figure 6. All data is read and written least significant bit first.

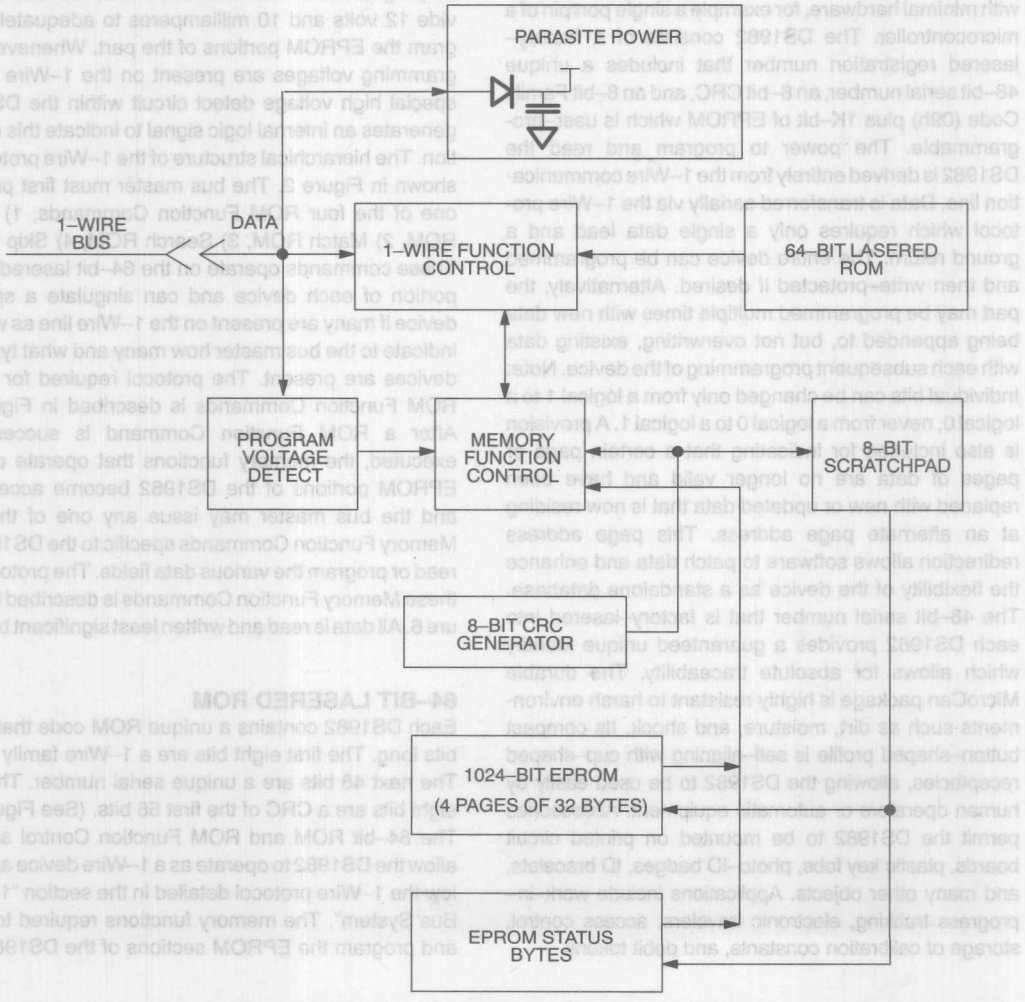
64–BIT LASERED ROM

Each DS1982 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 64–bit ROM and ROM Function Control section allow the DS1982 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The memory functions required to read and program the EPROM sections of the DS1982 are

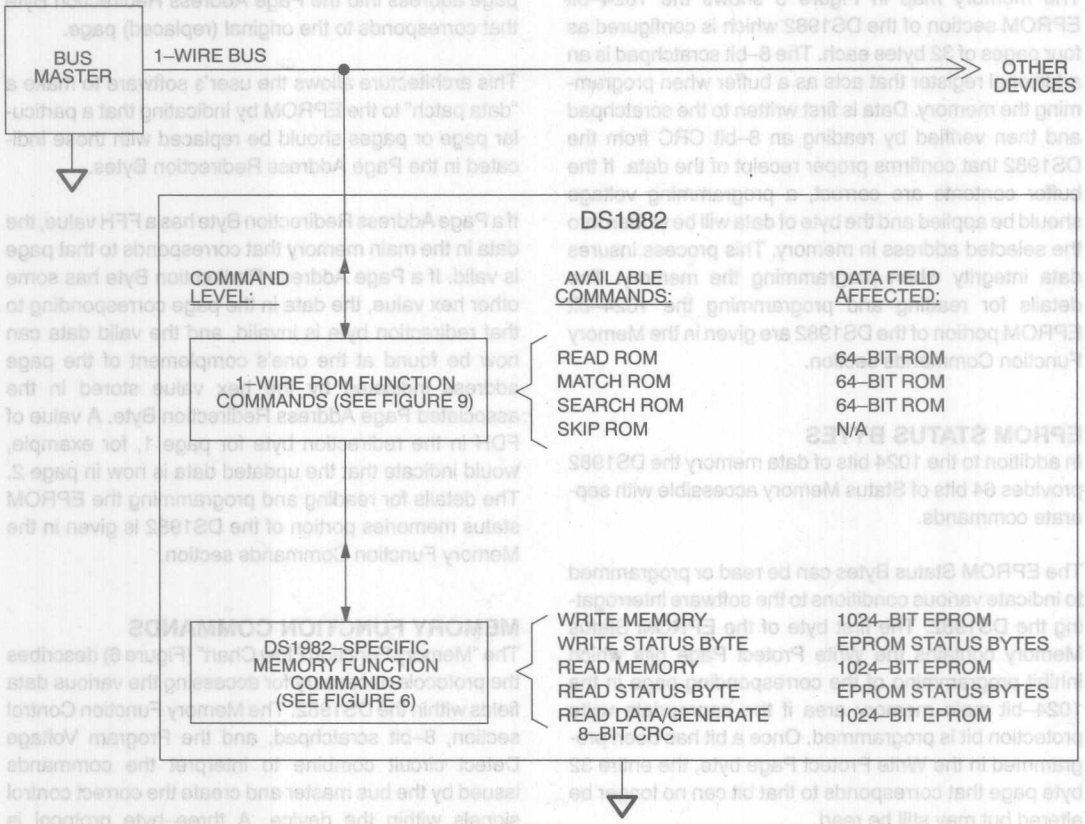
not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 9). The 1–Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS1982 (Figure 6).

The 1–Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards. The shift register acting as the CRC accumulator is initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the eighth bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeroes.

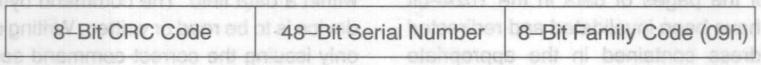
DS1982 BLOCK DIAGRAM Figure 1



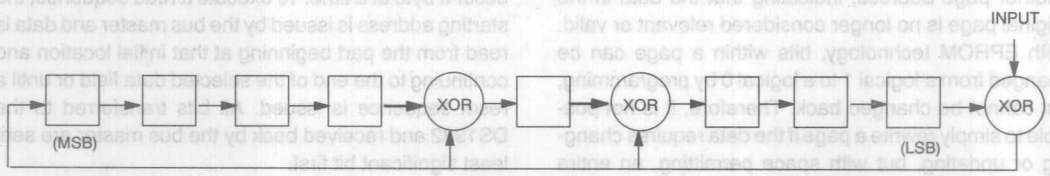
HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2



64–BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



1024–BIT EPROM

The memory map in Figure 5 shows the 1024–bit EPROM section of the DS1982 which is configured as four pages of 32 bytes each. The 8–bit scratchpad is an additional register that acts as a buffer when programming the memory. Data is first written to the scratchpad and then verified by reading an 8–bit CRC from the DS1982 that confirms proper receipt of the data. If the buffer contents are correct, a programming voltage should be applied and the byte of data will be written into the selected address in memory. This process insures data integrity when programming the memory. The details for reading and programming the 1024–bit EPROM portion of the DS1982 are given in the Memory Function Commands section.

EPROM STATUS BYTES

In addition to the 1024 bits of data memory the DS1982 provides 64 bits of Status Memory accessible with separate commands.

The EPROM Status Bytes can be read or programmed to indicate various conditions to the software interrogating the DS1982. The first byte of the EPROM Status Memory contains the Write Protect Page bits which inhibit programming of the corresponding page in the 1024–bit main memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page byte, the entire 32 byte page that corresponds to that bit can no longer be altered but may still be read.

The next four bytes of the EPROM Status Memory contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 1024–bit EPROM section have been invalidated and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS1982 makes no decisions based on the contents of the Page Address Redirection Bytes. These additional bytes of Status EPROM allow for the redirection of an entire page to another page address, indicating that the data in the original page is no longer considered relevant or valid. With EPROM technology, bits within a page can be changed from a logical 1 to a logical 0 by programming, but cannot be changed back. Therefore, it is not possible to simply rewrite a page if the data requires changing or updating, but with space permitting, an entire page of data can be redirected to another page within the DS1982 by writing the one's complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page.

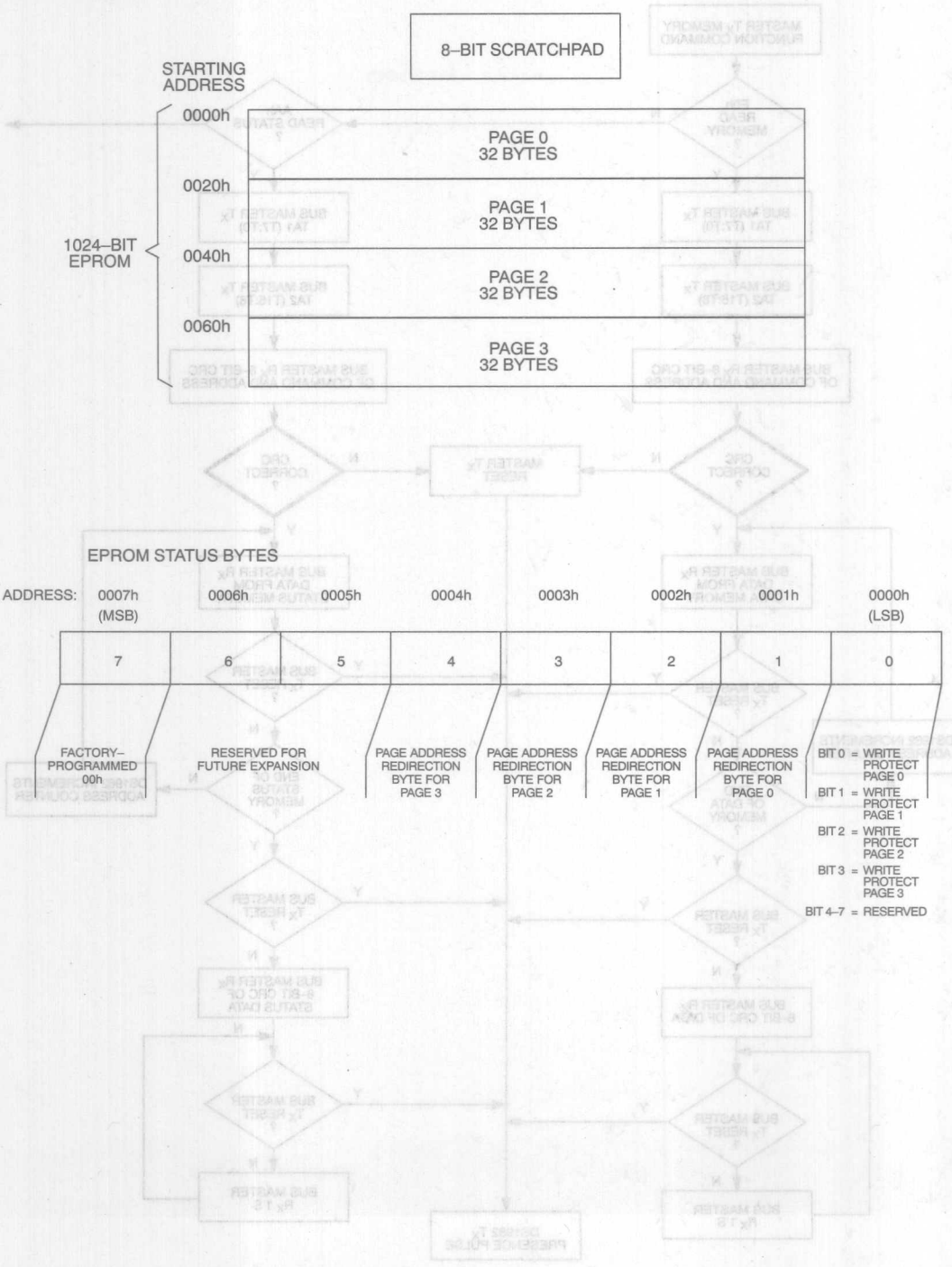
This architecture allows the user's software to make a "data patch" to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes.

If a Page Address Redirection Byte has a FFH value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value, the data in the page corresponding to that redirection byte is invalid, and the valid data can now be found at the one's complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDH in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. The details for reading and programming the EPROM status memories portion of the DS1982 is given in the Memory Function Commands section.

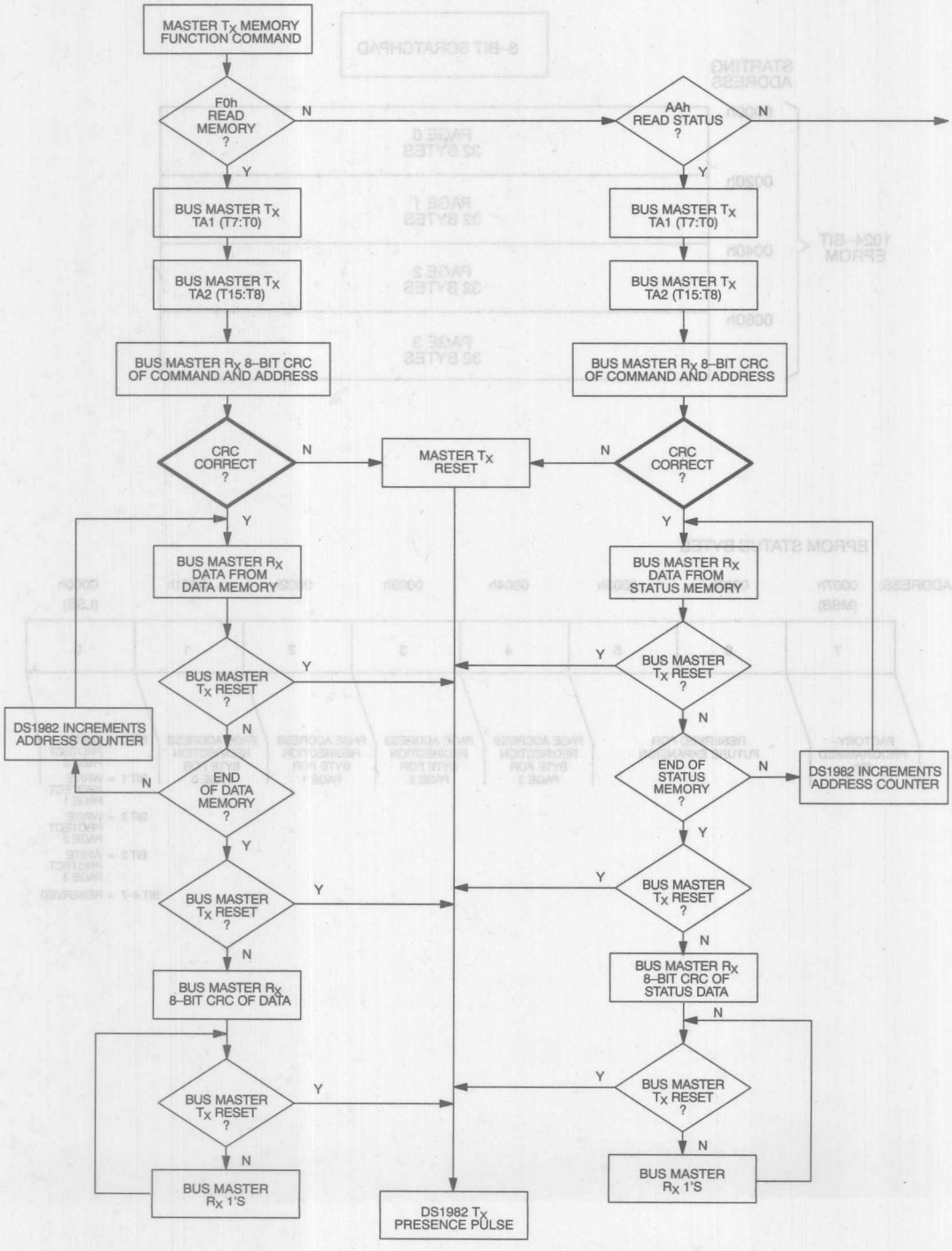
MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the various data fields within the DS1982. The Memory Function Control section, 8–bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three–byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field. The command byte indicates if the device is to be read or written. Writing data involves not only issuing the correct command sequence but also providing a 12 volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS1982 and received back by the bus master are sent least significant bit first.

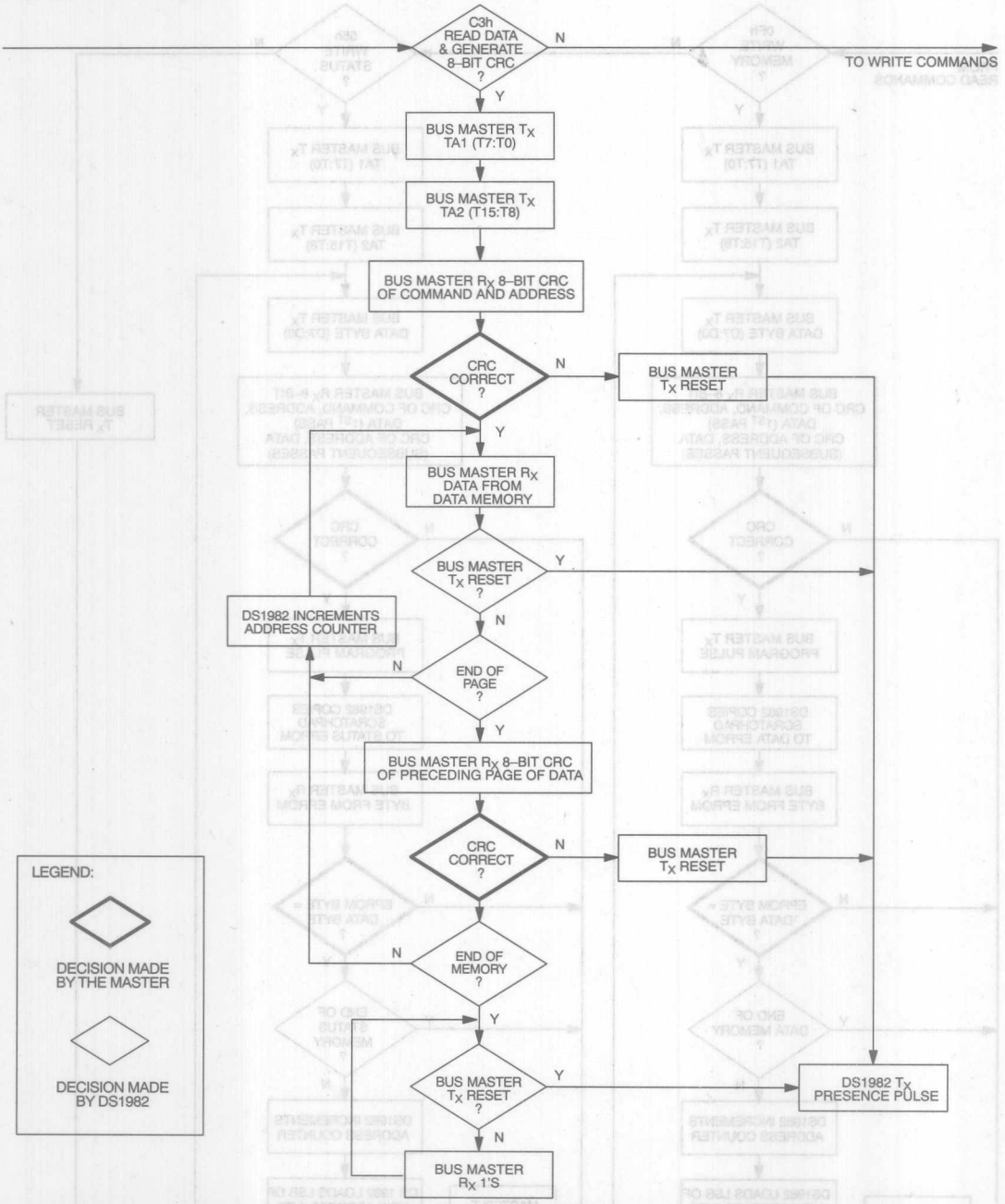
DS1982 MEMORY MAP Figure 5



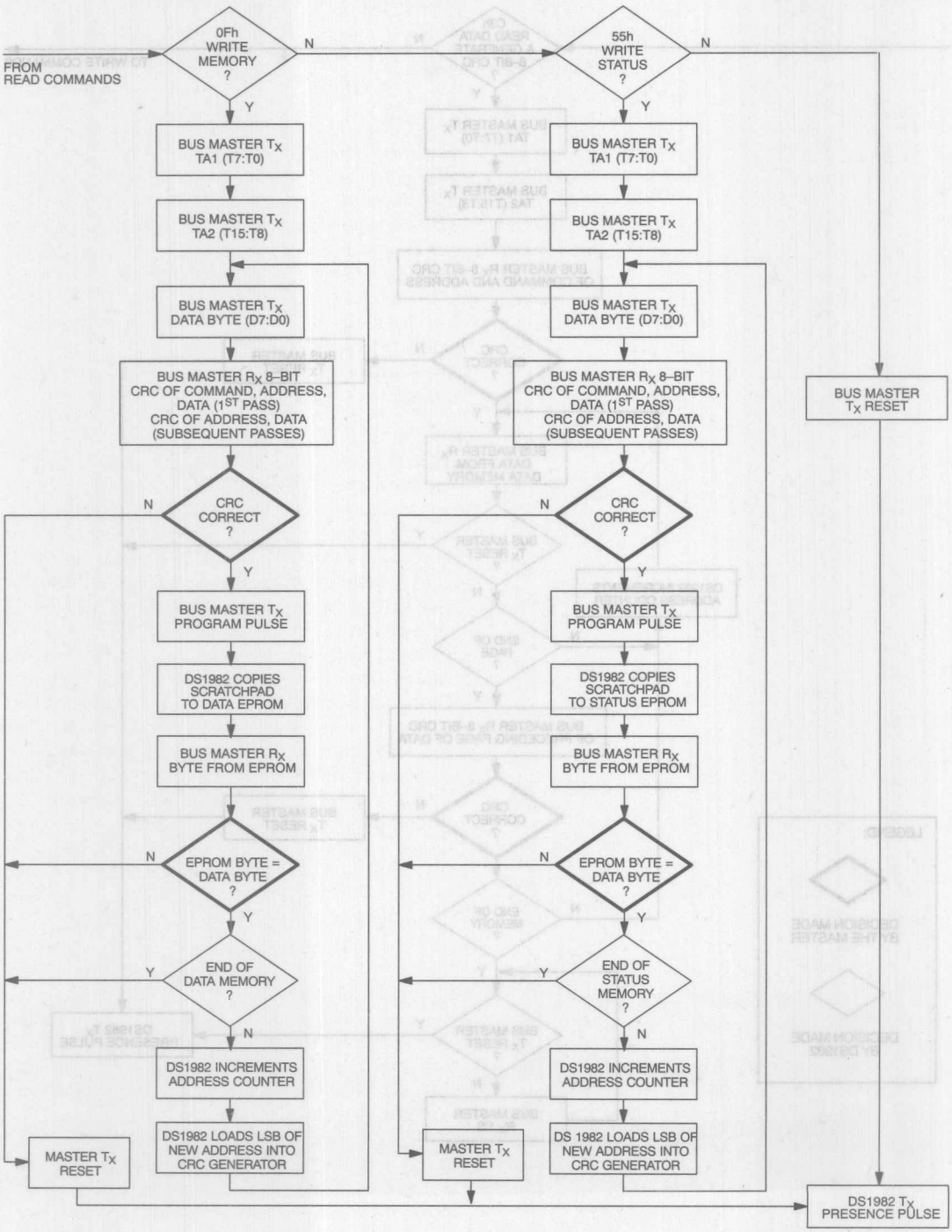
MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION FLOW CHART (cont'd) Figure 6



MEMORY FUNCTION FLOW CHART (cont'd) Figure 6



READ MEMORY [F0H]

The Read Memory command is used to read data from the 1024–bit EPROM data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8–bit CRC of the command byte and address bytes is computed by the DS1982 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS1982 starting at the initial address and continuing until the end of the 1024–bit data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue eight additional read time slots and the DS1982 will respond with an 8–bit CRC of all data bytes read from the initial starting byte through the last byte of memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 8–bit CRC available.

Typically a 16–bit CRC would be stored with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Book of DS19xx Touch Memory Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment.) If CRC values are imbedded within the data, a Reset Pulse may be issued at the end of memory space during a Read Memory command.

READ STATUS [AAH]

The Read Status command is used to read data from the EPROM Status data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8–bit CRC of the command byte and address bytes is computed by the DS1982 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS1982 starting at the supplied address and continuing until the end of the EPROM Status data field is reached. At that point the bus master will receive an 8–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte through the final factory–programmed byte that contains the 00h value.

This feature is provided since the EPROM Status information may change over time making it impossible to program the data once and include an accompanying CRC that will always be valid. Therefore, the Read Status command supplies an 8–bit CRC that is based on and always is consistent with the current data stored in the EPROM Status data field.

After the 8–bit CRC is read, the bus master will receive logical 1s from the DS1982 until a Reset Pulse is issued. The Read Status command sequence can be exited at any point by issuing a Reset Pulse.

READ DATA/GENERATE 8–BIT CRC [C3H]

The Read Data/Generate 8–bit CRC command is used to read data from the 1024–bit EPROM memory field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8–bit CRC of the command byte and address bytes is computed by the DS1982 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS1982 starting at the initial address and continuing until the end of a 32–byte page is reached. At that point the bus master will send eight additional read time slots and receive an 8–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page. Once the 8–bit CRC has been received, data is again read from the 1024–bit EPROM data field starting at the next page. This sequence will continue until the final page and its accompanying CRC are read by the bus master. Thus each page of data can be considered to be 33 bytes long, the 32 bytes of user–programmed EPROM data and an 8–bit CRC that gets generated automatically at the end of each page.

This type of read differs from the Read Memory command which simply reads each page until the end of address space is reached. The Read Memory com-

mand only generates an 8–bit CRC at the end of memory space that often might be ignored, since in many applications the user would store a 16–bit CRC with the data itself in each page of the 1024–bit EPROM data field at the time the page was programmed.

The Read Data/Generate 8–bit CRC command provides an alternate read capability for applications that are "bit–oriented" rather than "page–oriented" where the 1024–bit EPROM information may change over time within a page boundary making it impossible to program the page once and include an accompanying CRC that will always be valid. Therefore, the Read Data/Generate 8–Bit CRC command concludes each page with the DS1982 generating and supplying an 8–bit CRC that is based on and therefore is always consistent with the current data stored in each page of the 1024–bit EPROM data field. After the 8–bit CRC of the last page is read, the bus master will receive logical 1s from the DS1982 until a Reset Pulse is issued. The Read Data/Generate 8–Bit CRC command sequence can be exited at any point by issuing a Reset Pulse.

WRITE MEMORY [0FH]

The Write Memory command is used to program the 1024–bit EPROM data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). An 8–bit CRC of the command byte, address bytes, and data byte is computed by the DS1982 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 µs) is issued by the bus master. Prior to programming, the entire unprogrammed 1024–bit EPROM data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the 1024–bit EPROM will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480 µs programming pulse is applied and the data line returns to a 5 volt level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS1982 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM data address. If the EPROM data byte contains 1s in bit positions where the byte issued by the master contains 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS1982 EPROM data byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS1982 will automatically increment its address counter to select the next byte in the 1024–bit EPROM data field. The least significant byte of the new two–byte address will also be loaded into the 8–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS1982 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8–bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the bus master will read this 8–bit CRC from the DS1982 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Memory command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Memory flow chart will generate an 8–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Memory flow chart due to the DS1982 automatically incrementing its address counter will generate an 8–bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS1982) is made entirely by the bus master, since the DS1982 will not be able to determine if the 8–bit CRC calculated by the bus master agrees with the 8–bit CRC calculated by the DS1982. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS1982. Also note that the DS1982 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the

programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Memory command, incorrect programming could occur within the DS1982. The Write Memory command sequence can be exited at any point by issuing a Reset Pulse.

WRITE STATUS [55H]

The Write Status command is used to program the EPROM Status data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of status data (D7:D0). An 8–bit CRC of the command byte, address bytes, and data byte is computed by the DS1982 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 µs) is issued by the bus master. Prior to programming, the first seven bytes of the EPROM Status data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM Status data field will be programmed to a logical 0 after the programming pulse has been applied at that byte location. The eighth byte of the EPROM Status Byte data field is factory–programmed to contain 00h.

After the 480 µs programming pulse is applied and the data line returns to a 5 volt level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS1982 responds with the data from the selected EPROM Status address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM Status Byte address. If the EPROM Status Byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS1982 EPROM Status Byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS1982 will automatically increment its address counter to select the next byte in the EPROM Status data field. The least significant byte of the new two–byte address will also be loaded into the 8–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS1982 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8–bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the bus master will read this 8–bit CRC from the DS1982 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Status flow chart will generate an 8–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Status flow chart due to the DS1982 automatically incrementing its address counter will generate an 8–bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS1982) is made entirely by the bus master, since the DS1982 will not be able to determine if the 8–bit CRC calculated by the bus master agrees with the 8–bit CRC calculated by the DS1982. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS1982. Also note that the DS1982 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Status command, incorrect programming could occur within the DS1982. The Write Status command sequence can be ended at any point by issuing a Reset Pulse.

1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS1982 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signalling (signal type and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS1982 is an open drain part with an internal circuit equivalent to that shown in Figure 7. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 8a and 8b. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths.

A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second. If the bus master is also required to perform programming of the EPROM portions of the DS1982, a programming supply capable of delivering up to 10 milliamps at 12 volts for 480 μs is required. The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 μs, one or more of the devices on the bus may be reset.

TRANSACTION SEQUENCE

The sequence for accessing the DS1982 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read/Write Memory/Status

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1982 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

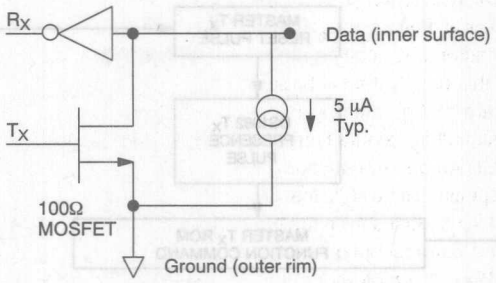
Read ROM [33H]

This command allows the bus master to read the DS1982's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can be used only if there is a single DS1982 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result).

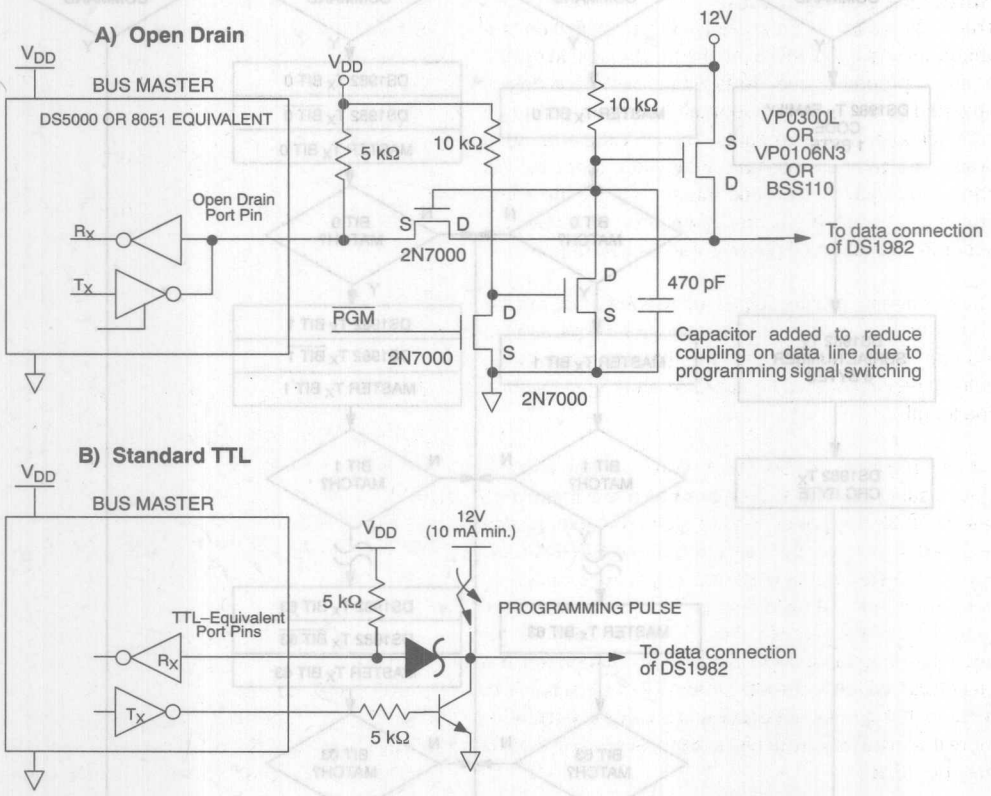
Match ROM [55H]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS1982 on a multidrop bus. Only the DS1982 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

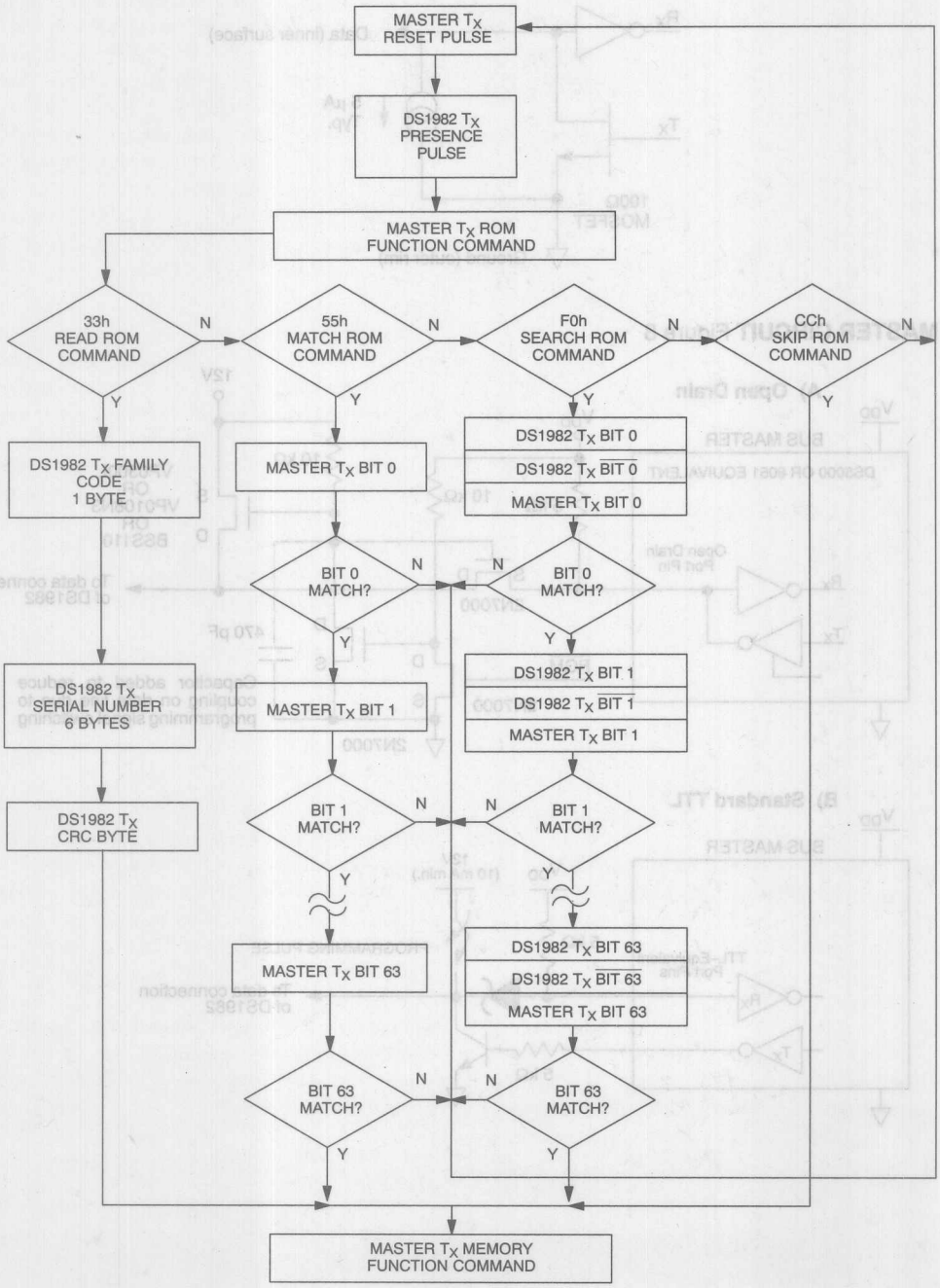
DS1982 EQUIVALENT CIRCUIT Figure 7



BUS MASTER CIRCUIT Figure 8



ROM FUNCTIONS FLOW CHART Figure 9



(SEE FIGURE 6)

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wire–AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM search, including an actual example.

1–Wire Signalling

The DS1982 requires strict protocols to insure data integrity. The protocol consists of five types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and Program Pulse. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS1982 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1982 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the 1–Wire line, the DS1982 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1982 to the master by triggering a delay circuit in the DS1982. During write time slots, the delay circuit determines when the DS1982 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1982 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8–bit scratchpad to the EPROM Data or Status Memory, a program pulse of 12 volts is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pull–up resistor to a state where the data line is actively driven to a programming voltage of 12 volts providing a minimum of 10 mA of current to the DS1982. This programming voltage (Figure 12) should be applied for 480 µs, after which the bus master returns the data line to an idle high state controlled by the pull–up resistor. Note that due to the high voltage programming requirements for any 1–Wire EPROM device, it is not possible to multi–drop non–EPROM based 1–Wire devices with the DS1982 during programming. An internal diode within the non–EPROM based 1–Wire devices will attempt to clamp the data line at approximately 8 volts and could potentially damage these devices.

CRC GENERATION

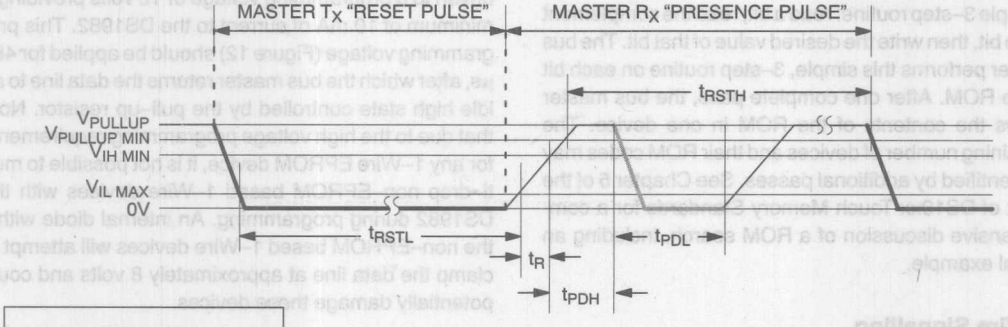
The DS1982 has an 8–bit CRC stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS1982 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$.

Under certain conditions, the DS1982 also generates an 8–bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of command, address, and data bytes from the bus master to the DS1982. The Memory Function Flow Chart of Figure 6 indicates that the DS1982 computes an 8–bit CRC for the command, address, and data bytes received for the Write Memory and the Write Status commands and then outputs this value to the bus master to confirm proper transfer. Similarly the DS1982 computes an 8–bit CRC for the command and address bytes received from the bus master

for the Read Memory, Read Status, and Read Data/ Generate 8–Bit CRC commands to confirm that these bytes have been received correctly. The CRC generator on the DS1982 is also used to provide verification of error–free data transfer as each page of data from the 1024–bit EPROM is sent to the bus master during a Read Data/Generate 8–Bit CRC command, and for the eight bytes of information in the status memory field.

In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8–bit CRC value stored in the 64–bit ROM portion of the DS1982 (for ROM reads) or the 8–bit CRC value computed within the DS1982. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS1982 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS1982 does not match the value generated by the bus master. Proper use of the CRC as outlined in the flow chart of Figure 6 can result in a communication channel with a very high level of integrity. For more details on generating CRC values including example implementations in both hardware and software, see the Book of DS19xx Touch Memory Standards.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10

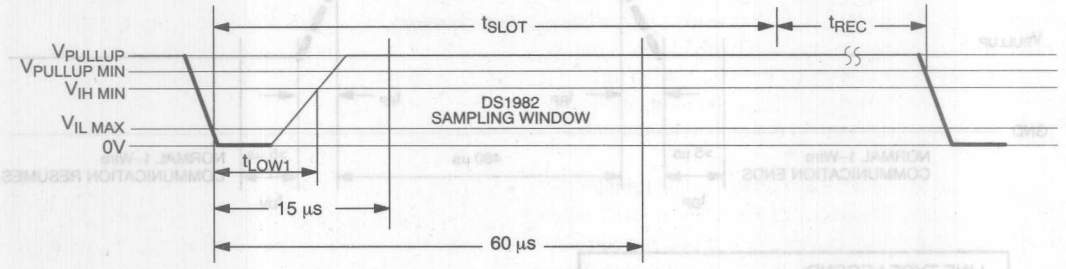


480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

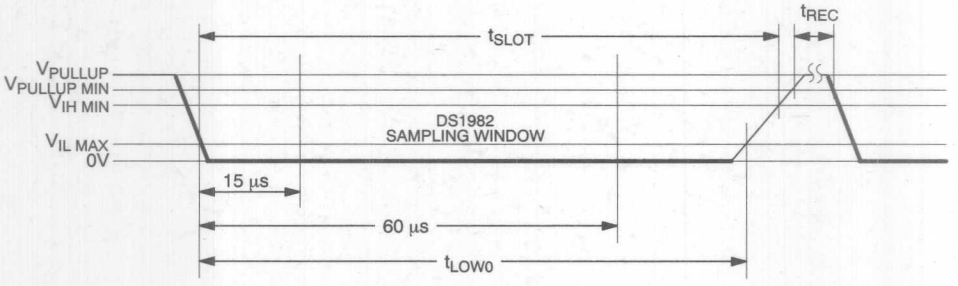
READ/WRITE TIMING DIAGRAM Figure 11

Write–one Time Slot



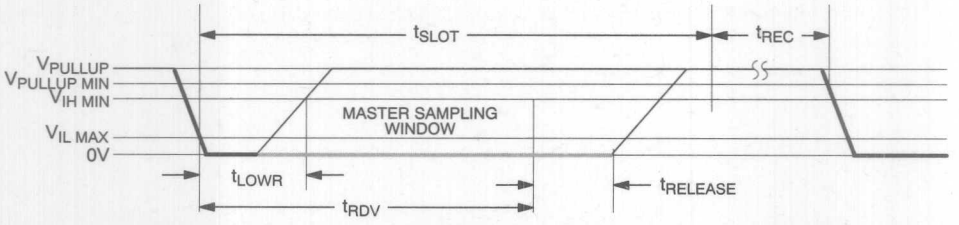
$60\ \mu s \le t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{LOW1} < 15\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

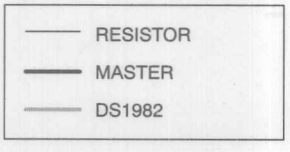
Write–zero Time Slot



$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

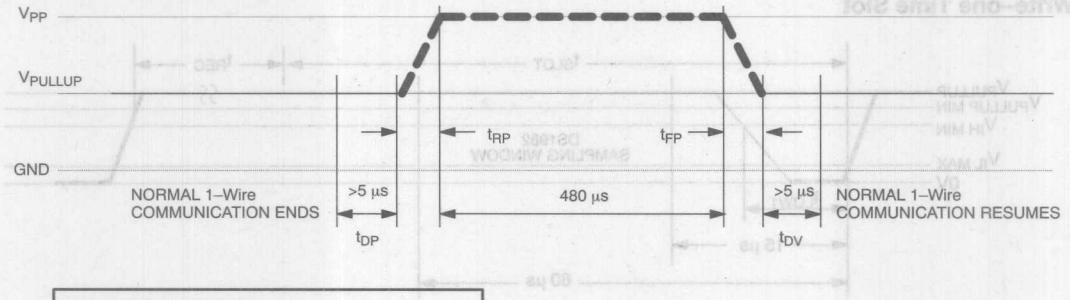
Read–data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{LOWR} < 15\ \mu s$
$0 \le t_{RELEASE} < 45\ \mu s$
$1\ \mu s \le t_{REC} < \infty$
$t_{RDV} = 15\ \mu s$

PROGRAM PULSE TIMING DIAGRAM Figure 12



LINE TYPE LEGEND:

- Bus master active high (12V @ 10 mA)
- Resistor pull–up

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +12.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Voltage @ 10 mA	V_{PP}	11.0	11.5	12.0	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Delay to Program	t_{DP}	5			µs	10
Delay to Verify	t_{DV}	5			µs	10
Program Pulse Width	t_{PP}	480			µs	10
Program Voltage Rise Time	t_{RP}	5			µs	10
Program Voltage Fall Time	t_{FP}	5			µs	10

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. Maximum 1–Wire voltage for programming parameters is 11.5V ± 0.5V; temperature range is –40°C to +85°C.

DALLAS SEMICONDUCTOR

DS1985
16Kbit Add–Only Touch Memory

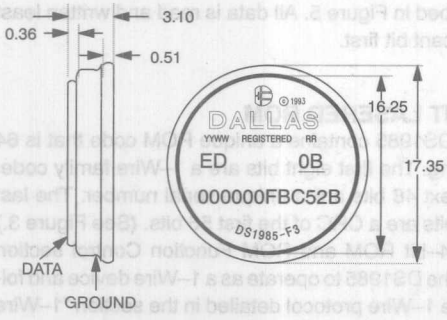
SPECIAL FEATURES

- 16384–bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- EPROM partitioned into sixty–four 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- 8–bit family code specifies DS1985 communications requirements to reader
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –20°C to +50°C

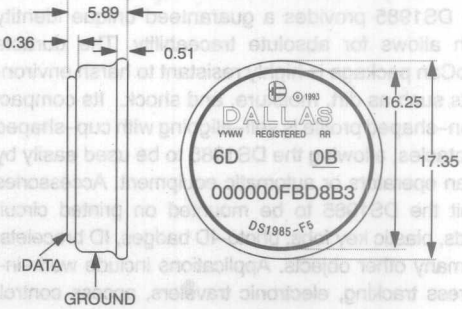
COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

F3 MICROCAN™



F5 MICROCAN™



All dimensions shown in millimeters.

ORDERING INFORMATION

DS1985–F3	F3 MicroCan
DS1985–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1985 16K–bit Add–Only Touch Memory Button™ is a rugged read/write data carrier that identifies and stores relevant information about the product or person to which it is attached. This information can be accessed with minimal hardware, for example a single port pin of a microcontroller. The DS1985 consists of a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit Family Code (0BH) plus 16K–bit of EPROM which is user–programmable. The power to program and read the DS1985 is derived entirely from the 1–Wire communication line. Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write–protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a standalone database. The 48–bit serial number that is factory–lasered into each DS1985 provides a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to harsh environments such as dirt, moisture, and shock. Its compact button–shaped profile is self–aligning with cup–shaped receptacles, allowing the DS1985 to be used easily by human operators or automatic equipment. Accessories permit the DS1985 to be mounted on printed circuit boards, plastic key fobs, photo–ID badges, ID bracelets, and many other objects. Applications include work–in–progress tracking, electronic travelers, access control, storage of calibration constants, and debit tokens.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1985. The DS1985 has three main data components: 1) 64–bit lasered ROM, 2) 16384–bits EPROM Data Memory, and 3) 704–bits EPROM Status Memory. The device derives its power for read operations entirely from the 1–Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1–Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1–Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1–Wire line a special high voltage detect circuit within the DS1985 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1–Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 8. After a ROM Function Command is successfully executed, the memory functions that operate on the EPROM portions of the DS1985 become accessible and the bus master may issue any one of the five Memory Function Commands specific to the DS1985 to read or program the various data fields. The protocol for these Memory Function Commands is described in Figure 5. All data is read and written least significant bit first.

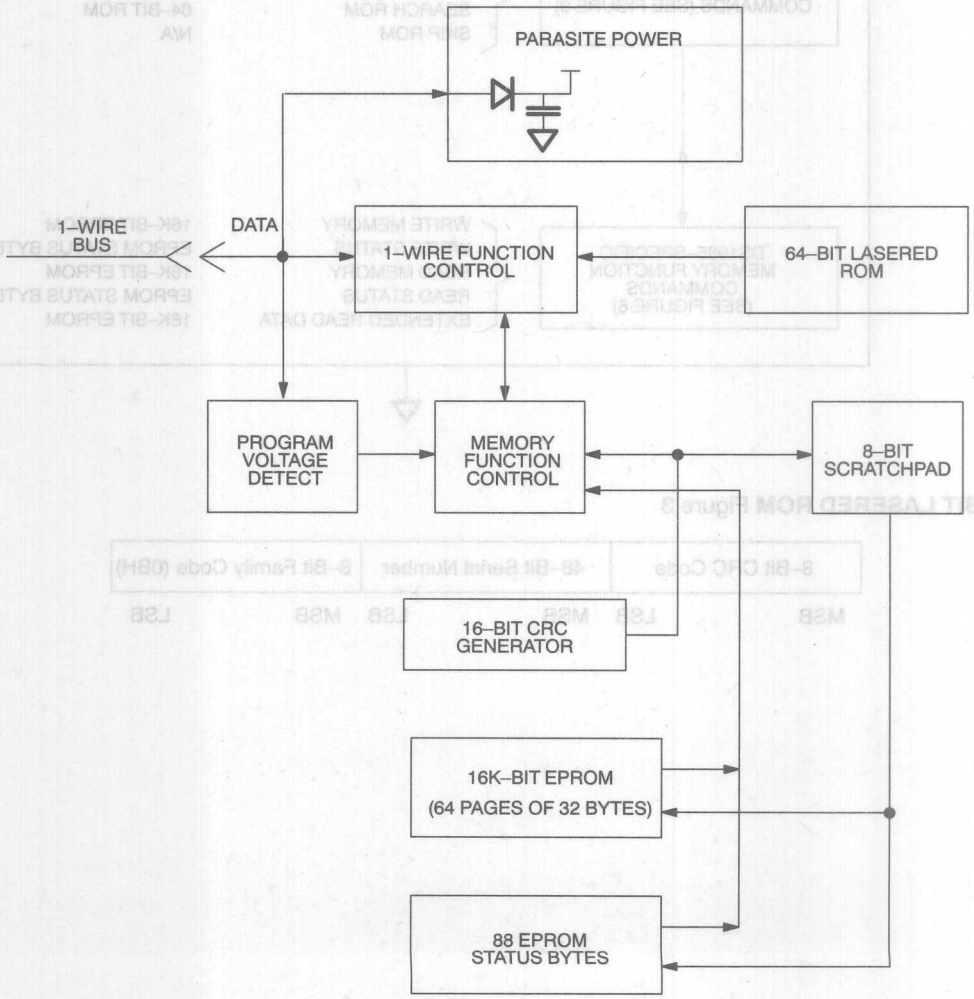
64–BIT LASERED ROM

Each DS1985 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 64–bit ROM and ROM Function Control section allow the DS1985 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The memory functions required to read

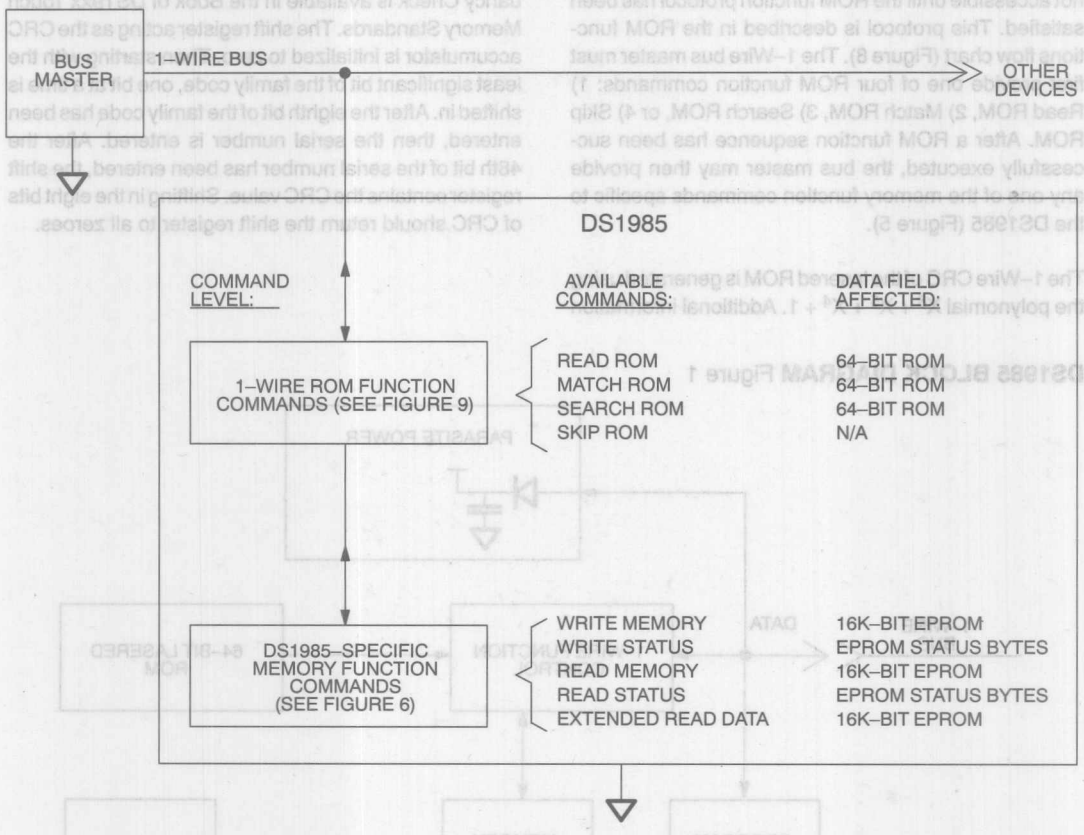
and program the EPROM sections of the DS1985 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 8). The 1–Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS1985 (Figure 5).

The 1–Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards. The shift register acting as the CRC accumulator is initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the eighth bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeroes.

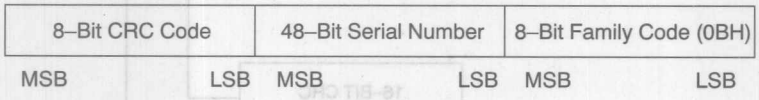
DS1985 BLOCK DIAGRAM Figure 1



HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2



64–BIT LASERED ROM Figure 3



16384–BITS EPROM

The memory map in Figure 4 shows the 16384–bits EPROM section of the DS1985 which is configured as sixty–four pages of 32 bytes each. The 8–bit scratchpad is an additional register that acts as a buffer when programming the memory. Data is first written to the scratchpad and then verified by reading an 16–bit CRC from the DS1985 that confirms proper receipt of the data and address. If the buffer contents are correct, a programming voltage should be applied and the byte of data will be written into the selected address in memory. This process insures data integrity when programming the memory. The details for reading and programming the 16384–bits EPROM portion of the DS1985 are given in the Memory Function Commands section.

EPROM STATUS BYTES

In addition to the 16384 bits of data memory the DS1985 provides 704 bits of Status Memory accessible with separate commands.

The EPROM Status Bytes can be read or programmed to indicate various conditions to the software interrogating the DS1985. The first eight bytes of the EPROM Status Memory (addresses 000 to 007H) contain the Write Protect Page bits which inhibit programming of the corresponding page in the 16384–bit main memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page section of the Status Memory, the entire 32 byte page that corresponds to that bit can no longer be altered but may still be read.

The next eight bytes of the EPROM Status Memory (addresses 020 to 027H) contain the Write Protect bits which inhibit altering the Page Address Redirection Byte corresponding to each page in the 16384–bit main memory area.

The following eight bytes within the EPROM Status Memory (addresses 040 to 047H) are reserved for use by the Touch Memory EXecutive TMEX. Their purpose is to indicate which memory pages are already in use. Originally, all of these bits are unprogrammed, indicating that the device does not store any data. As soon as data is written to any page of the device under control of TMEX, the bit inside this bitmap corresponding to that page will be programmed to 0, marking this page as used. These bits are application flags only and have no impact on the internal logic of the DS1985.

The next sixty–four bytes of the EPROM Status Memory (addresses 100H to 13FH) contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 16384–bits EPROM section have been invalidated by software and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS1985 makes no decisions based on the contents of the Page Address Redirection Bytes. These additional bytes of Status EPROM allow for the redirection of an entire page to another page address, indicating that the data in the original page is no longer considered relevant or valid. With EPROM technology, bits within a page can be changed from a logical 1 to a logical 0 by programming, but cannot be changed back. Therefore, it is not possible to simply rewrite a page if the data requires changing or updating, but with space permitting, an entire page of data can be redirected to another page within the DS1985 by writing the one's complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page.

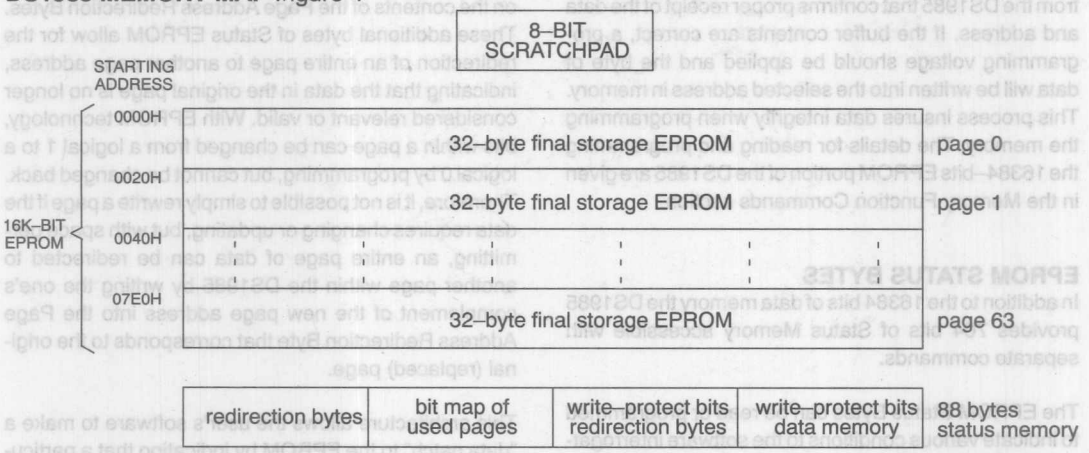
This architecture allows the user's software to make a "data patch" to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes. To leave an authentic audit trail of data patches, it is recommended to also program the write protect bit of the Page Address Redirection Byte, after the page redirection is programmed. Without this protection, it is still possible to modify the Page Address Redirection Byte, making it point to a different memory page than the true one.

If a Page Address Redirection Byte has a FFH value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value, the data in the page corresponding to that redirection byte is invalid, and the valid data can now be found at the one's complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDH in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. The details for reading and programming the EPROM status memory portion of the DS1985 are given in the Memory Function Commands section.

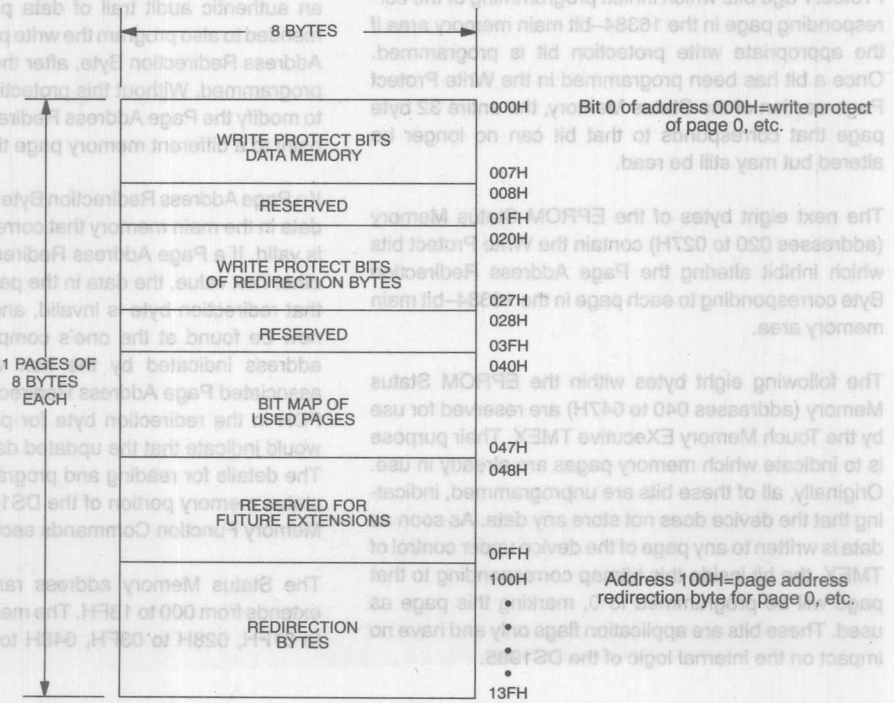
The Status Memory address range of the DS1985 extends from 000 to 13FH. The memory locations 008H to 01FH, 028H to 03FH, 048H to 0FFH and 140H to

7FFH are physically not implemented. Reading these locations will usually result in FFH bytes. Attempts to write to these locations will be ignored. If the bus master sends a starting address higher than 7FFH, the five most significant address bits are set to zeros by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS1985 and the CRC calculated by the bus master, indicating an error condition.

DS1985 MEMORY MAP Figure 4



STATUS MEMORY MAP



MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 5) describes the protocols necessary for accessing the various data fields within the DS1985. The Memory Function Control section, 8–bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three–byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field. The command byte indicates if the device is to be read or written. Writing data involves not only issuing the correct command sequence but also providing a 12–volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS1985 and received back by the bus master are sent least significant bit first.

READ MEMORY [F0H]

The Read Memory command is used to read data from the 16384–bits EPROM data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With every subsequent read data time slot the bus master receives data from the DS1985 starting at the initial address and continuing until the end of the 16384–bits data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue sixteen additional read time slots and the DS1985 will respond with a 16–bit CRC of the command, address bytes and all data bytes read from the initial starting byte through the last byte of memory. This CRC is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes and the data bytes beginning at the first addressed memory location and continuing through to the last byte of the EPROM data memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 16–bit CRC available.

Typically a 16–bit CRC would be stored with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Book of DS19xx Touch Memory Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment.) If CRC values are imbedded within the data, a Reset Pulse may be issued at the end of memory space during a Read Memory command.

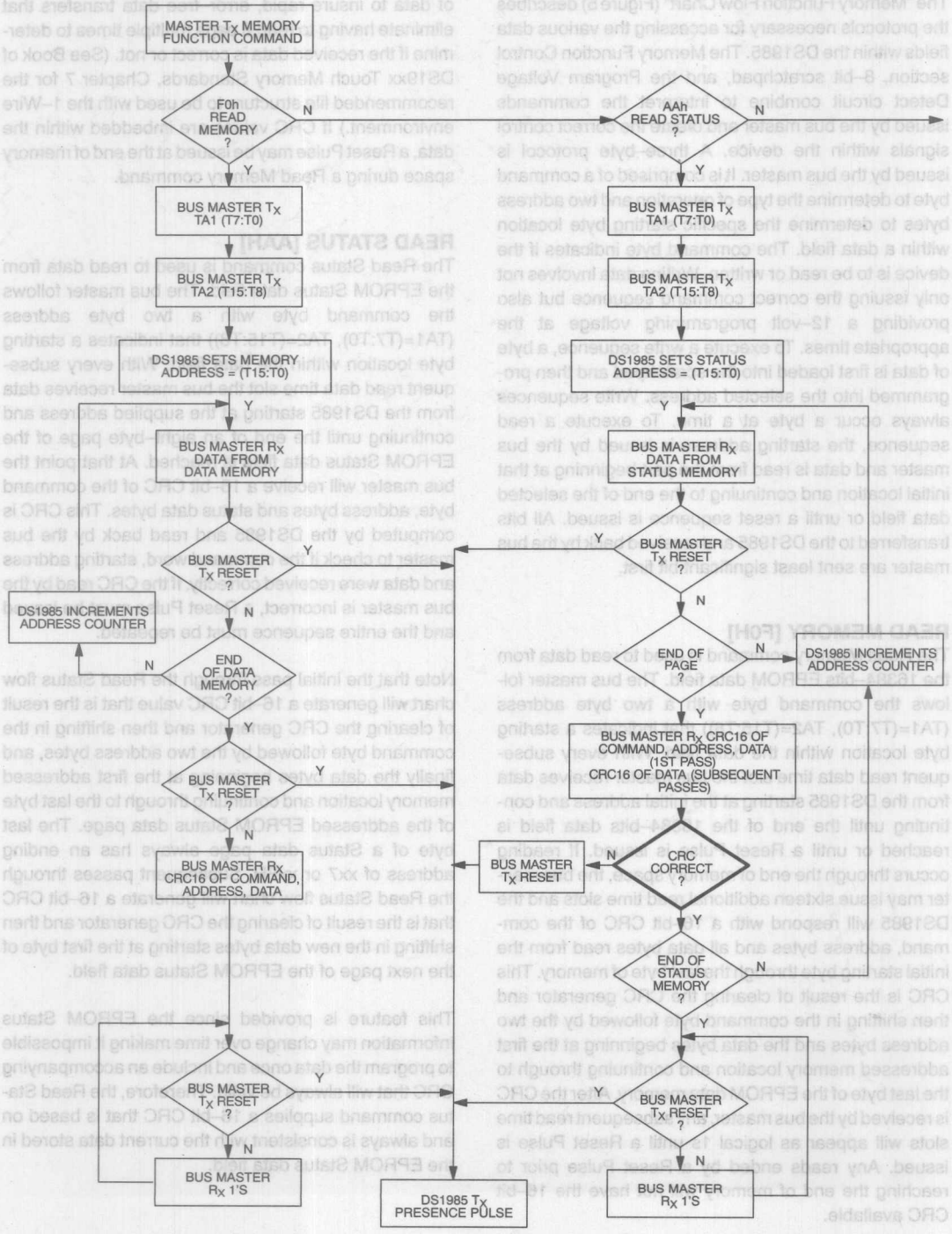
READ STATUS [AAH]

The Read Status command is used to read data from the EPROM Status data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With every subsequent read data time slot the bus master receives data from the DS1985 starting at the supplied address and continuing until the end of an eight–byte page of the EPROM Status data field is reached. At that point the bus master will receive a 16–bit CRC of the command byte, address bytes and status data bytes. This CRC is computed by the DS1985 and read back by the bus master to check if the command word, starting address and data were received correctly. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated.

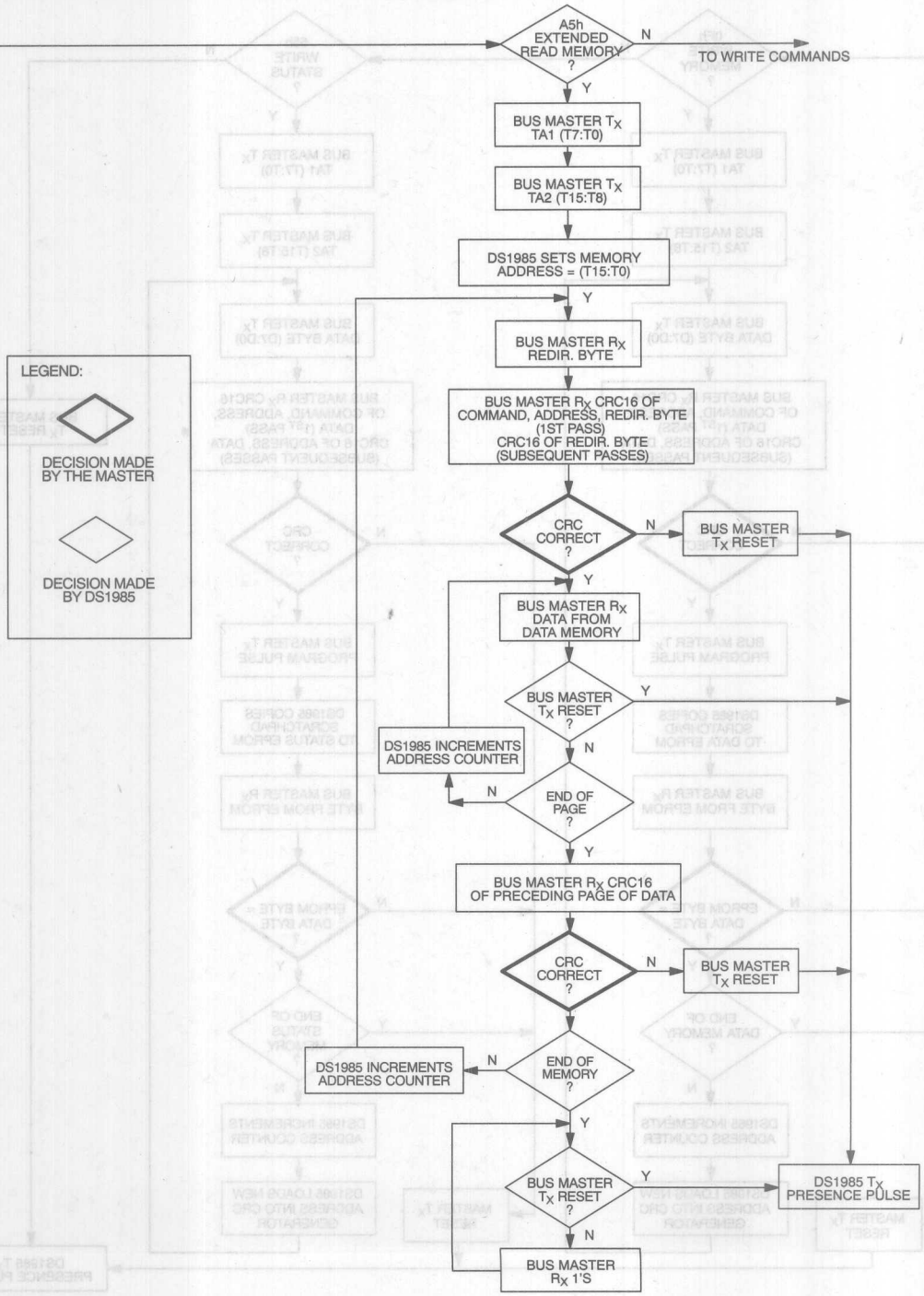
Note that the initial pass through the Read Status flow chart will generate a 16–bit CRC value that is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes, and finally the data bytes beginning at the first addressed memory location and continuing through to the last byte of the addressed EPROM Status data page. The last byte of a Status data page always has an ending address of xx7 or xxFH. Subsequent passes through the Read Status flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes starting at the first byte of the next page of the EPROM Status data field.

This feature is provided since the EPROM Status information may change over time making it impossible to program the data once and include an accompanying CRC that will always be valid. Therefore, the Read Status command supplies a 16–bit CRC that is based on and always is consistent with the current data stored in the EPROM Status data field.

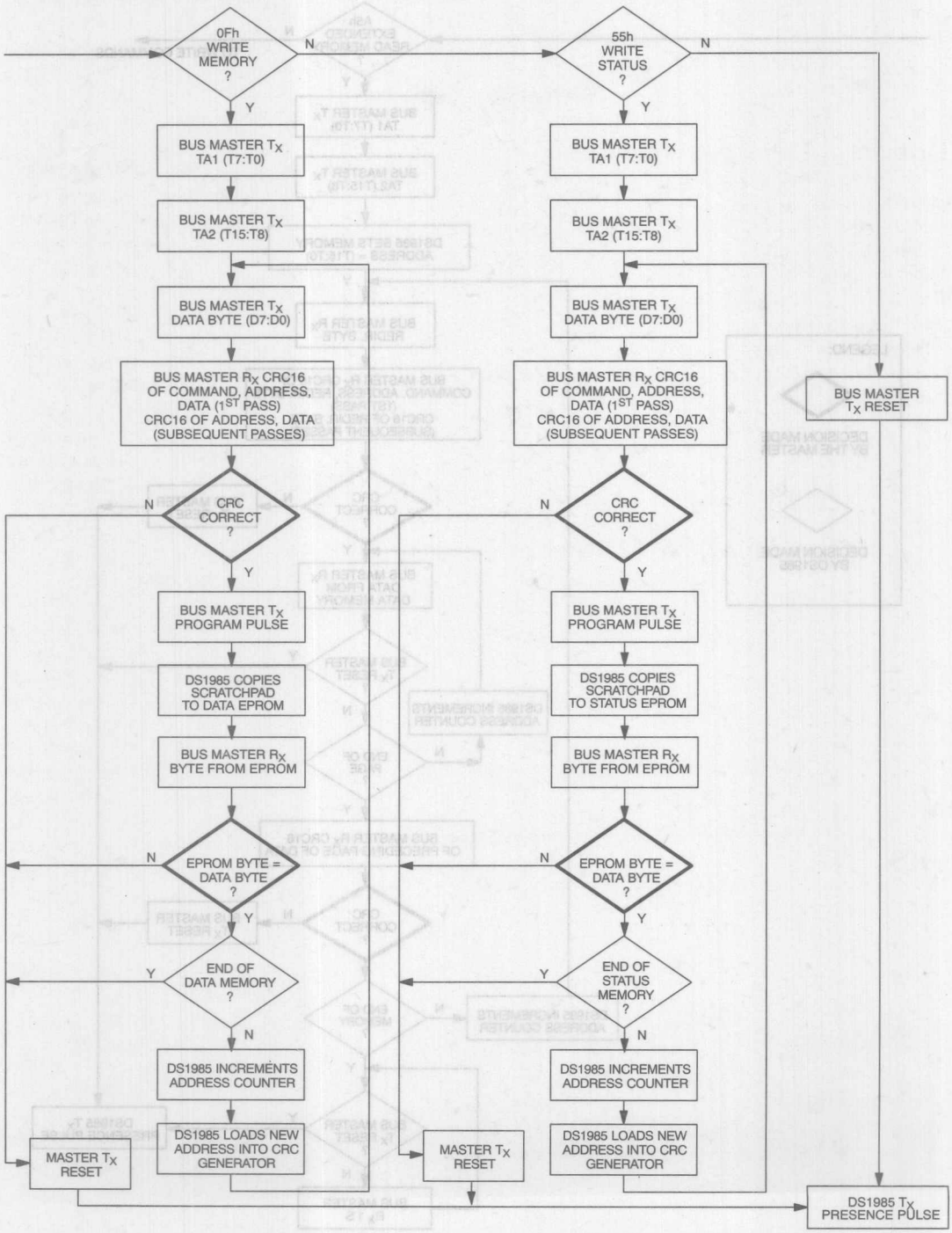
MEMORY FUNCTION FLOW CHART Figure 5



MEMORY FUNCTION FLOW CHART (cont'd) Figure 5



MEMORY FUNCTION FLOW CHART (cont'd) Figure 5



After the 16–bit CRC of the last EPROM Status data page is read, the bus master will receive logical 1s from the DS1985 until a Reset Pulse is issued. The Read Status command sequence can be ended at any point by issuing a Reset Pulse.

EXTENDED READ MEMORY [A5H]

The Extended Read Memory command supports page redirection when reading data from the 16384–bit EPROM data field. One major difference between the Extended Read Memory and the basic Read Memory command is that the bus master receives the Redirection Byte first before investing time in reading data from the addressed memory location. This allows the bus master to quickly decide whether to continue and access the data at the selected starting page or to terminate and restart the reading process at the redirected page address. A non–redirected page is identified by a Redirection Byte with a value of FFH (see description of EPROM Status Bytes). If the Redirection Byte is different than this, the master has to complement it to obtain the new page number. Multiplying the page number by 32 (20H) results in the new address the master has to send to the DS1985 to read the updated data replacing the old data. There is no logical limitation in the number of redirections of any page. The only limit is the number of available memory pages within the DS1985.

In addition to page redirection, the Extended Read Memory command also supports "bit–oriented" applications where the user cannot store a 16–bit CRC with the data itself. With bit–oriented applications the EPROM information may change over time within a page boundary making it impossible to include an accompanying CRC that will always be valid. Therefore, the Extended Read Memory command concludes each page with the DS1985 generating and supplying a 16–bit CRC that is based on and therefore always consistent with the current data stored in each page of the 16384–bit EPROM data field.

After having sent the command code of the Extended Read Memory command, the bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. By sending eight read data time slots, the master receives the Redirection Byte associated with the page given by the starting address. With the next sixteen read data time slots, the bus master receives a 16–bit CRC of the command byte, address bytes and the Redirection Byte. This CRC is computed by the DS1985 and read back by the bus master to check if the command word, starting address and Redirection Byte were received correctly.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS1985 starting at the initial address and continuing until the end of a 32–byte page is reached. At that point the bus master will send sixteen additional read time slots and receive a 16–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page.

With the next 24 read data time slots the master will receive the Redirection Byte of the next page followed by a 16–bit CRC of the Redirection Byte. After this, data is again read from the 16384–bit EPROM data field starting at the beginning of the new page. This sequence will continue until the final page and its accompanying CRC are read by the bus master.

The Extended Read Memory command provides a 16–bit CRC at two locations within the transaction flow chart: 1) after the Redirection Byte and 2) at the end of each memory page. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. The CRC received by the bus master directly following the Redirection Byte, is calculated in two different ways. With the initial pass through the Extended Read Memory flow chart the 16–bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only.

After the 16–bit CRC of the last page is read, the bus master will receive logical 1s from the DS1985 until a Reset Pulse is issued. The Extended Read Memory command sequence can be ended at any point by issuing a Reset Pulse.

WRITE MEMORY [0FH]

The Write Memory command is used to program the 16384–bit EPROM data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). A 16–bit CRC of the command byte, address bytes, and data byte is computed by the DS1985 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

The highest starting address within the DS1985 is 07FFH. If the bus master sends a starting address higher than this, the five most significant address bits are set to zero by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS1985 and the CRC calculated by the bus master, indicating an error condition.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 μs) is issued by the bus master. Prior to programming, the entire unprogrammed 16384–bit EPROM data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the 16384–bit EPROM will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480 μs programming pulse is applied and the data line returns to the idle level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS1985 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM data address. If the EPROM data byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS1985 EPROM data byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS1985 will automatically increment its address counter to select the next byte in the 16384–bit EPROM data field. The new two–byte address will also be loaded into the 16–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots. As the DS1985 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16–bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16–bit CRC from the DS1985 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Memory command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Memory flow chart will generate a 16–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Memory flow chart due to the DS1985 automatically incrementing its address counter will generate a 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS1985) is made entirely by the bus master, since the DS1985 will not be able to determine if the 16–bit CRC calculated by the bus master agrees with the 16–bit CRC calculated by the DS1985. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS1985. Also note that the DS1985 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Memory command, incorrect programming could occur within the DS1985. The Write Memory command sequence can be ended at any point by issuing a Reset Pulse.

To save time when writing more than one consecutive byte of the DS1985's data memory it is possible to omit reading the 16–bit CRC which allows verification of data and address before the data is copied to the EPROM memory. This saves 16 time slots or 976 μs for every byte to be programmed. This speed–programming

mode is accessed with the command code F3H instead of 0FH. It follows basically the same flow chart as the Write Memory command, but skips sending the CRC immediately preceding the program pulse. This command should only be used if the electrical contact between bus master and the DS1985 is firm since a poor contact may result in corrupted data inside the EPROM memory.

WRITE STATUS [55H]

The Write Status command is used to program the EPROM Status data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of status data (D7:D0). A 16–bit CRC of the command byte, address bytes, and data byte is computed by the DS1985 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 μs) is issued by the bus master. Prior to programming, the EPROM Status data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM Status data field will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480 μs programming pulse is applied and the data line returns to the idle level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS1985 responds with the data from the selected EPROM Status address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM Status Byte address. If the EPROM Status Byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS1985 EPROM Status byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS1985 will automatically increment its address counter to select the next byte in the EPROM Status data field. The new two–byte address will also be loaded into the 16–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS1985 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16–bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16–bit CRC from the DS1985 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Status flow chart will generate a 16–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Status flow chart due to the DS1985 automatically incrementing its address counter will generate a 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS1985) is made entirely by the bus master, since the DS1985 will not be able to determine if the 16–bit CRC calculated by the bus master agrees with the 16–bit CRC calculated by the DS1985. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS1985. Also note that the DS1985 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Status command, incorrect programming could occur within the DS1985. The Write Status command sequence can be ended at any point by issuing a Reset Pulse.

To save time when writing more than one consecutive byte of the DS1985's status memory it is possible to omit reading the 16–bit CRC which allows verification of data and address before the data is copied to the EPROM memory. This saves 16 time slots or 976 μs for every byte to be programmed. This speed–programming mode is accessed with the command code F5H instead of 55H. It follows basically the same flow chart as the

Write Status command, but skips sending the CRC immediately preceding the program pulse. This command should only be used if the electrical contact between bus master and the DS1985 is firm since a poor contact may result in corrupted data inside the EPROM status memory.

1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS1985 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signalling (signal type and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS1985 is an open drain part with an internal circuit equivalent to that shown in Figure 6. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 7a and 7b. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths.

A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second. If the bus master is also required to perform programming of the EPROM portions of the DS1985, a programming supply capable of delivering up to 10 milliamps at 12 volts for 480 µs is required. The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

Transaction Sequence

The sequence for accessing the DS1985 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read/Write Memory/Status

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1985 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

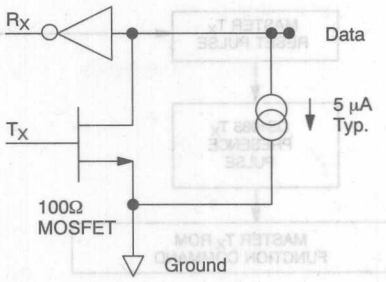
ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 8):

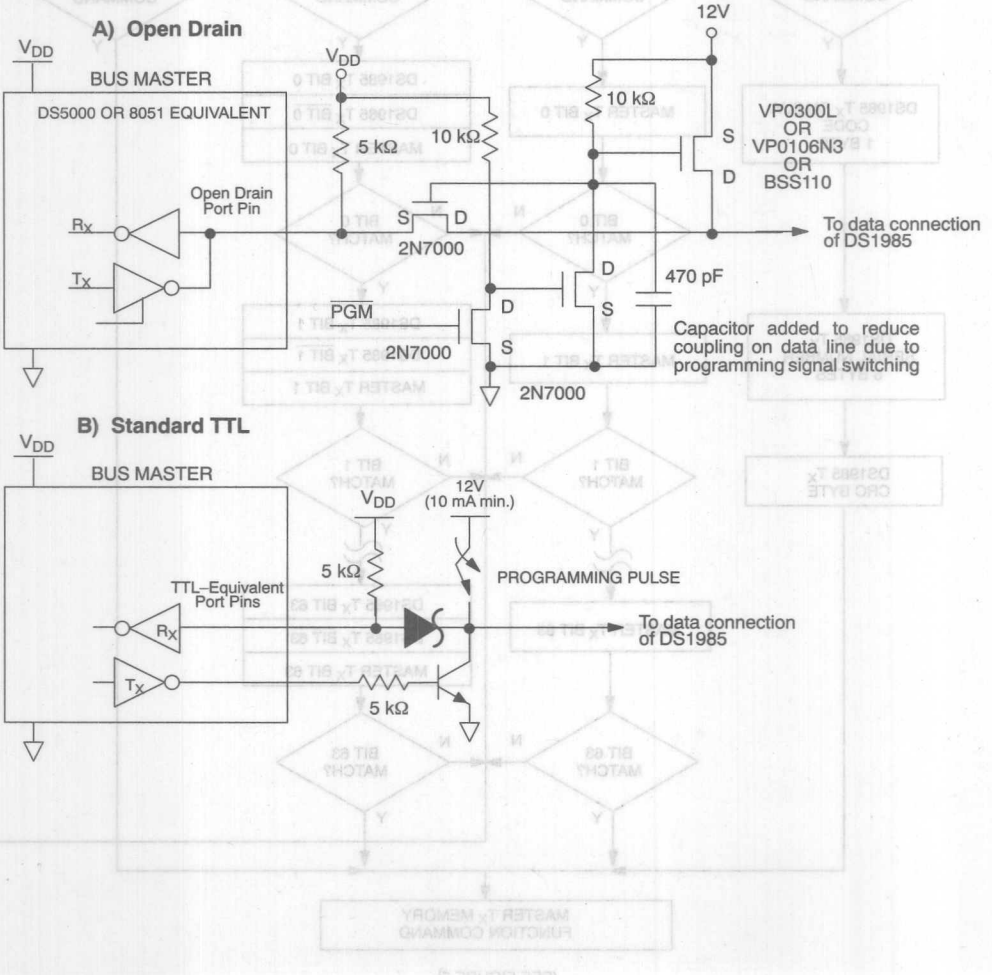
Read ROM [33H]

This command allows the bus master to read the DS1985's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can be used only if there is a single DS1985 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result).

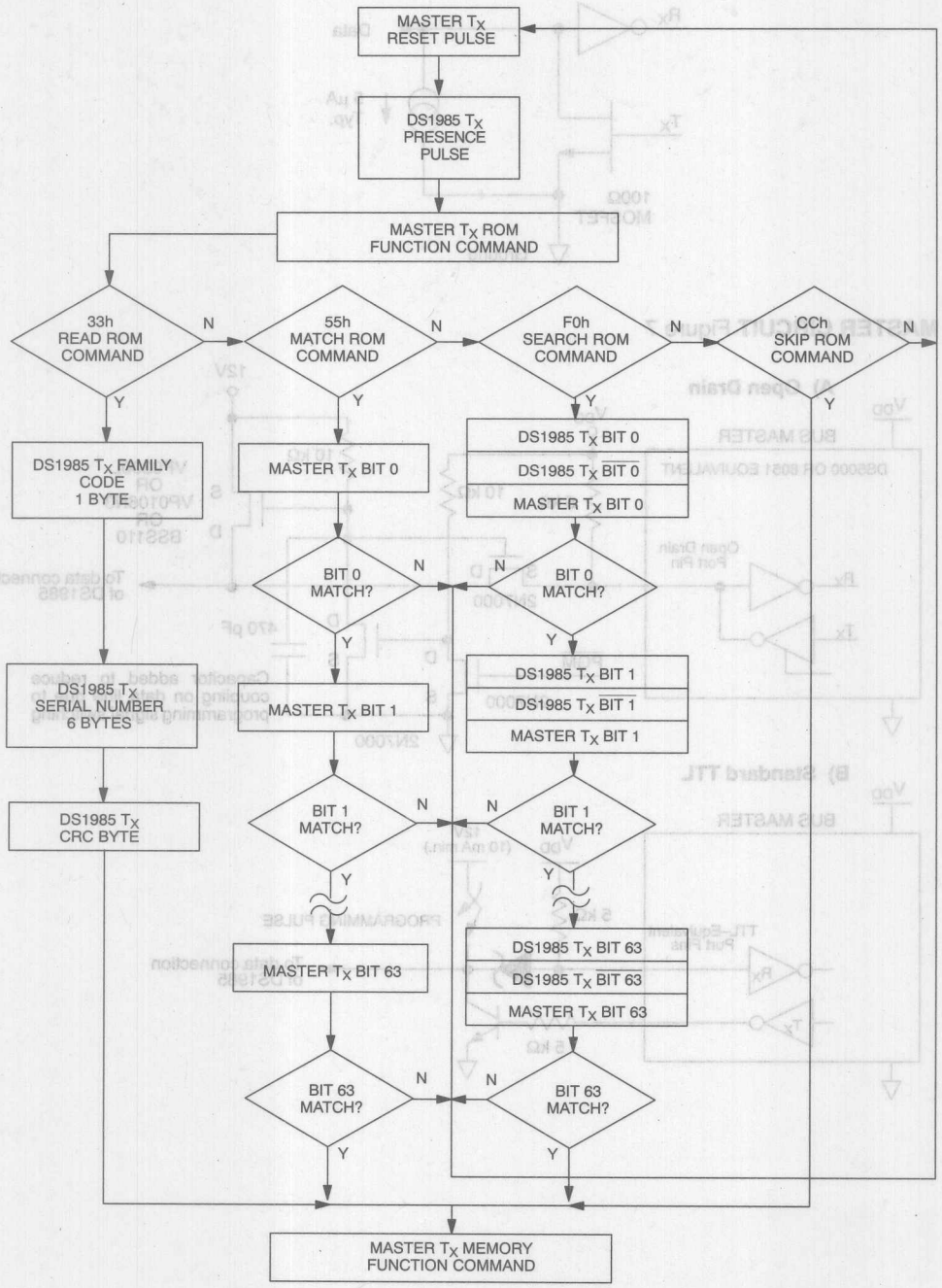
DS1985 EQUIVALENT CIRCUIT Figure 6



BUS MASTER CIRCUIT Figure 7



ROM FUNCTIONS FLOW CHART Figure 8



Match ROM [55H]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS1985 on a multidrop bus. Only the DS1985 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM search, including an actual example.

1–Wire Signalling

The DS1985 requires strict protocols to insure data integrity. The protocol consists of five types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and Program Pulse. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS1985 is shown in Figure 9. A reset pulse followed by a presence pulse indicates the DS1985 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data pin, the DS1985 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

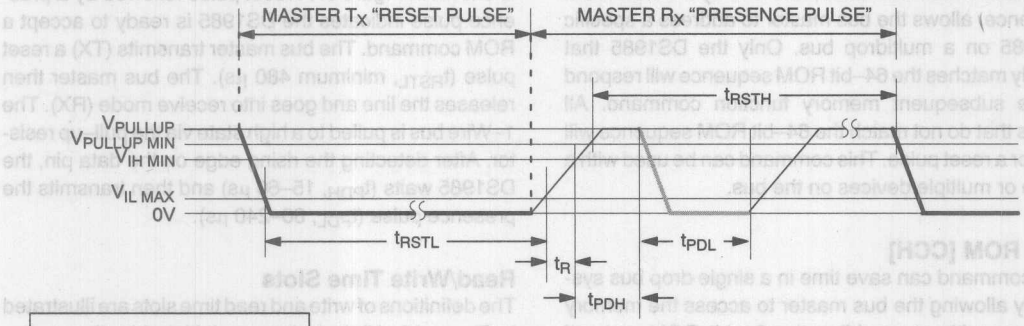
Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 10. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1985 to the master by triggering a delay circuit in the DS1985. During write time slots, the delay circuit determines when the DS1985 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1985 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8–bit scratchpad to the EPROM Data or Status Memory, a program pulse of 12 volts is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pull–up resistor to a state where the data line is actively driven to a programming voltage of 12 volts providing a minimum of 10 mA of current to the DS1985. This programming voltage (Figure 11) should be applied for 480 µs, after which the bus master returns the data line to an idle high state controlled by the pull–up resistor. Note that due to the high voltage programming requirements for any 1–Wire EPROM device, it is not possible to multi–drop non–EPROM based 1–Wire devices with the DS1985 during programming. An internal diode within the non–EPROM based 1–Wire devices will attempt to clamp the data line at approximately 8 volts and could potentially damage these devices.

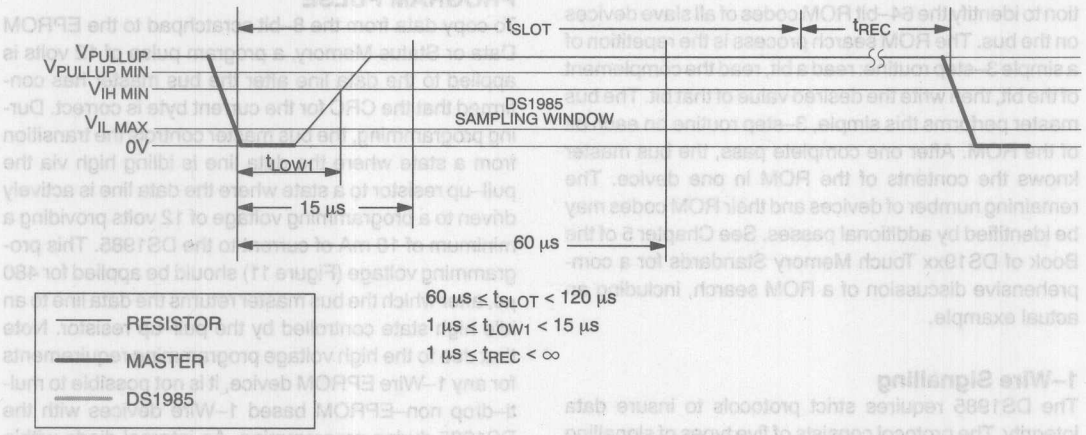
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

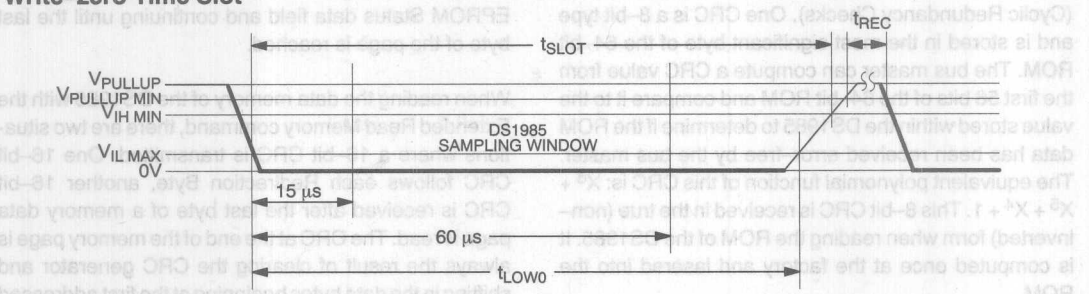
READ/WRITE TIMING DIAGRAM Figure 10

Write–one Time Slot



READ/WRITE TIMING DIAGRAM (cont'd) Figure 10

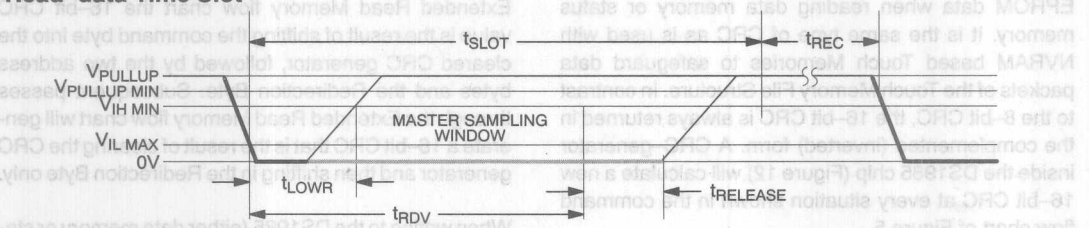
Write–zero Time Slot



$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–data Time Slot



RESISTOR
MASTER
DS1985

$60\ \mu s \le t_{SLOT} < 120\ \mu s$

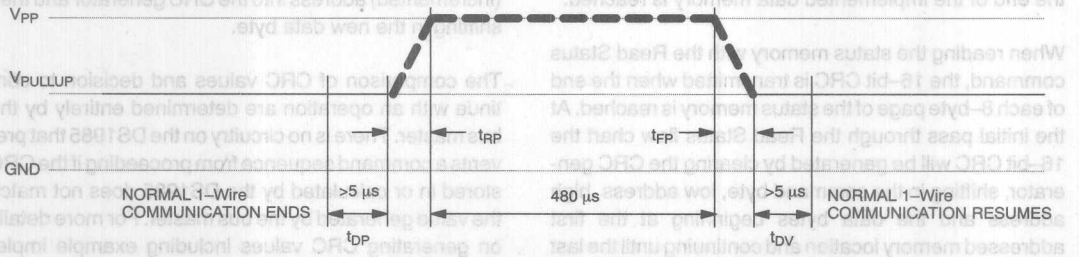
$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

PROGRAM PULSE TIMING DIAGRAM Figure 11



LINE TYPE LEGEND:

Bus master active high (12V @ 10 mA)

Resistor pull–up

CRC GENERATION

With the DS1985 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is a 8–bit type and is stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS1985 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8–bit CRC is received in the true (non–inverted) form when reading the ROM of the DS1985. It is computed once at the factory and lasered into the ROM.

The other CRC is a 16–bit type, generated according to the standardized CRC16–polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used to safeguard user–defined EPROM data when reading data memory or status memory. It is the same type of CRC as is used with NVRAM based Touch Memories to safeguard data packets of the Touch Memory File Structure. In contrast to the 8–bit CRC, the 16–bit CRC is always returned in the complemented (inverted) form. A CRC–generator inside the DS1985 chip (Figure 12) will calculate a new 16–bit CRC at every situation shown in the command flow chart of Figure 5.

The DS1985 provides this CRC–value to the bus master to validate the transfer of command, address, and data to and from the bus master. When reading the data memory of the DS1985 with the Read Memory command, the 16–bit CRC is only transmitted as the end of the memory is reached. This CRC is generated by clearing the CRC generator, shifting in the command, low address, high address and every data byte starting at the first addressed memory location and continuing until the end of the implemented data memory is reached.

When reading the status memory with the Read Status command, the 16–bit CRC is transmitted when the end of each 8–byte page of the status memory is reached. At the initial pass through the Read Status flow chart the 16–bit CRC will be generated by clearing the CRC generator, shifting in the command byte, low address, high address and the data bytes beginning at the first addressed memory location and continuing until the last byte of the addressed EPROM Status data page is reached. Subsequent passes through the Read Status flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes starting at the first byte of the next page of the EPROM Status data field and continuing until the last byte of the page is reached.

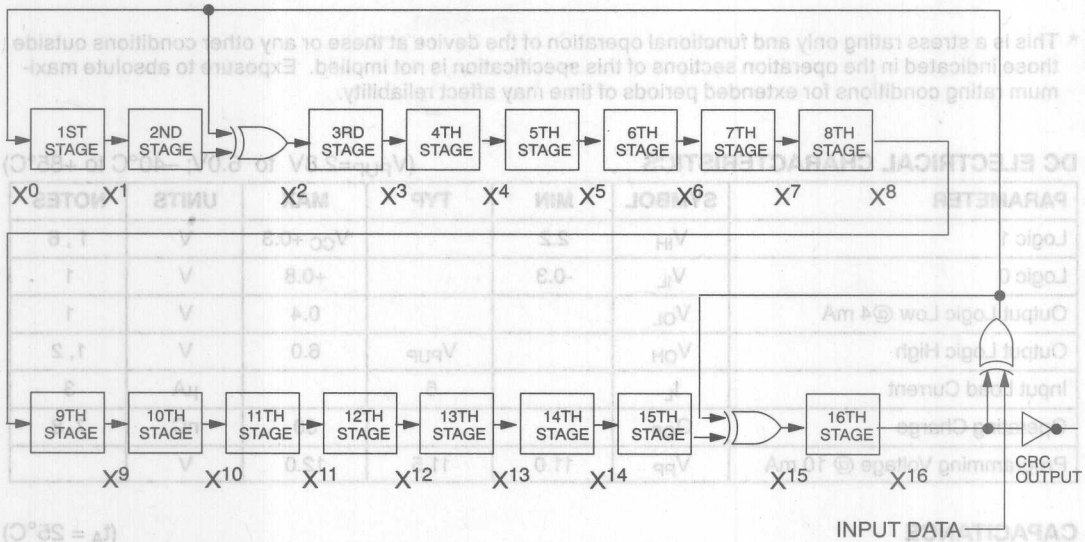
When reading the data memory of the DS1985 with the Extended Read Memory command, there are two situations where a 16–bit CRC is transmitted. One 16–bit CRC follows each Redirection Byte, another 16–bit CRC is received after the last byte of a memory data page is read. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. The CRC received by the bus master directly following the Redirection Byte, is calculated in two different ways. With the initial pass through the Extended Read Memory flow chart the 16–bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only.

When writing to the DS1985 (either data memory or status memory), the bus master receives a 16–bit CRC to verify the correctness of the data transfer before applying the programming pulse. With the initial pass through the Write Memory/Status flow chart the 16–bit CRC will be generated by clearing the CRC–generator, shifting in the command, address low, address high and the data byte. Subsequent passes through the Write Memory/Status flow chart due to the DS1985 automatically incrementing its address counter will generate an 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS1985 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS1985 does not match the value generated by the bus master. For more details on generating CRC values including example implementations in both hardware and software, see the Book of DS19xx Touch Memory Standards.

CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 22

Polynomial = $X^{16} + X^{15} + X^2 + 1$



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +12.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1 , 6
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Voltage @ 10 mA	V_{PP}	11.0	11.5	12.0	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	9

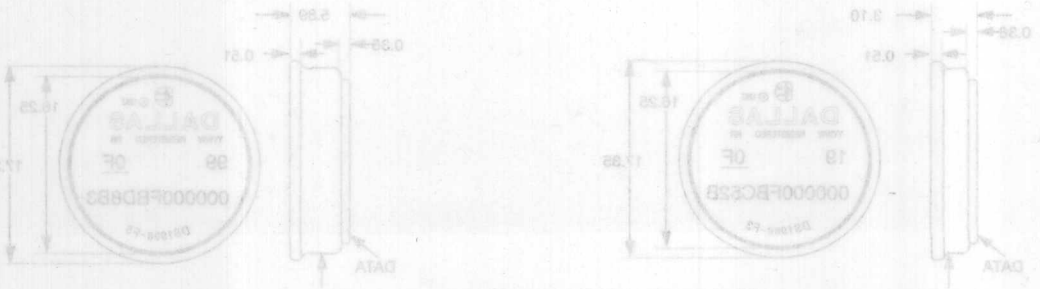
AC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Delay to Program	t_{DP}	5			µs	10
Delay to Verify	t_{DV}	5			µs	10
Program Pulse Width	t_{PP}	480			µs	10
Program Voltage Rise Time	t_{RP}	5			µs	10
Program Voltage Fall Time	t_{FP}	5			µs	10

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. Maximum 1–Wire voltage for programming parameters is 11.5V ± 0.5V; temperature range is –20°C to +50°C.



PRELIMINARY

DALLAS SEMICONDUCTOR

DS1986
64Kbit Add–Only Touch Memory

SPECIAL FEATURES

- 65536–bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- EPROM partitioned into two hundred and fifty–six 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- 8–bit family code specifies DS1986 communications requirements to reader
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –20°C to +50°C

COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

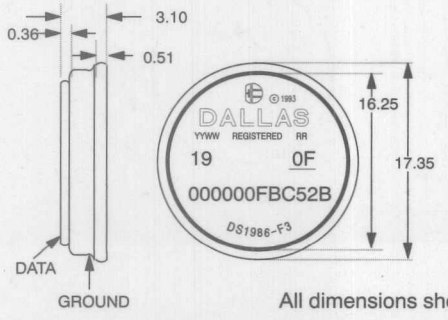
ORDERING INFORMATION

DS1986–F3	F3 MicroCan
DS1986–F5	F5 MicroCan

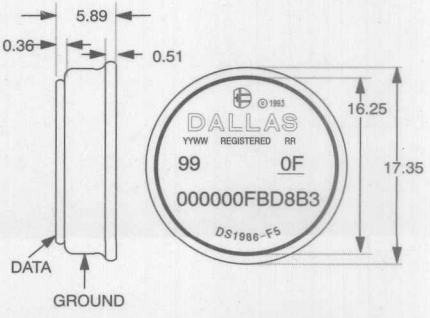
SILICON LABEL™ DESCRIPTION

The DS1986 Add–Only Touch Memory Button™ operates nearly identically to the DS1985. The main differences are: 64K bit of memory organized as 256 pages of 32 bytes and a family code of 0F hexadecimal. For further details please refer to the DS1985 data sheet.

F3 MICROCAN™



F5 MICROCAN™



All dimensions shown in millimeters.

DALLAS SEMICONDUCTOR

DS1920
Touch Thermometer

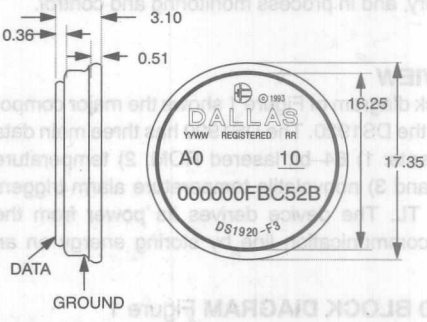
SPECIAL FEATURES

- Digital thermometer measures temperatures from –55°C to +100°C in typically 1 second
- Accuracy ±0.5°C within 0°C to +70°C, no calibration or reference required
- Zero standby power
- 0.5°C resolution, digital temperature reading is two's complement of °C value
- Access to internal counters allows increased resolution through interpolation
- Reduces control, address, data, and power to a single data contact
- 8–bit device–generated CRC for data integrity
- 8–bit family code specifies DS1920 communications requirements to reader
- Special command set allows user to skip ROM section and do temperature measurements simultaneously for all devices on the bus
- Two bytes of EEPROM to be used either as alarm triggers or user memory
- Alarm search directly indicates which device senses alarming temperatures

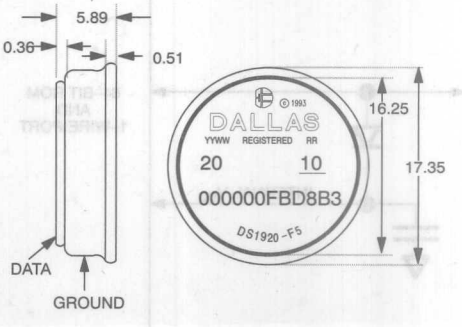
COMMON TOUCH MEMORY FEATURES

- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN™
- Digital identification and information by momentary contact
- Chip–based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Touch Memory family
- Button shape is self–aligning with cup–shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self–stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

F3 MICROCAN™



F5 MICROCAN™



All dimensions are shown in millimeters.

DS1920–F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self–Stick Adhesive Pad
DS9101	Multi–Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap–In Fob
DS9092	Touch Memory Probe

SILICON LABEL™ DESCRIPTION

The DS1920 Touch Thermometer™ provides 9–bit temperature readings which indicate the temperature of the device.

Information is sent to/from the DS1920 over a 1–Wire interface. Power for reading, writing, and performing temperature conversions is derived from the data line itself. Because each DS1920 contains a unique silicon serial number, multiple DS1920s can exist on the same 1–Wire bus. This allows for placing temperature sensors in many different places. Applications where this feature is useful include HVAC environmental controls, sensing temperatures inside buildings, equipment or machinery, and in process monitoring and control.

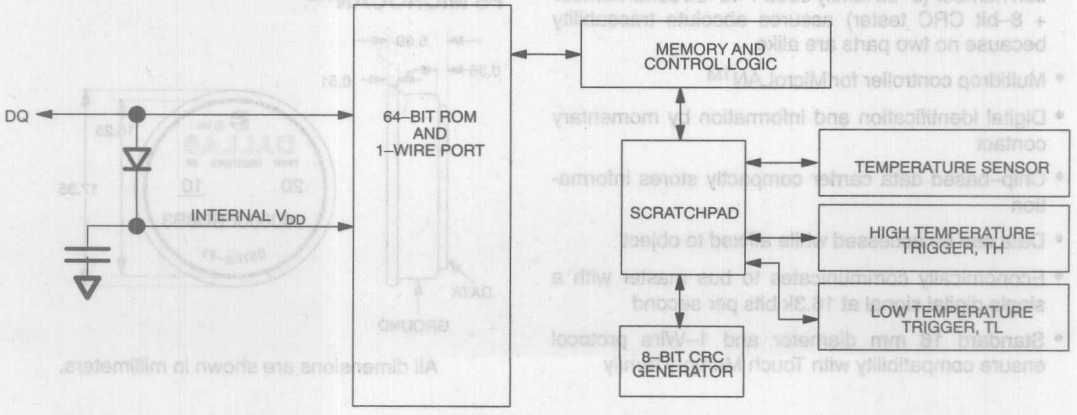
OVERVIEW

The block diagram of Figure 1 shows the major components of the DS1920. The DS1920 has three main data components: 1) 64–bit lasered ROM, 2) temperature sensor, and 3) nonvolatile temperature alarm triggers TH and TL. The device derives its power from the 1–Wire communication line by storing energy on an source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply.

Communication to the DS1920 is via a 1–Wire port. With the 1–Wire port, the memory and control functions will not be available before the ROM function protocol has been established. The master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. These commands operate on the 64–bit lasered ROM portion of each device and can single out a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible and the master may then provide any one of the five memory and control function commands.

One control function command instructs the DS1920 to perform a temperature measurement. The result of this measurement will be placed in the DS1920's scratchpad memory, and may be read by issuing a memory function command which reads the contents of the scratchpad memory. The temperature alarm triggers TH and TL consist of one byte of EEPROM each. If the alarm search command is not applied to the DS1920, these registers may be used as general purpose user memory. Writing TH and TL is done using a memory function command. Read access to these registers is through the scratchpad. All data is read and written least significant bit first.

DS1920 BLOCK DIAGRAM Figure 1



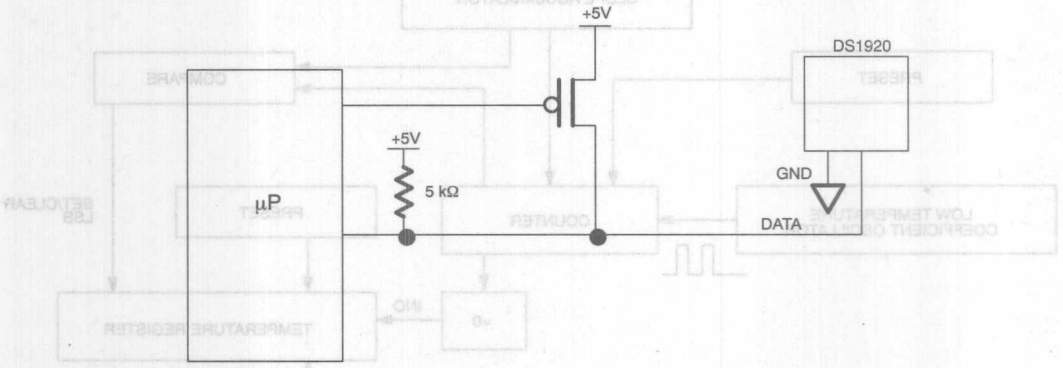
PARASITE POWER

The block diagram (Figure 1) shows the parasite powered circuitry. This circuitry "steals" power whenever the data contact is high. Data will provide sufficient power as long as the specified timing and voltage requirements are met (see the section titled "1–Wire Bus System"). The advantage of parasite power is that no local power source is needed for remote sensing of temperature.

In order for the DS1920 to be able to perform accurate temperature conversions, sufficient power must be provided over the data line when a temperature conversion is taking place. The DS1920 requires a current during conversion of up to 1 mA, therefore, the data line will not have sufficient drive due to the 5 kΩ pullup resistor. This problem is particularly acute if several DS1920's are on the same data line and attempting to convert simultaneously.

The way to assure that the DS1920 has sufficient supply current is to provide a strong pullup on the data line whenever temperature conversion is taking place. This may be accomplished by using a MOSFET to connect the data line directly to the power supply as shown in Figure 2.

STRONG PULL–UP FOR SUPPLYING DS1920 DURING TEMPERATURE CONVERSION Figure 2



OPERATION – MEASURING TEMPERATURE

The DS1920 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 3.

The DS1920 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator compensates for the non–linear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

Internally, this calculation is done inside the DS1920 to provide 0.5°C resolution. The temperature reading is provided in a 16–bit, sign–extended two's complement reading. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1–Wire interface. The DS1920 can measure temperature over the range of –55°C to +100°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Note that temperature is represented in the DS1920 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

MSB								LSB
1	1	1	0	0	1	1	1	0

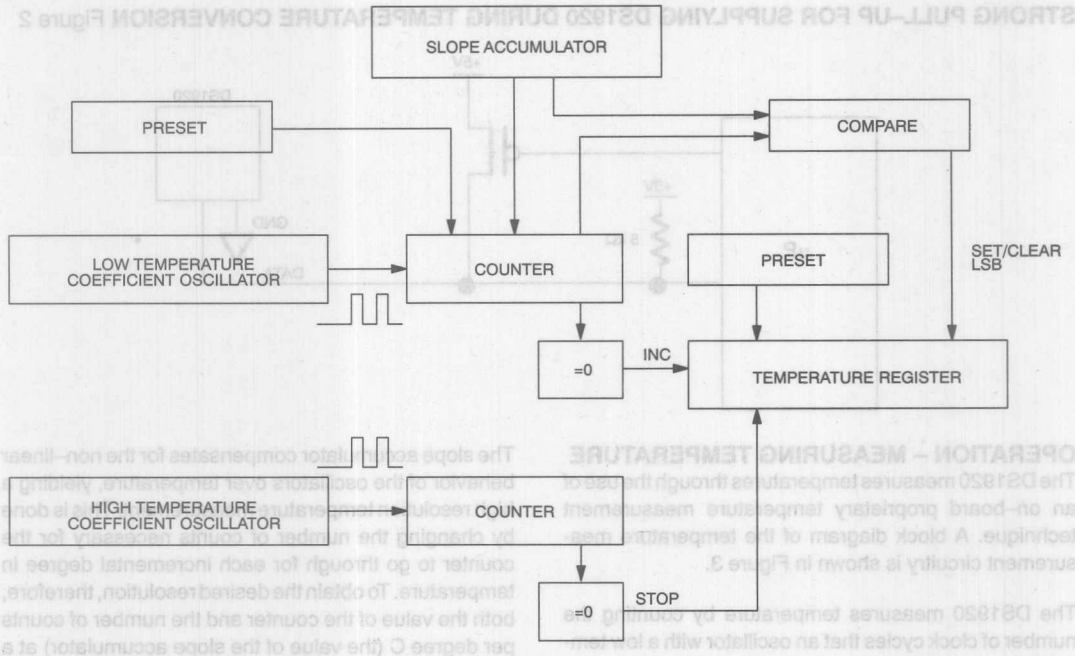
= –25°C

The most significant (sign) bit is duplicated into all of the bits in the upper MSB of the two–byte temperature register in memory. This "sign–extension" yields the 16–bit temperature readings as shown in Table 1.

Higher resolutions may be obtained by the following procedure. First, read the temperature, and truncate the 0.5°C bit (the LSB) from the read value. This value is TEMP_READ. The value left in the counter may then be read. This value is the count remaining (COUNT_REMAIN) after the gate period has ceased. The last value needed is the number of counts per degree C (COUNT_PER_C) at that temperature. The actual temperature may be then be calculated by the user using the following formula:

$$\text{TEMPERATURE} = \text{TEMP\_READ} - 0.25 + \frac{(\text{COUNT\_PER\_C} - \text{COUNT\_REMAIN})}{\text{COUNT\_PER\_C}}$$

TEMPERATURE MEASURING CIRCUITRY Figure 3



TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+100°C	00000000 11001000	00C8H
+25°C	00000000 00110010	0032H
$+^1/_2$°C	00000000 00000001	0001H
+0°C	00000000 00000000	0000H
$-^1/_2$°C	11111111 11111111	FFFFH
–25°C	11111111 11001110	FFCEH
–55°C	11111111 10010010	FF92H

OPERATION – ALARM SIGNALLING

After the DS1920 has performed a temperature conversion, the temperature value is compared to the trigger values stored in TH and TL. Since these registers are 8 bits only, the 0.5°C bit is ignored for comparison. The most significant bit of TH or TL directly corresponds to the sign bit of the 16–bit temperature register. If the result of a temperature measurement is higher than TH or lower than TL, an alarm flag inside the device is set. This flag is updated with every temperature measurement. As long as the alarm flag is set, the DS1920 will respond to the alarm search command. This allows many DS1920s to be connected in parallel doing simultaneous temperature measurements. If somewhere the temperature exceeds the limits, the alarming device(s) can be identified and read immediately without having to read non–alarming devices.

64–BIT LASERED ROM

Each DS1920 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code (DS1920 code is 10h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 4.) The 64–bit ROM and ROM Function Control section allow the DS1920 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The memory and control functions of the DS1920 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM function protocol flowchart (Figure 5). The 1–Wire bus master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. After a ROM function sequence has been successfully executed, the functions specific to the DS1920 are accessible and the bus master may then provide any one of the five memory and control function commands.

CRC GENERATION

The DS1920 has an 8–bit CRC stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS1920 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is:

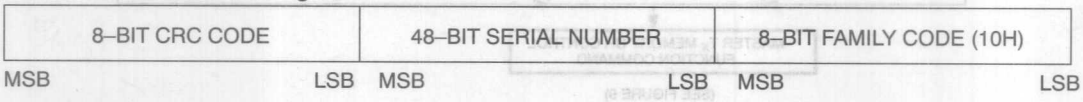
$$CRC = X^8 + X^5 + X^4 + 1$$

The DS1920 also generates an 8–bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8–bit CRC value stored in the 64–bit ROM portion of the DS1920 (for ROM reads) or the 8–bit CRC value computed within the DS1920 (which is read as a ninth byte when the scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS1920 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS1920 does not match the value generated by the bus master.

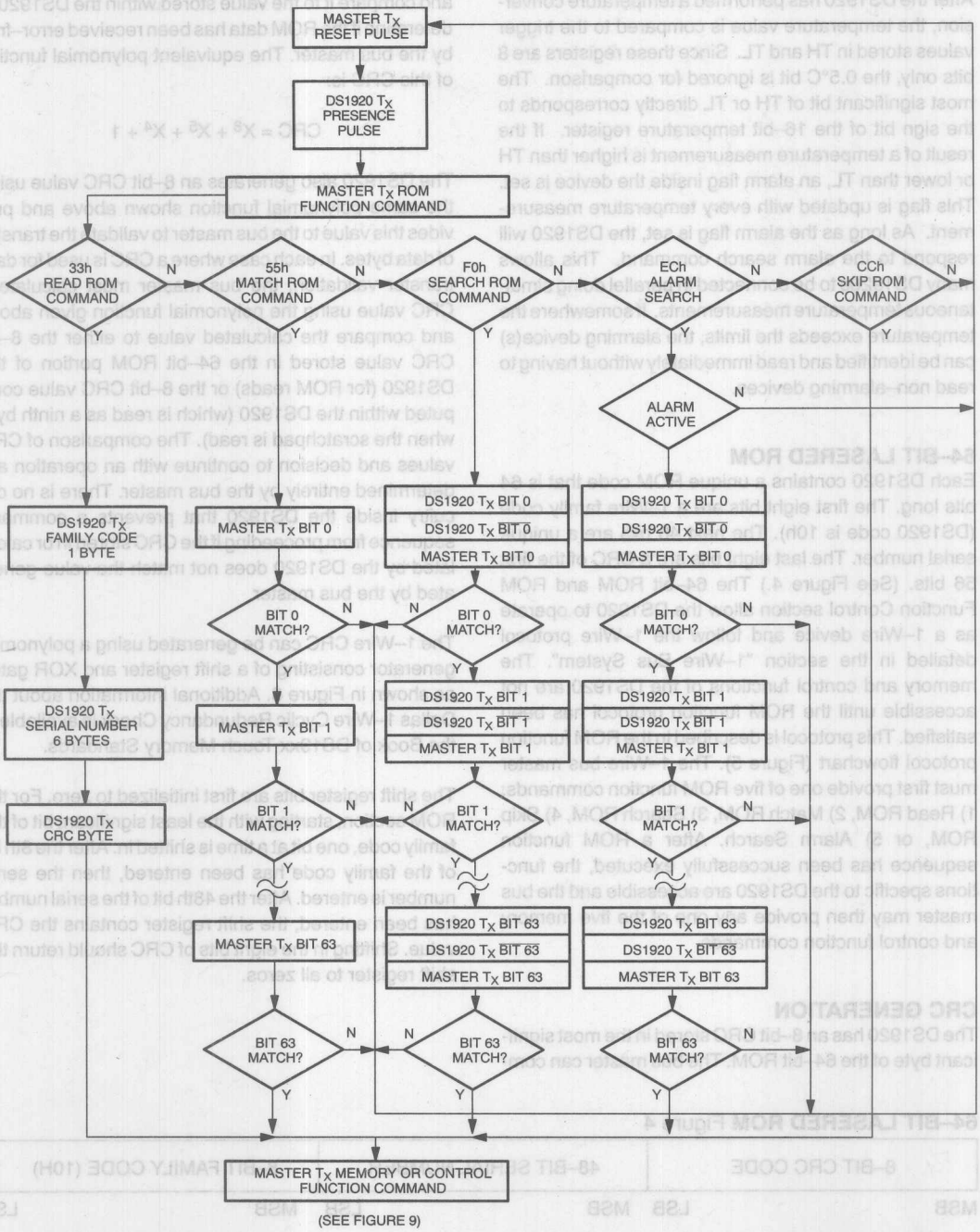
The 1–Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 6. Additional information about the Dallas 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards.

The shift register bits are first initialized to zero. For the ROM section, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

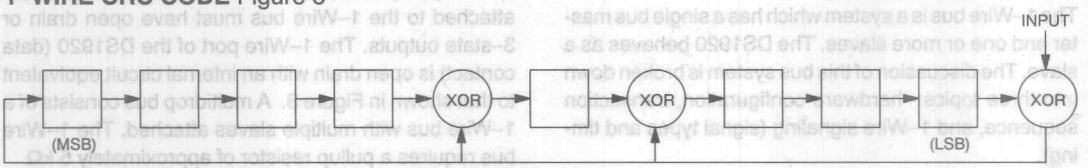
64–BIT LASERED ROM Figure 4



ROM FUNCTIONS FLOW CHART Figure 5



1–WIRE CRC CODE Figure 6



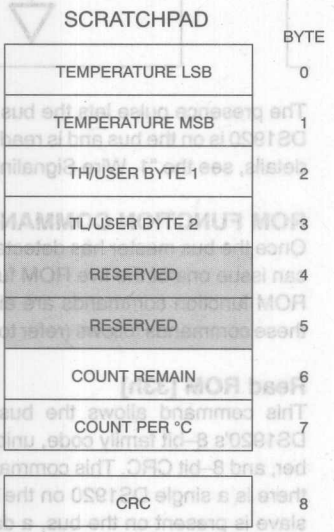
MEMORY

The DS1920's memory is organized as shown in Figure 7. The memory consists of a scratchpad and two bytes of EEPROM which store the high and low temperature triggers TH and TL. The scratchpad helps insure data integrity when communicating over the 1–Wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the EEPROM. This process insures data integrity when modifying the memory.

The scratchpad is organized as eight bytes of memory. The first two bytes contain the measured temperature information. The third and fourth bytes are volatile copies of TH and TL and are refreshed with every power–on reset. The next two bytes are not used; upon reading back, however, they will appear as all logic 1's. The seventh and eighth bytes are count registers, which may be used in obtaining higher temperature resolution (see "Operation–Measuring Temperature" section).

There is a ninth byte which may be read with a Read Scratchpad command. This byte is a cyclic redundancy check (CRC) over all of the eight previous bytes. This CRC is implemented as described in the section titled "CRC Generation".

DS1920 MEMORY MAP Figure 7



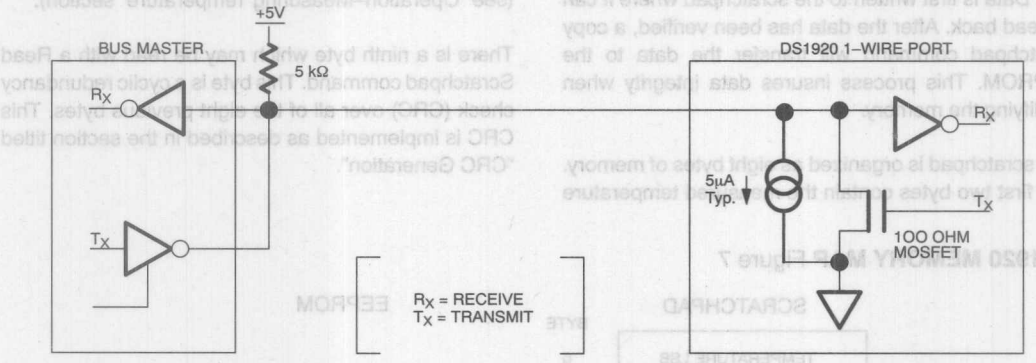
1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. The DS1920 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have open drain or 3–state outputs. The 1–Wire port of the DS1920 (data contact) is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus requires a pullup resistor of approximately 5 kΩ.

HARDWARE CONFIGURATION Figure 8



The idle state for the 1–Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS1920 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/Control Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1920 is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence pulse, it can issue one of the five ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 5):

Read ROM [33h]

This command allows the bus master to read the DS1920's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can only be used if there is a single DS1920 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired AND result).

Match ROM [55h]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific

DS1920 on a multidrop bus. Only the DS1920 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired AND result).

The Skip ROM command is useful to address all DS1920s on the bus to do a temperature conversion. Since the DS1920 uses a special command set, other device types will not respond to these commands.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus.

The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM Search, including an actual example.

Alarm Search [ECh]

The flowchart of this command is identical to the Search ROM command. However, the DS1920 will respond to this command only if an alarm condition has been encountered at the last temperature measurement. An alarm condition is defined as a temperature higher than TH or lower than TL. The alarm condition remains set as long as the DS1920 is powered up, until another temperature measurement reveals a non–alarming value, or the settings of TH or TL are modified so that the measured value again is within the allowed limits. For alarming, the trigger values stored in EEPROM are taken into account.

MEMORY AND CONTROL FUNCTION COMMANDS

The following command protocols are summarized in Table 2, and by the flowchart of Figure 9.

Write Scratchpad [4Eh]

This command writes to the scratchpad of the DS1920, starting at address 2. The next two bytes written will be saved in scratchpad memory, at address locations 2 and 3. Writing may be terminated at any point by issuing a reset. However, if a reset occurs before both bytes have been completely sent, the contents of these bytes will be indeterminate. Bytes 2 and 3 can be read and written, all other bytes are read only.

Read Scratchpad [BEh]

This command reads the complete scratchpad. After the last byte of the scratchpad is read, the bus master will receive an 8–bit CRC of all scratchpad bytes. If not all locations are to be read, the master may issue a reset to terminate reading at any time.

Copy Scratchpad [48h]

This command copies from the scratchpad into the E^2 memory of the DS1920, storing the temperature trigger bytes in nonvolatile memory. The bus master has to enable a strong pullup for at least 10 ms immediately after issuing this command.

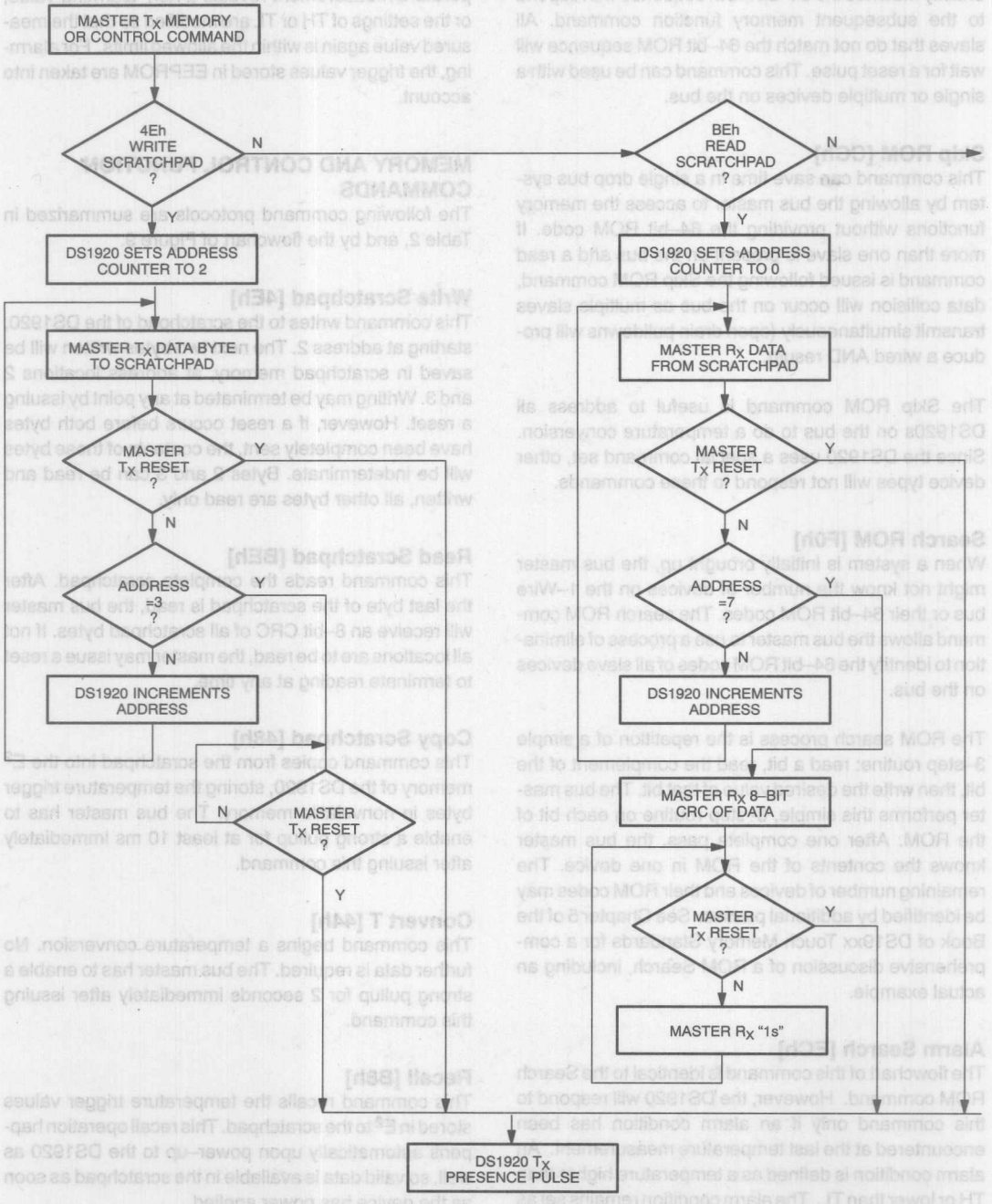
Convert T [44h]

This command begins a temperature conversion. No further data is required. The bus master has to enable a strong pullup for 2 seconds immediately after issuing this command.

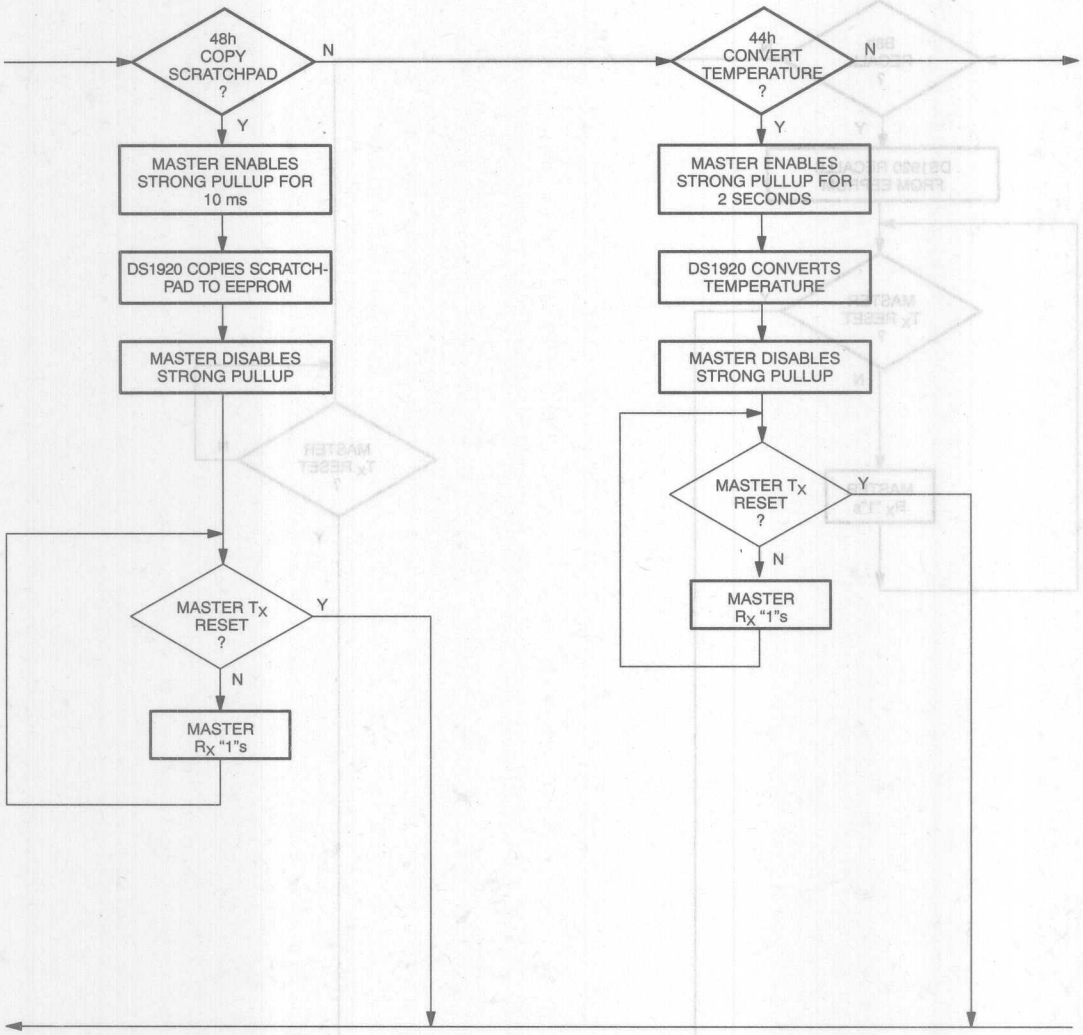
Recall [B8h]

This command recalls the temperature trigger values stored in E^2 to the scratchpad. This recall operation happens automatically upon power–up to the DS1920 as well, so valid data is available in the scratchpad as soon as the device has power applied.

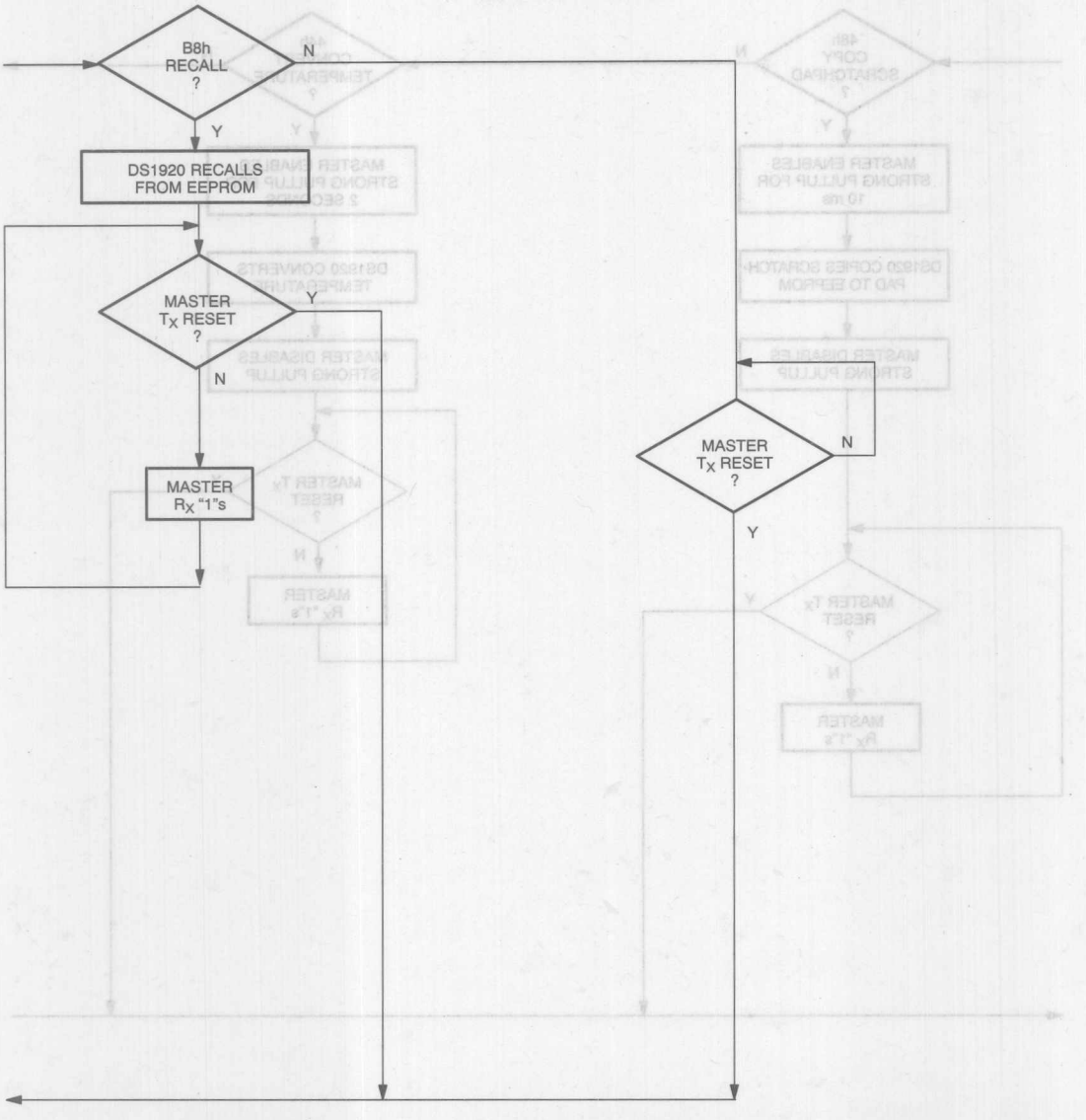
MEMORY AND CONTROL FUNCTIONS FLOW CHART Figure 9



MEMORY AND CONTROL FUNCTIONS FLOW CHART (cont'd) Figure 9



MEMORY AND CONTROL FUNCTIONS FLOW CHART (cont'd) Figure 9



1–WIRE SIGNALLING

The DS1920 requires strict protocols to insure data integrity. The protocol consists of five types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, write 0, write 1, read data and Strong Pullup. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS1920 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1920 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the 1–Wire line, the DS1920 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

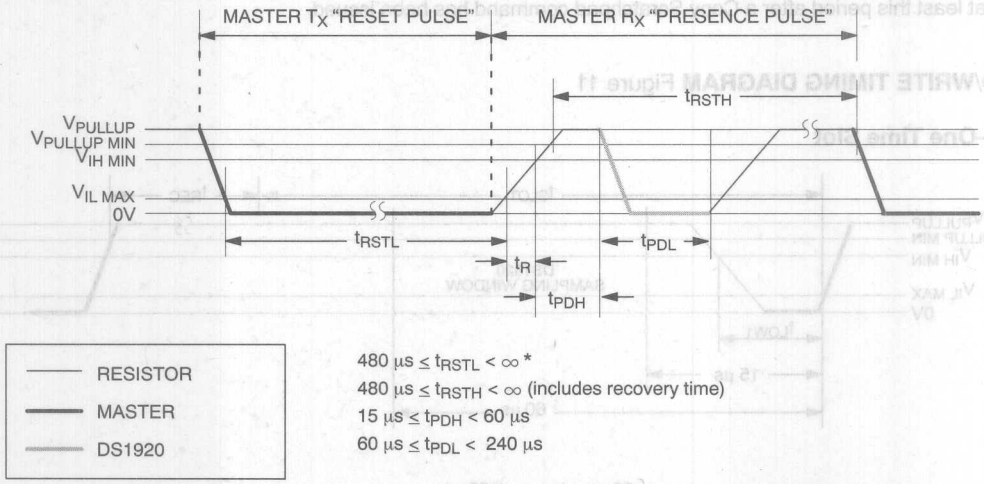
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1920 to the master by triggering a delay circuit in the DS1920. During write time slots, the delay circuit determines when the DS1920 will sample the data line, For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1920 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the DS1920 will leave the read data time slot unchanged.

STRONG PULLUP

To provide energy for a temperature conversion or for copying data from the scratchpad to the EEPROM, a low impedance pullup of the 1–Wire bus to 5V is required just after the corresponding command has been sent by the master. During temperature conversion or copying the scratchpad, the bus master controls the transition from a state where the data line is idling high via the pull–up resistor to a state where the data line is actively driven to 5 volts providing a minimum of 1 mA of current for each DS1920 doing temperature conversion. This low impedance pullup should be active for 2 seconds for temperature conversion or at least 10 ms for copying to the scratchpad. After that, the data line returns to an idle high state controlled by the pull–up resistor. The low–impedance pullup does not affect other devices on the 1–Wire bus. Therefore it is possible to multidrop other 1–Wire devices with the DS1920.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

DS1920 MEMORY AND CONTROL FUNCTION COMMANDS Table 2

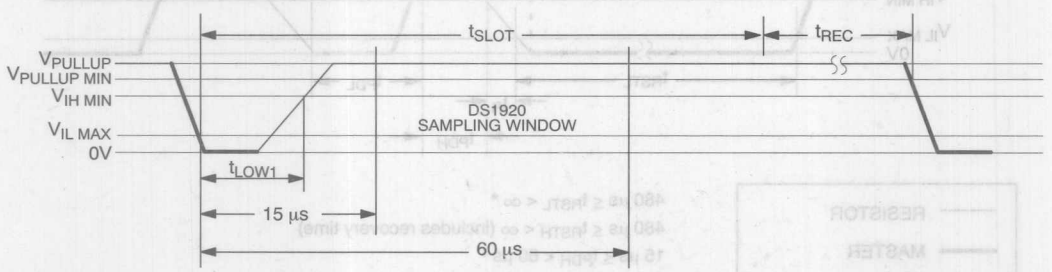
INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44H	strong pullup	1
MEMORY COMMANDS				
Read Scratchpad	Reads bytes from scratchpad and reads CRC byte.	BEH	<read up to 9 data bytes>	
Write Scratchpad	Writes bytes into scratchpad at addresses 2 and 3 (TH and TL temperature triggers).	4EH	<write data into 2 bytes at addr. 2 and addr. 3>	
Copy Scratchpad	Copies scratchpad into nonvolatile memory (addresses 2 and 3 only).	48H	strong pullup	2
Recall	Recalls values stored in nonvolatile memory into scratchpad (temperature triggers).	B8H	idle	

NOTE:

1. Temperature conversion takes up to 2 seconds. After receiving the Convert T protocol, the data line for the DS1920 must be held high for at least 2 seconds to provide power during the conversion process. As such, no other activity may take place on the 1–Wire bus for at least this period after a Convert T command has been issued.
2. After receiving the Copy Scratchpad protocol, the data line for the DS1920 must be held high for at least 10 ms to provide power during the copy process. As such, no other activity may take place on the 1–Wire bus for at least this period after a Copy Scratchpad command has been issued.

READ/WRITE TIMING DIAGRAM Figure 11

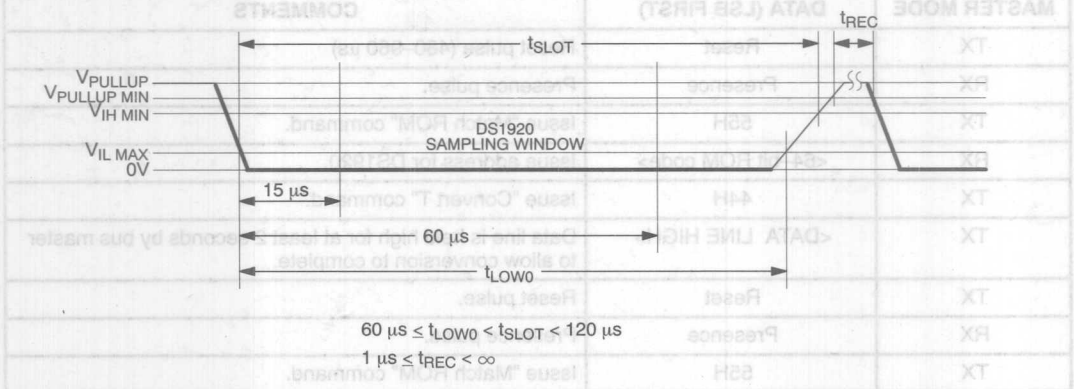
Write–One Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM (cont'd) Figure 11

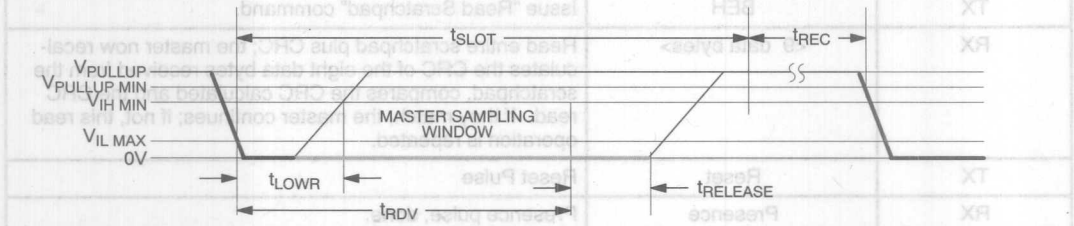
Write–Zero Time Slot

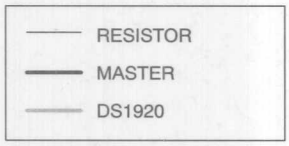


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–Data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

MEMORY FUNCTION EXAMPLE Table 3

Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 μs)
RX	Presence	Presence pulse.
TX	55H	Issue "Match ROM" command.
RX	<64–bit ROM code>	Issue address for DS1920.
TX	44H	Issue "Convert T" command.
TX	<DATA LINE HIGH>	Data line is held high for at least 2 seconds by bus master to allow conversion to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	55H	Issue "Match ROM" command.
TX	<64–bit ROM code>	Issue address for DS1920.
TX	BEH	Issue "Read Scratchpad" command.
RX	<9 data bytes>	Read entire scratchpad plus CRC; the master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC calculated and the CRC read. If they match, the master continues; if not, this read operation is repeated.
TX	Reset	Reset Pulse
RX	Presence	Presence pulse, done.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +100°C
Storage Temperature	–55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CONDITIONS

(–55°C to +100°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Pullup Voltage	V_{PUP}	I/O Functions	2.8	5.0	6.0	V	1, 2
		±1/2°C Accurate Temperature Conversions	4.3		6.0	V	
Logic 1	V_{IH}		2.2		V_{PUP}+0.3	V	2
Logic 0	V_{IL}		–0.3		+0.8	V	2

DC ELECTRICAL CHARACTERISTICS

(–55°C to +100°C; V_{PUP}=4.3V to 6.0V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	t_{ERR}	0°C to +70°C			±1/2	°C	
		–40°C to +0°C and +70°C to +85°C			±1	°C	
		–55°C to –40°C and +85°C to +100°C			±2	°C	
Active Current	I_{DD}			500	1000	µA	3, 4
Input Load Current	I_L			5		µA	
Output Logic Low @ 4 mA	V_{OL}				0.4	V	2

AC ELECTRICAL CHARACTERISTICS; TEMPERATURE CONVERSION AND COPY SCRATCHPAD

(–55°C to +100°C; V_{PUP}=4.3V to 6.0V)

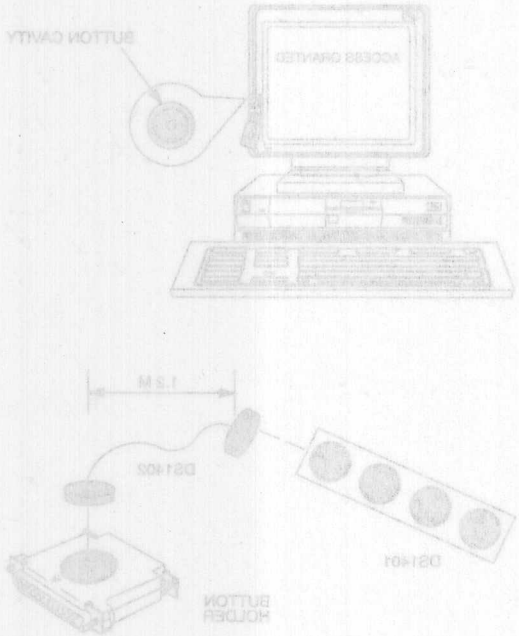
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion	t_{CONV}		1.2	2.0	seconds	
Copy Scratchpad	t_{COPY}			10	ms	5

Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	8
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		4800	µs	6, 7
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

NOTES:

1. Temperature conversion will work with ±2°C accuracy down to V_{PUP} = 3.4V.
2. All voltages are referenced to ground.
3. I_{DD} specified with V_{CC} at 5.0V
4. Active current refers to temperature conversion.
5. Writing to EEPROM consumes approximately 200 µA.
6. t_{RSTL} may be up to 4800 µs. With longer times, the value of temperature conversion may get lost.
7. The reset low time should be restricted to a maximum of 960 ms, to allow interrupt signalling, otherwise it could mask or conceal interrupt pulses.
8. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)

ACCESSORIES

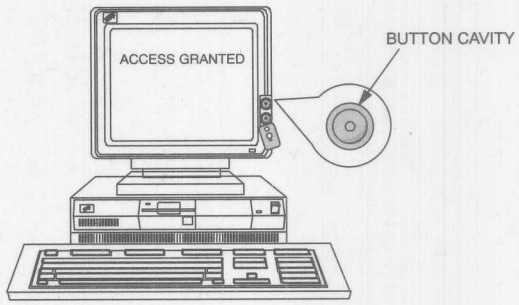


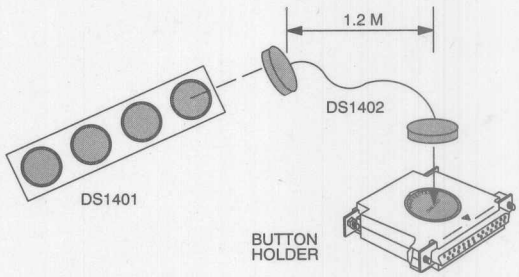
DALLAS SEMICONDUCTOR

DS1401
Front Panel Button Holder
DS1402
Button Cable

FEATURES

- A convenient interface for Buttons
- Can be used with any Dallas Semiconductor Button holder
- Provides from 4 to 24 Button ports (1 port used for Button Cable connection)
- Buttons can be inserted in any combination
- Momentary touch or dwelled contact
- Fastens to any convenient location





DESCRIPTION

Dallas Buttons can now be conveniently accessed using the DS1401 and DS1402.

The DS1401 is connected to the computer using the DS1402 and any Dallas Button Holder (which connects to an I/O port). The DS1401 mounts to any surface (top of tower computer, CRT, keyboard).

The DS1401 supports Dallas' MicroLan architecture, allowing Buttons to be inserted into Button ports in any combination. Each Button's unique 64–bit ID makes location detection automatic.

The DS1401 also supports momentary touch contact with Button ports for applications which do not require a dwelled contact.

Multiple versions of the DS1401 are available to provide 4 to 24 Button ports.

DALLAS SEMICONDUCTOR

DS9092
Touch Memory Probe

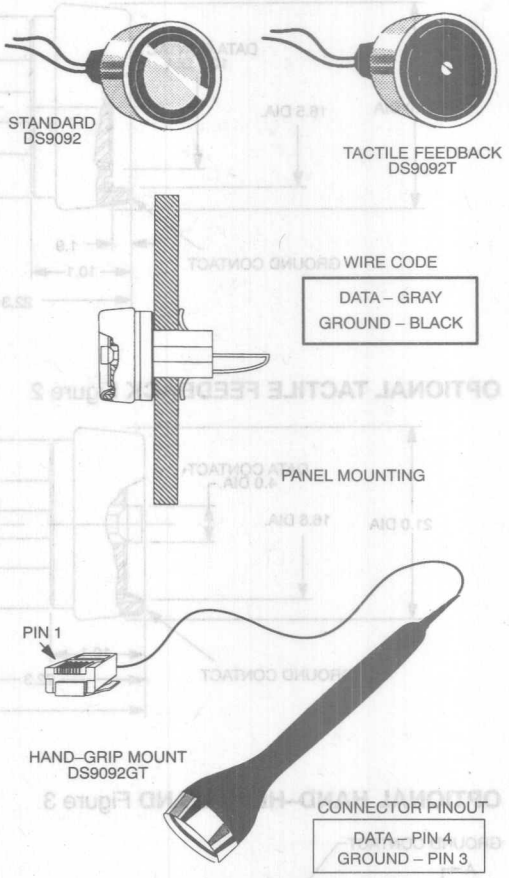
FEATURES

- Simple, low–cost metal stampings form a read/write probe for the Touch Memory family
- Probe guides the entry of the Touch Memory
- Touch Memory slides over the surface to self–clean contacts
- Accessible shallow probe cavity simplifies removal of debris such as mud
- Flexible design supports panel mount or hand–grip mount with optional tactile feedback
- Bright tarnish–resistant metal surface provides millions of operations
- Panel–mount probe, pre–wired for easy installation
- Hand–grip probe mates to RJ–11 jack for quick installation

ORDERING INFORMATION

DS9092	Panel–mount probe, solid face
DS9092T	Panel–mount probe with tactile feedback
DS9092GT	Hand–grip mount with tactile feedback

PACKAGE DESCRIPTION



DESCRIPTION

The DS9092 Touch Memory Probe provides the electrical contact necessary for the transfer of data to and from the DS19xx family of Touch Memories. The round probe shape provides a self–aligning interface that readily matches the circular rim of the Touch Memory MicroCan. Metal contacts resist wear and are easy to keep clean.

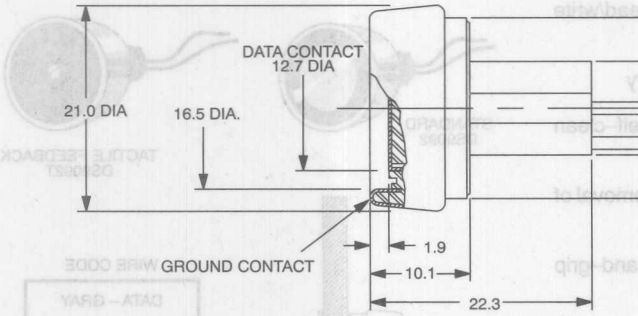
The DS9092 is available with a flat face plate (standard) or with optional tactile feedback. The center contact of the standard reader has no moving parts, making this a more rugged interface for harsh environments. This type of probe is best suited for designs where the Touch Memory is brought into contact with the reader. The tactile feedback probe is ideal for situations where the

Touch Memory is stationary and the movable reader is brought in contact with it.

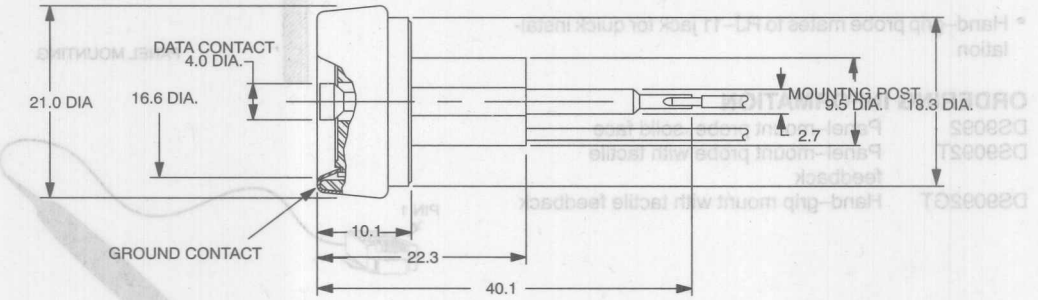
Both types of probes are available in a panel–mount version. The tactile feedback probe is also available in a grip–mount version. The panel–mount probes are fastened behind the panel with a push–on type spring nut.

The two 15 cm 22AWG wires are provided for easy connection to the system microcontroller. The hand–grip mount probe comes attached to a 10 cm handle and 1–meter cable which is terminated with an RJ11 jack.

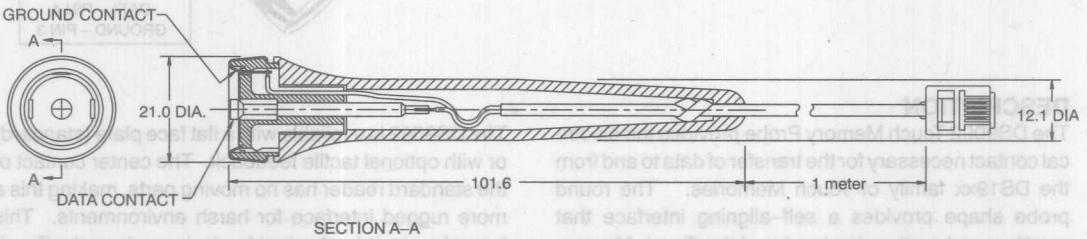
STANDARD TOUCH PROBE Figure 1



OPTIONAL TACTILE FEEDBACK Figure 2



OPTIONAL HAND–HELD WAND Figure 3



All dimensions are in millimeters. DS9092GT

DALLAS SEMICONDUCTOR

DS9092R Touch Port

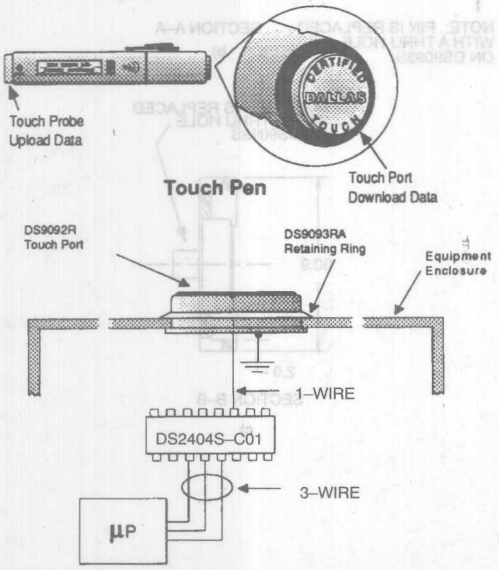
FEATURES

- Empty stainless steel MicroCan with opening in rear and solder tabs.
- Acts as a touch contact for remotely located 1–Wire devices
- Together with DS2404S–C01 makes complex functions involving microcontrollers behave as if they were Touch Memories.
- Available with "CERTIFIED DALLAS TOUCH" logo

DESCRIPTION

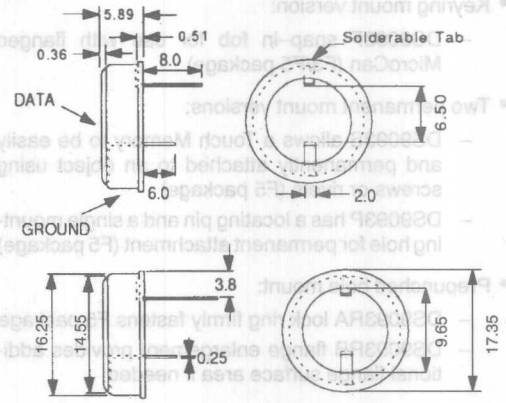
The DS9092R Touch Port provides the electrical contact necessary for mating remotely located Touch Memories or other 1–Wire MicroLAN devices with reader/writers. The DS9092R is also available with logo.

APPLICATIONS



Equipment fitted with 1–Wire button contact.

PACKAGE OUTLINE



All dimensions are shown in millimeters.

CONTACTS

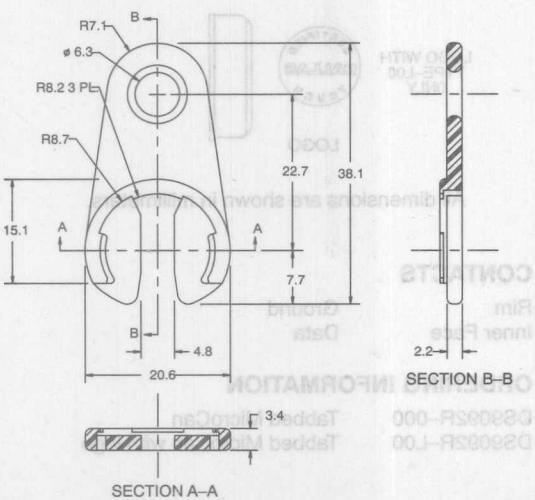
Rim	Ground
Inner Face	Data

ORDERING INFORMATION

DS9092R–000	Tabbed MicroCan
DS9092R–L00	Tabbed MicroCan with logo

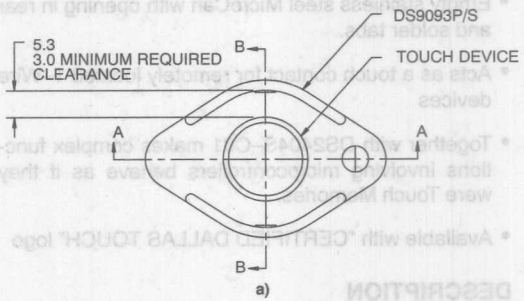
FEATURES

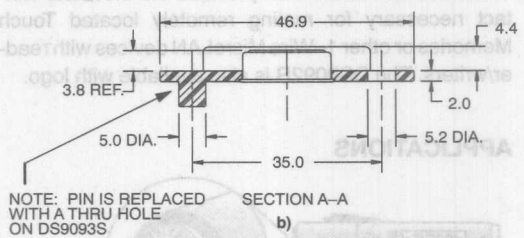
- Keyring mount version:
  - DS9093F snap–in fob for use with flanged MicroCan (F3/F5 package)
- Two permanent mount versions:
  - DS9093S allows a Touch Memory to be easily and permanently attached to an object using screws or rivets (F5 package)
  - DS9093P has a locating pin and a single mounting hole for permanent attachment (F5 package)
- Prepunched hole mount:
  - DS9093RA lock ring firmly fastens F5 package
  - DS9093RB flange enlargement provides additional flange surface area if needed

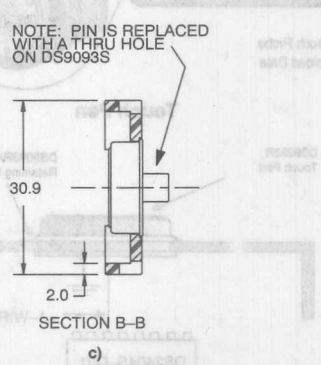


All dimensions are in millimeters.

THROUGH–MOUNT FOR CONTAINERS







DESCRIPTION

The DS9093 Touch Memory Mount Products offer the user low–cost fixtures that hold a Touch Memory for thumbpad applications or permanent attachment to an object.

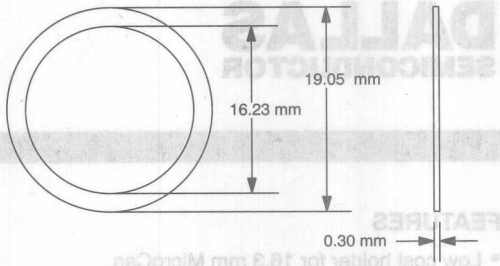
The DS9093F plastic snap–in fob offers the simplest way to mount a Touch Memory for applications that require only momentary contact. The fob can be attached to a keyring for carrying. Do not apply solvents or adhesives to this fob. This might affect the mechanical strength and reliability.

The DS9093S and DS9093P allows the user to permanently attach a Touch Memory to an object with one or two screws, rivets, etc. The plastic plate is designed with an inset that accommodates the flange of the F5 package and allows for flush mounting. A protective wall is provided along the sides of the plate to reduce incidental damage to the Touch Memory.

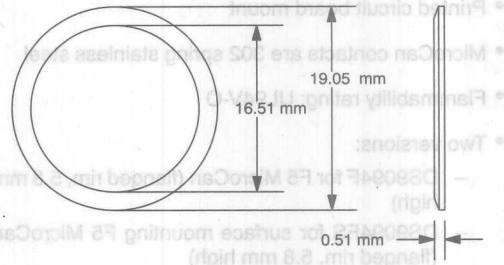
The DS9093RA Lock Ring is a stainless steel fastener which provides an inexpensive method for firmly attaching a Touch Memory to any item with a pre–punched hole. The Touch Memory is inserted through the hole and is restrained by the flange on the Touch Memory. The DS9093RA Lock Ring is crimped onto the portion of the Touch Memory which protrudes through the hole.

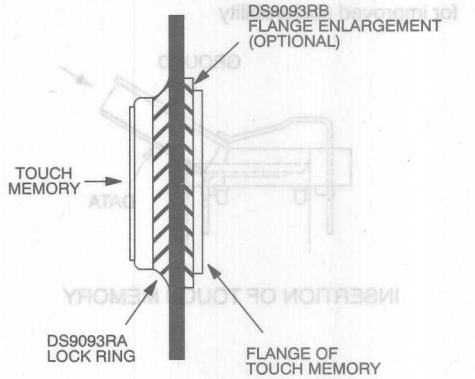
The optional DS9093RB Flange Enlargement is a thin stainless steel washer that provides additional surface area to improve retention of the Touch Memory in materials that are very thin or flexible. The DS9093RB is formed with a slight dome to improve the gripping force exerted onto the pre–punched material. The domed side of the washer should face the flange of the Touch Memory, the flat side should face the material.

DS9093RA



DS9093RB



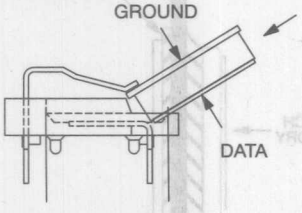


DALLAS SEMICONDUCTOR

DS9094
MicroCan Clip

FEATURES

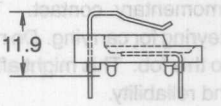
- Low cost holder for 16.3 mm MicroCan
- Printed circuit board mount
- MicroCan contacts are 302 spring stainless steel
- Flammability rating: UL94V-O
- Two versions:
  - DS9094F for F5 MicroCan (flanged rim, 5.8 mm high)
  - DS9094FS for surface mounting F5 MicroCan (flanged rim, 5.8 mm high)
- Printed circuit contacts are selectively tin-lead plated for improved solderability



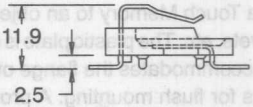
INSERTION OF TOUCH MEMORY

DESCRIPTION

The DS9094 Clip holds a MicroCan and connects to a printed circuit board. By deflecting the spring clip in the molded housing, a MicroCan can be inserted and extracted without special tools. If reverse insertion is attempted, the beveled edge on the housing prevents contact. The DS9094's low profile minimizes the clearance height above the printed circuit board.

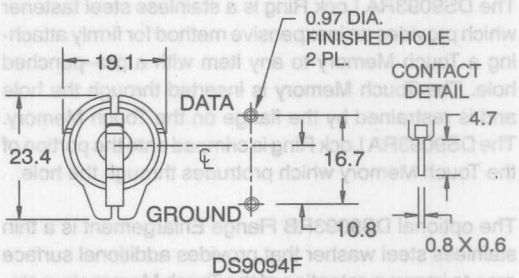


DS9094F

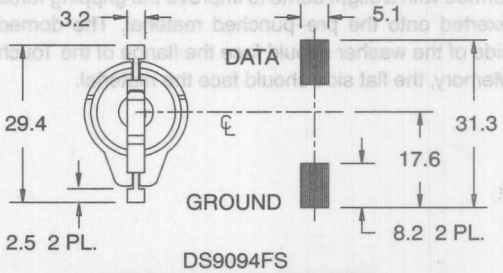


DS9094FS

PC BOARD MOUNTING DETAILS



DS9094F
RECOMMENDED HOLE SIZE



DS9094FS
RECOMMENDED PAD SIZE

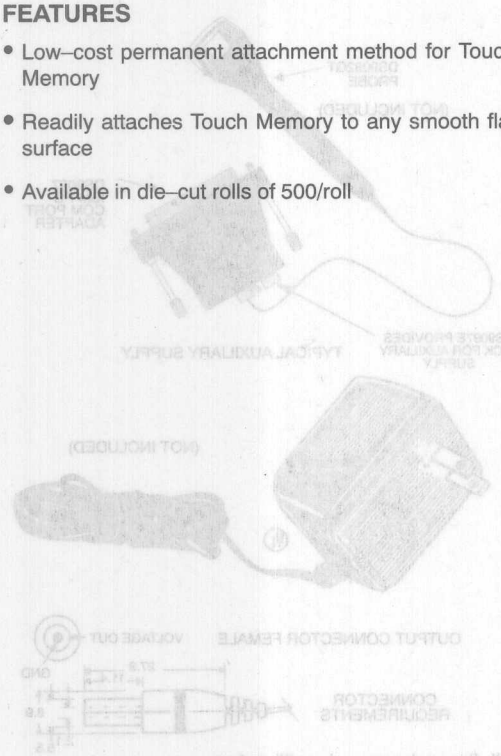
All dimensions are in millimeters.

DALLAS SEMICONDUCTOR

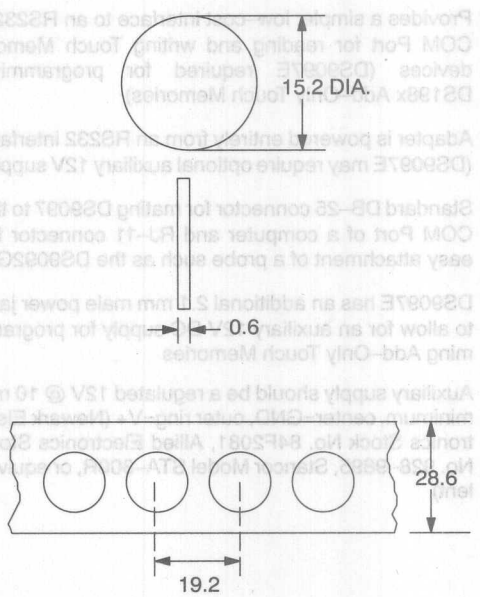
DS9096P
Touch Memory Adhesive Pads

FEATURES

- Low–cost permanent attachment method for Touch Memory
- Readily attaches Touch Memory to any smooth flat surface
- Available in die–cut rolls of 500/roll



DIMENSIONS



All dimensions are shown in millimeters.

DESCRIPTION

The DS9096P Touch Memory adhesive pad is a double–sided pad that is die–cut to match the diameter of Touch Memory devices. The pads allow Touch Memories to be attached to virtually any smooth surface. The DS9096P offers a very permanent attachment method that is not intended to be removed.

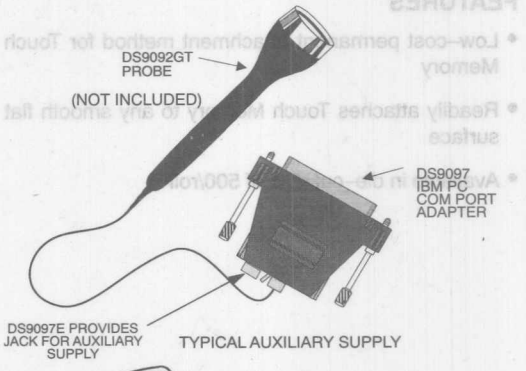
DALLAS SEMICONDUCTOR

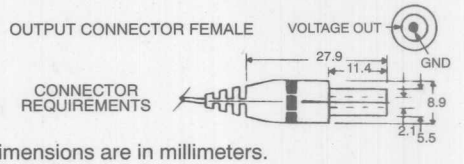
DS9097/DS9097E
Touch COM Port Adapter

FEATURES

- Provides a simple, low–cost interface to an RS232C COM Port for reading and writing Touch Memory devices (DS9097E required for programming DS198x Add–Only Touch Memories)
- Adapter is powered entirely from an RS232 interface (DS9097E may require optional auxiliary 12V supply)
- Standard DB–25 connector for mating DS9097 to the COM Port of a computer and RJ–11 connector for easy attachment of a probe such as the DS9092GT
- DS9097E has an additional 2.1 mm male power jack to allow for an auxiliary 12V DC supply for programming Add–Only Touch Memories

  Auxiliary supply should be a regulated 12V @ 10 mA minimum, center=GND, outer ring=V+ (Newark Electronics Stock No. 84F2081, Allied Electronics Stock No. 928–9895, Stancor Model STA–300R, or equivalent)





All dimensions are in millimeters.

DESCRIPTION

The DS9097 Touch Serial Port Adapter is a simple, low–cost passive adapter which performs RS232C level conversion, allowing a Touch Memory probe to be connected to the serial port of a computer so that a Touch Memory can be read and written directly. The serial port must support a data transmission rate of 115,200 bits/s in order to create the 1–Wire time slots correctly. Nearly all PCs support the required bit rate and are fully compatible with the DS9097. Since an eight bit character on the RS232 bus operating at 115,200 bits/s is used to form the 1–Wire time slots, the maximum effective 1–Wire transfer rate is 14,400 bits/s. A selection of software examples illustrating how to communicate with Touch Memories using the DS9097 is provided in the DS9092K Touch Memory Starter Kit, available from Dallas Semiconductor.

The DS9097E is an upgraded version of the DS9097 that is capable of supplying the 12 volts necessary to program the EPROM–based Touch Memory products (DS198x Add–Only Memories) in addition to reading and writing standard devices (DS199x). When combined with the appropriate software, the DS9097E can be used in a standalone mode where all of the programming current is supplied by the serial port itself. In this configuration, the maximum number of EPROM bits that can be programmed simultaneously is four on a typical serial port. For higher performance, the above mentioned 12V auxiliary supply can be plugged into the power jack on the DS9097E and with proper software enable the serial port to program up to eight EPROM bits simultaneously.

DALLAS SEMICONDUCTOR

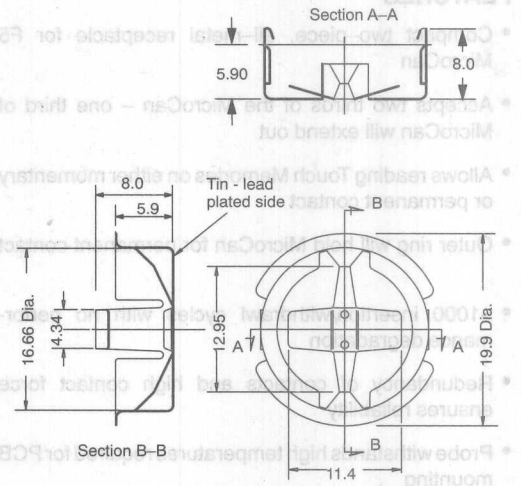
DS9098
MicroCan Retainer

FEATURES

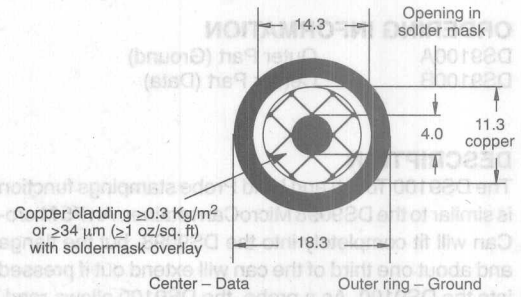
- Compact single-piece, all-metal receptacle for MicroCan mounting
- Retainer withstands high temperatures required for surface mounting
- Center contact is permanently separated at first insertion of MicroCan
- Material is stainless steel with selective tin-lead plating for optimal solderability to printed circuit board
- Retainer to MicroCan connection is stainless steel to stainless steel
- Quadruple redundancy of contacts (4 plus 4)
- Contact force exceeds 200 grams for reliable connection
- At insertion, MicroCan is latched for retention
- Pops up for removal when latch is released
- Gentle deflection of latches allows removal of the MicroCan
- >25 insertion/withdrawal cycles with no performance degradation
- Compatible with standard pick and place equipment; insensitive to angular orientation
- Cleaning fluids drain freely for quick clean up
- Available in bulk packaging (DS9098) or in extruded tube packaging (DS9098T)

DESCRIPTION

The DS9098 MicroCan Retainer is a low-cost, surface mount device that retains a 16.3mm x 5.8mm MicroCan on a printed circuit board. The slender design secures the MicroCan for a compact printed circuit board mount. The retainer latches the flange of the MicroCan and prevents reversed insertion.



Recommended Printed Circuit Layout Pads



All dimensions are in millimeters

PRECAUTIONS ON USE

At first insertion closely align axis of the MicroCan and the Retainer, and then apply approximately 10 kg force for the separation of the center contacts. At subsequent insertion maintain similar axial alignment to avoid permanent deformation. At removal, limit deflection of retainer latches to just free MicroCan edge from retained state. Avoid applying excess force to latches.

041594 1/1

PRELIMINARY

DALLAS SEMICONDUCTOR

DS9100
Touch and Hold Probe Stampings

FEATURES

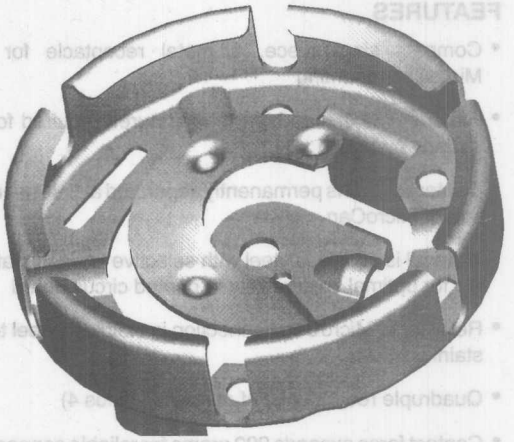
- Compact two–piece, all–metal receptacle for F5 MicroCan
- Accepts two thirds of the MicroCan – one third of MicroCan will extend out
- Allows reading Touch Memories on either momentary or permanent contact
- Outer ring will hold MicroCan for permanent contact
- >1000 insertion/withdrawl cycles with no performance degradation
- Redundancy of contacts and high contact force ensures reliability
- Probe withstands high temperatures required for PCB mounting
- Material is stainless steel with selective tin–lead plating for optimal solderability to printed circuit board
- Cleaning fluids drain freely for quick clean up

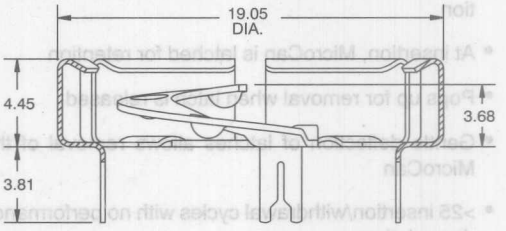
ORDERING INFORMATION

DS9100A	Outer Part (Ground)
DS9100B	Center Part (Data)

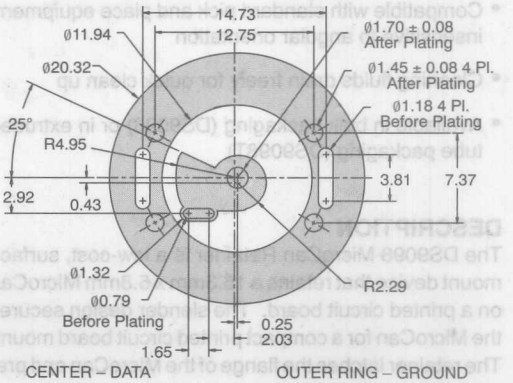
DESCRIPTION

The DS9100 Touch and Hold Probe stampings function is similar to the DS9098 MicroCan retainer. An F5 MicroCan will fit completely into the DS9098, but the flange and about one third of the can will extend out if pressed into the DS9100. As a probe, the DS9100 allows reading Touch Memories on contact. With Additional pressure the stiff springs of the DS9100's outer ring will deflect and grip the MicroCan sufficiently to provide a continuous contact to both the ground can and the data lid.





RECOMMENDED PCB LAYOUT



CENTER – DATA OUTER RING – GROUND

COPPER CLADDING > 0.3 kg/m^2 or > 34 µm
(>1 oz/sq. ft)

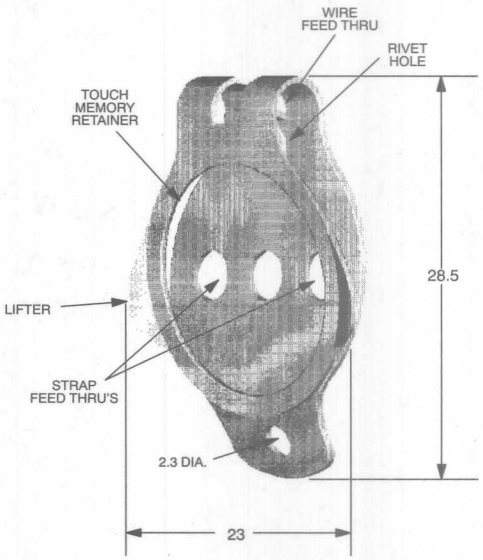
All dimensions are in millimeters.

DALLAS SEMICONDUCTOR

DS9101
Multi–Purpose Clip

FEATURES

- Attachable to a badge
- Easy detachment by hand
- Mountable by safety pin to fabric
- Two pairs of holes for attachment, one for wire mounting, and one for tie wrap
- Clipable to shirt pocket
- Stainless steel 0.5 mm thickness
- Attachable to other items with snap fastener (DS9101S)

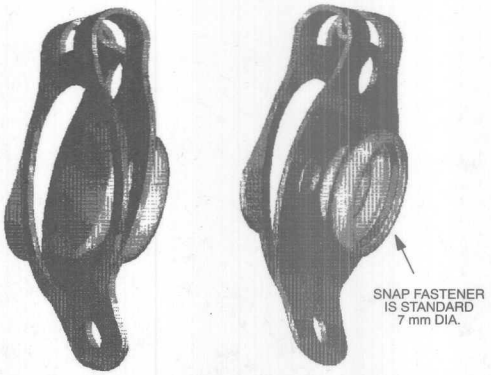


DESCRIPTION

The DS9101 Multi–Purpose Clip offers the user a low–cost fixture that mounts a Touch Memory to a plastic badge or, using an additional wire or tie wrap, any object that provides a hole for strap–mounting. In contrast to the DS9093P/S, the DS9101 also allows mounting Touch Memories to bags or other soft surfaced objects.

The DS9101 is designed for easy attachment and detachment. Using a DS9093RA Lock Ring, the DS9101 can hold a Touch Memory permanently and still allow all the flexibility of strap mounting.

For quick attachment and dismount use DS9101S, assembled with snap fastener, providing smooth and reliable fastening means.



FRONT SIDE BACK SIDE

DS9101S for snap fastening

Dimensions are shown in millimeters.

FEATURES

- Attachable to a badge
- Easy detachment by hand
- Mountable by safety pin to fabric
- Two pairs of holes for attachment, one for wire mounting, and one for tie wrap
- Clipable to shirt pocket
- Stainless steel 0.5 mm thickness
- Attachable to other items with snap fastener (DS9101S)

DESCRIPTION

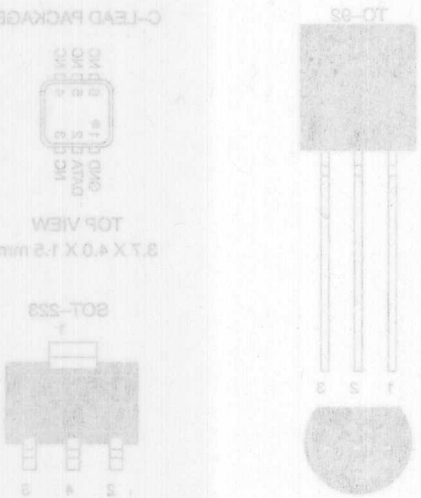
The DS9101 Multi-Purpose Clip offers the user a low-cost fixture that mounts a Touch Memory to a plastic badge or, using an additional wire or tie wrap, any object that provides a hole for strap-mounting. In contrast to the DS9092P/S, the DS9101 also allows mounting Touch Memories to bags or other soft surfaced objects.

The DS9101 is designed for easy attachment and detachment. Using a DS9092RA Lock Ring, the DS9101 can hold a Touch Memory permanently and still allow all the flexibility of strap mounting.

For quick attachment and dismount use DS9101S, assembled with snap fastener, providing smooth and reliable fastening means.

DS9101S for snap fastening

Dimensions are shown in millimeters.



PIN DESCRIPTION

TO–92/SOT–223		C–LEAD	
Pin 1	– Ground	Pin 1	– Ground
Pin 2	– Data (DQ)	Pin 2	– Data (DQ)
Pin 3	– No Connect	Pin 3	– No Connect
Pin 4	– Ground	Pin 4–6	– No Connect

ORDERING INFORMATION

DS2401	TO–92 Package
DS2401Z	SOT–223 Surface Mount Package
DS2401T	Tape & Reel of DS2401
DS2401Y	Tape & Reel of DS2401Z
DS2401P	C–lead Surface Mount Package
DS2401V	Tape & Reel of DS2401P

DALLAS SEMICONDUCTOR

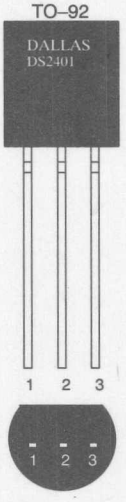
DS2401
Silicon Serial Number

FEATURES

- Upgrade and drop–in replacement for DS2400
  - Extended 2.8 to 6.0 voltage range
  - Multiple DS2401's can reside on a common 1–wire bus
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester); guaranteed no two parts alike
- Built–in multidrop controller ensures compatibility with other MicroLAN™ products
- 8–bit family code specifies DS2401 communications requirements to reader
- Presence pulse acknowledges when the reader first applies voltage
- Low–cost TO–92, SOT–223 and C–lead surface mount packages
- Reduces control, address, and data to a single pin
- Zero standby power required
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits/s
- Pulse width measurement determines 1's or 0's
- Power derived from data line
- Applications
  - PCB Identification
  - Network Node ID
  - Equipment Registration
- Operates over industrial temperature range of –40°C to +85°C

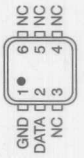
PIN ASSIGNMENT

TO–92



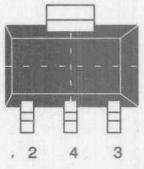
BOTTOM VIEW
See Mech. Drawing Pg. 340

C–LEAD PACKAGE



TOP VIEW
3.7 X 4.0 X 1.5 mm

SOT–223



TOP VIEW
See Mech. Drawing Pg. 344

PIN DESCRIPTION

TO–92/SOT–223			C–LEAD		
Pin 1	–	Ground	Pin 1	–	Ground
Pin 2	–	Data (DQ)	Pin 2	–	Data (DQ)
Pin 3	–	No Connect	Pin 3	–	No Connect
Pin 4	–	Ground	Pin 4–6	–	No Connect

ORDERING INFORMATION

DS2401	TO–92 Package
DS2401Z	SOT–223 Surface Mount Package
DS2401T	Tape & Reel of DS2401
DS2401Y	Tape & Reel of DS2401Z
DS2401P	C–lead Surface Mount Package
DS2401V	Tape & Reel of DS2401P

SILICON LABEL™ DESCRIPTION

The DS2401 enhanced Silicon Serial Number is a low–cost, electronic registration number that provides an absolutely unique identity which can be determined with a minimal electronic interface, typically a single port pin of a microcontroller. The DS2401 consists of a factory–lasered, 64–bit ROM that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit Family Code (01h). Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return. Power for reading and writing the device is

derived from the data line itself with no need for an external power source. The DS2401 is an upgrade to the DS2400. The DS2401 is fully reverse–compatible with the DS2400 but provides the additional multi–drop capability that enables many devices to reside on a single data line. The familiar TO–92, SOT–223 or C–lead package provides a compact enclosure that allows standard assembly equipment to handle the device easily.

OPERATION

The DS2401's internal ROM is accessed via a single data line. The 48–bit serial number, 8–bit family code and 8–bit CRC are retrieved using the Dallas 1–Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

1–WIRE BUS SYSTEM

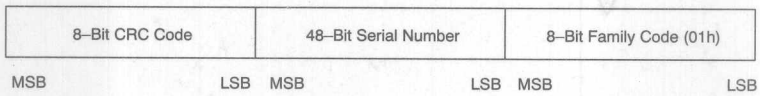
The 1–Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS2401 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal type and timing). For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

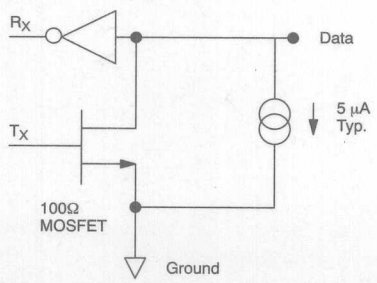
The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS2401 is an open drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second.

The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

DS2401 MEMORY MAP Figure 1

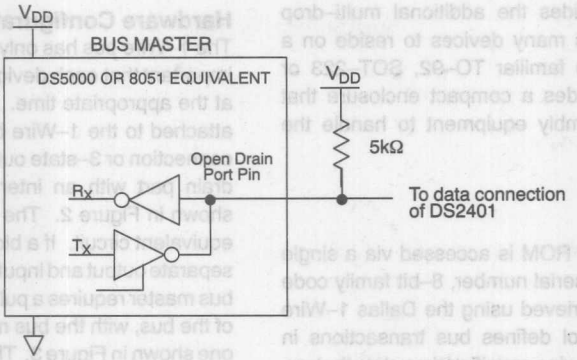


DS2401 EQUIVALENT CIRCUIT Figure 2

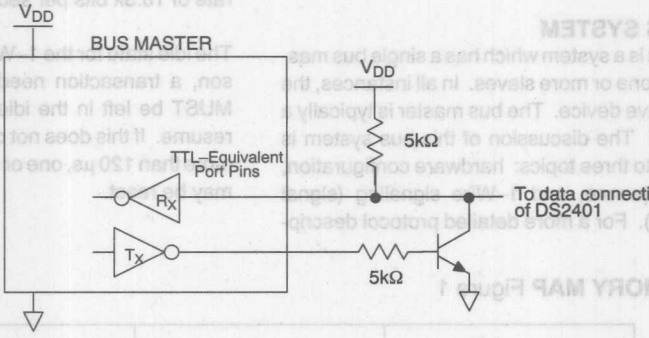


BUS MASTER CIRCUIT Figure 3

A) Open Drain



B) Standard TTL



TRANSACTION SEQUENCE

The sequence for accessing the DS2401 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2401 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 4):

Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS2401's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2401 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The DS2401 Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS2400, which will only respond to a 0Fh command word with its 64–bit ROM data.

Match ROM [55h] / Skip ROM [CCh]

The complete 1–Wire protocol for all Dallas Semiconductor Touch Memories contains a Match ROM and a Skip ROM command. (See the Book of DS19xx Touch Memory Standards.) Since the DS2401 contains only the 64–bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1–Wire bus if executed. The DS2401 does not interfere with other 1–Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (for example, a DS2401 and DS1994 on the same bus).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM search, including an actual example.

1–WIRE SIGNALLING

The DS2401 requires a strict protocol to insure data integrity. The protocol consists of four types of signalling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1 and read data. All these signals except presence pulse are initiated by the bus master.

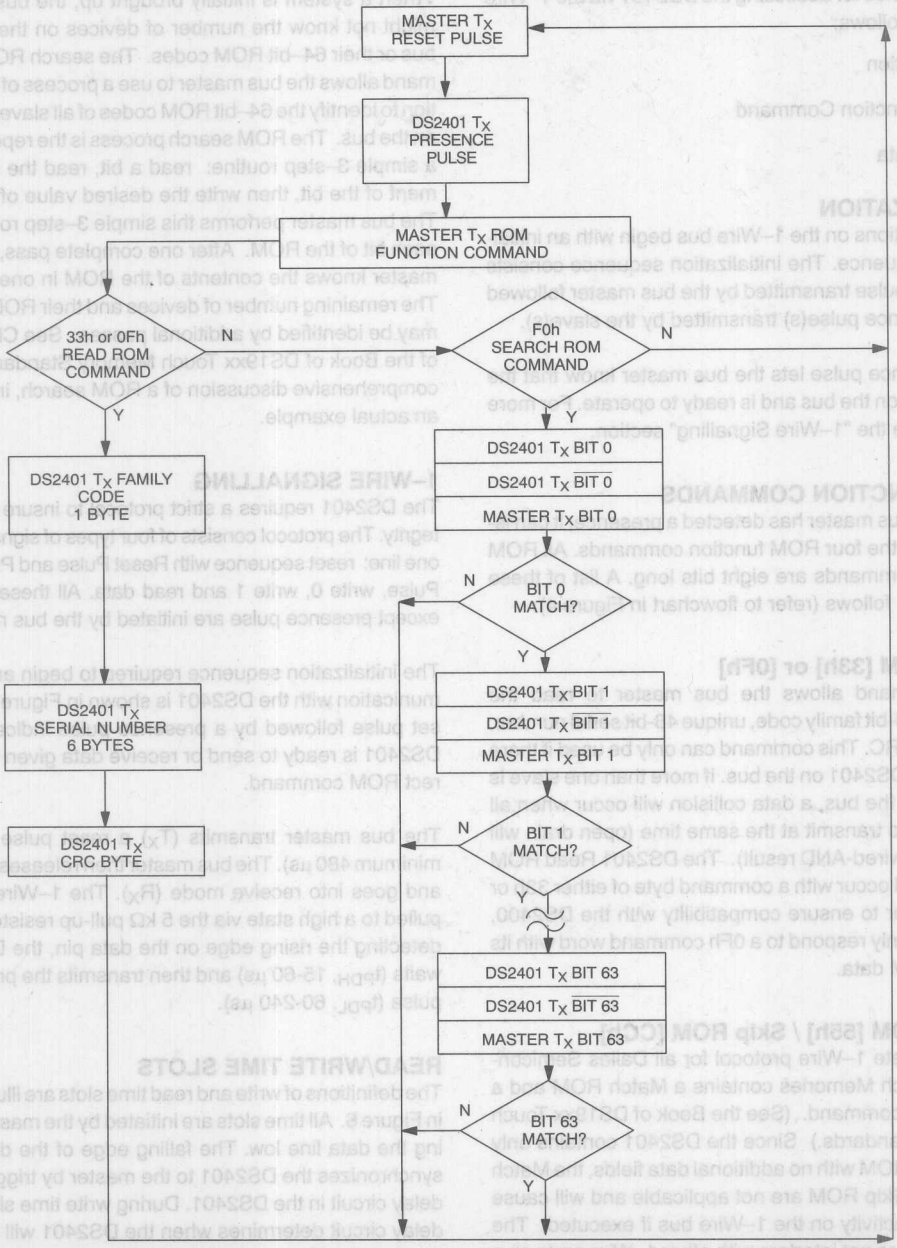
The initialization sequence required to begin any communication with the DS2401 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS2401 is ready to send or receive data given the correct ROM command.

The bus master transmits (T_X) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1–Wire bus is pulled to a high state via the 5 kΩ pull-up resistor. After detecting the rising edge on the data pin, the DS2401 waits (t_{PDH}, 15-60 µs) and then transmits the presence pulse (t_{PDL}, 60-240 µs).

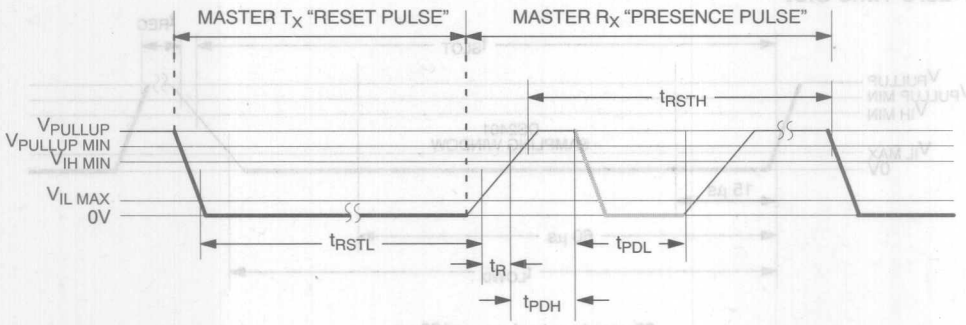
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2401 to the master by triggering a delay circuit in the DS2401. During write time slots, the delay circuit determines when the DS2401 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2401 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the DS2401 will leave the read data time slot unchanged.

ROM FUNCTIONS FLOW CHART Figure 4



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5

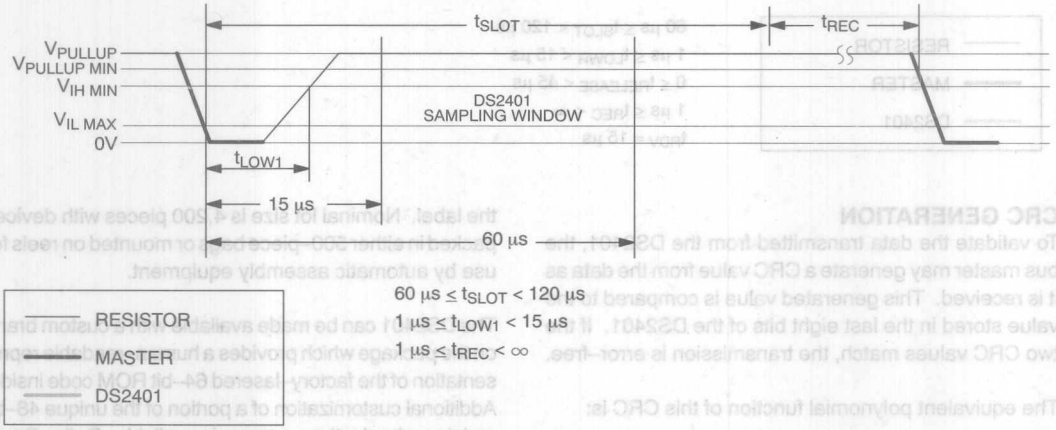


480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

READ/WRITE TIMING DIAGRAM Figure 6

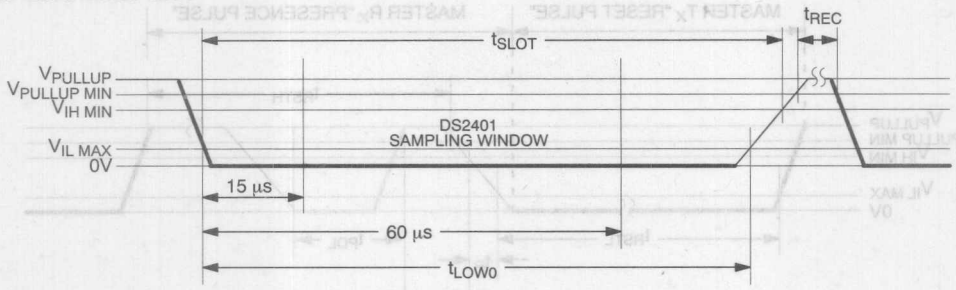
Write–One Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM (cont'd) Figure 6

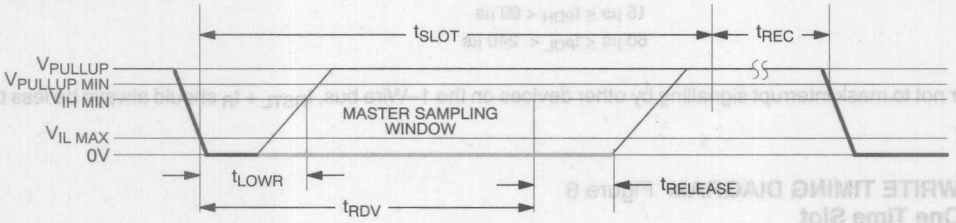
Write–zero Time Slot

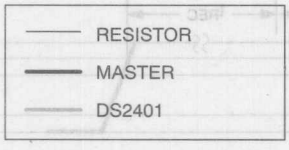


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

CRC GENERATION

To validate the data transmitted from the DS2401, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS2401. If the two CRC values match, the transmission is error–free.

The equivalent polynomial function of this CRC is:

$$CRC = x^8 + x^5 + x^4 + 1$$

For more details, see the Book of DS19xx Touch Memory Standards.

LOT QUANTITIES AND CUSTOM DS2401

The DS2401 is available in registered whole lots sealed in tamper–detecting cartons with the beginning number and range which that particular lot spans specified on the label. Nominal lot size is 4,200 pieces with devices packed in either 500–piece bags or mounted on reels for use by automatic assembly equipment.

The DS2401 can be made available with a custom brand on the package which provides a human–readable representation of the factory–lasered 64–bit ROM code inside. Additional customization of a portion of the unique 48–bit serial number by the customer is available. Dallas Semiconductor will register and assign a specific customer ID in the 12 most significant bits of the 48–bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non–selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your Dallas Semiconductor sales representative for more information.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	10
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum (15 µs total from falling edge on 1–Wire bus).
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the I/O line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signalling, otherwise it could mask or conceal interrupt pulses if this device is used in parallel with a DS2404 or DS1994.

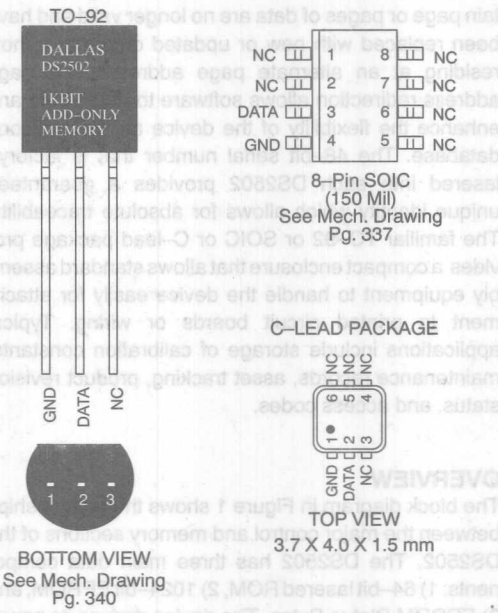
DALLAS SEMICONDUCTOR

DS2502
1Kbit Add–Only Memory

FEATURES

- 1024–bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Built–in multidrop controller ensures compatibility with other MicroLAN™ products
- EPROM partitioned into four 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- 8–bit family code specifies DS2502 communications requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Low cost TO–92 or 8–pin SOIC and C–lead surface mount packages
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –40°C to +85°C

PIN ASSIGNMENT



ORDERING INFORMATION

DS2502	TO–92 package
DS2502S	8–pin SOIC package
DS2502P	6–pin C–lead package
DS2502T	Tape & Reel version of DS2502
DS2502Y	Tape & Reel version of DS2502S
DS2502V	Tape & Reel version of DS2502P

SILICON LABEL™ DESCRIPTION

The DS2502 1K–bit Add–Only Memory identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2502 consists of a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit Family Code (09h) plus 1K–bit of EPROM which is user–programmable. The power to program and read the DS2502 is derived entirely from the 1–Wire

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communication line. Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write–protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a standalone database. The 48–bit serial number that is factory–lasered into each DS2502 provides a guaranteed unique identity which allows for absolute traceability. The familiar TO–92 or SOIC or C–lead package provides a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, maintenance records, asset tracking, product revision status, and access codes.

OVERVIEW

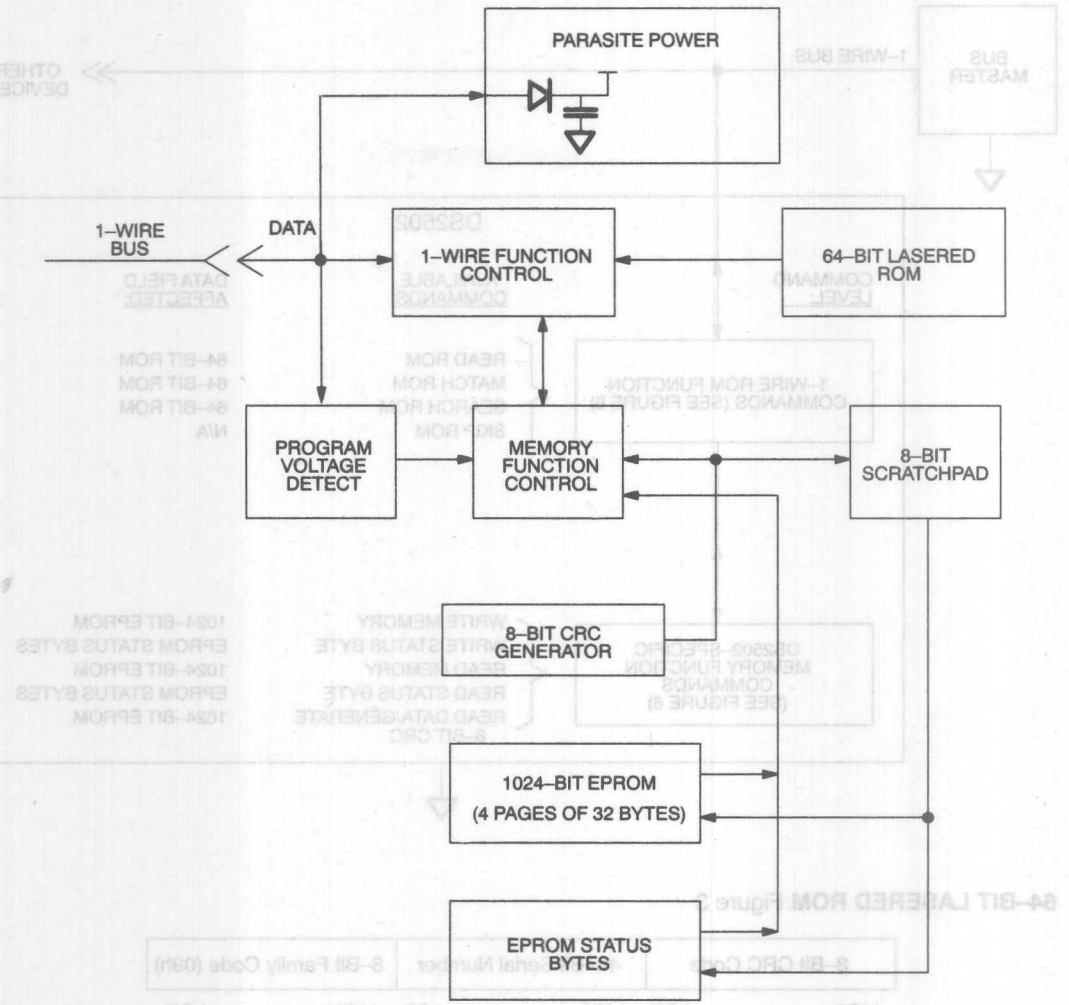
The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2502. The DS2502 has three main data components: 1) 64–bit lasered ROM, 2) 1024–bit EPROM, and 3) EPROM Status Bytes. The device derives its power for read operations entirely from the 1–Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1–Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1–Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1–Wire line a special high voltage detect circuit within the DS2502 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1–Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 9. After a ROM Function Command is successfully executed, the memory functions that operate on the EPROM portions of the DS2502 become accessible and the bus master may issue any one of the five Memory Function Commands specific to the DS2502 to read or program the various data fields. The protocol for these Memory Function Commands is described in Figure 6. All data is read and written least significant bit first.

64–BIT LASERED ROM

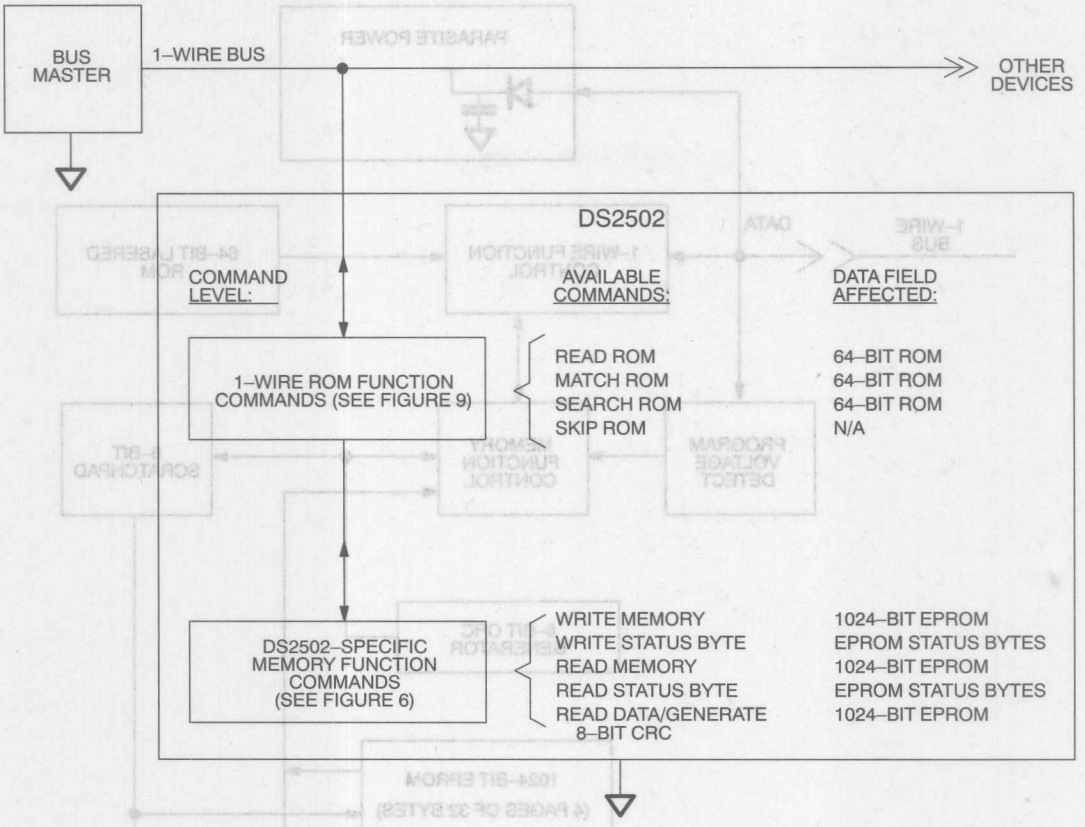
Each DS2502 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 64–bit ROM and ROM Function Control section allow the DS2502 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The memory functions required to read and program the EPROM sections of the DS2502 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 9). The 1–Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS2502 (Figure 6).

The 1–Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Figure 4 shows a hardware implementation of this CRC generator. Additional information about the Dallas Semiconductor 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards. The shift register acting as the CRC accumulator is initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the eighth bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeroes.

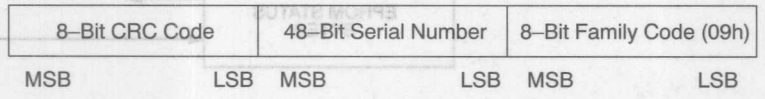
DS2502 BLOCK DIAGRAM Figure 1



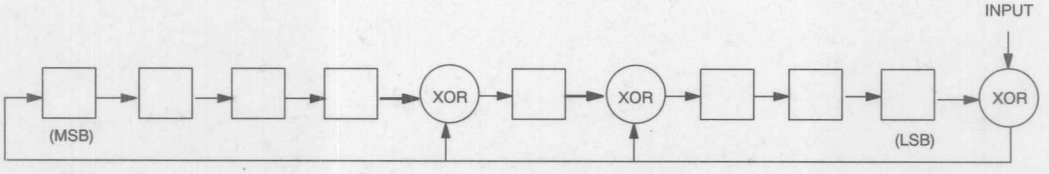
HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2



64–BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



1024–BIT EPROM

The memory map in Figure 5 shows the 1024–bit EPROM section of the DS2502 which is configured as four pages of 32 bytes each. The 8–bit scratchpad is an additional register that acts as a buffer when programming the memory. Data is first written to the scratchpad and then verified by reading an 8–bit CRC from the DS2502 that confirms proper receipt of the data. If the buffer contents are correct, a programming voltage should be applied and the byte of data will be written into the selected address in memory. This process insures data integrity when programming the memory. The details for reading and programming the 1024–bit EPROM portion of the DS2502 are given in the Memory Function Commands section.

EPROM STATUS BYTES

In addition to the 1024 bits of data memory the DS2502 provides 64 bits of Status Memory accessible with separate commands.

The EPROM Status Bytes can be read or programmed to indicate various conditions to the software interrogating the DS2502. The first byte of the EPROM Status Memory contains the Write Protect Page bits which inhibit programming of the corresponding page in the 1024–bit main memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page byte, the entire 32 byte page that corresponds to that bit can no longer be altered but may still be read.

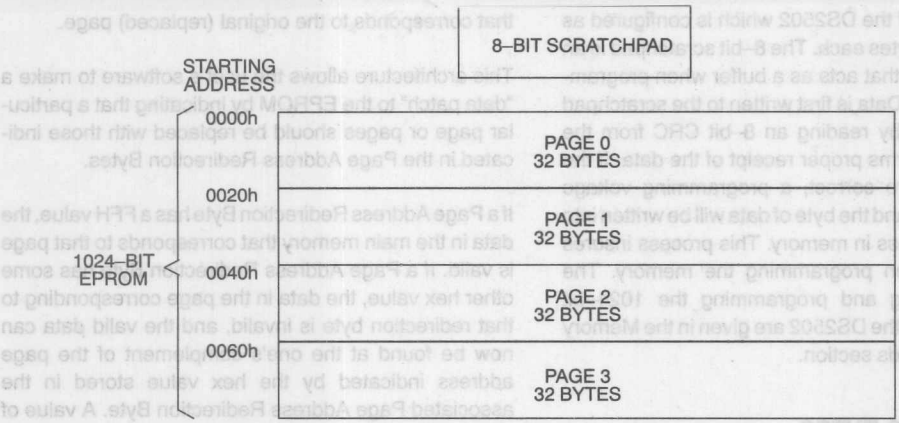
The next four bytes of the EPROM Status Memory contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 1024–bit EPROM section have been invalidated and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS2502 makes no decisions based on the contents of the Page Address Redirection Bytes. These additional bytes of Status EPROM allow for the redirection of an entire page to another page address, indicating that the data in the original page is no longer considered relevant or valid. With EPROM technology, bits within a page can be changed from a logical 1 to a logical 0 by programming, but cannot be changed back. Therefore, it is not possible to simply rewrite a page if the data requires changing or updating, but with space permitting, an entire page of data can be redirected to another page within the DS2502 by writing the one's complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page.

This architecture allows the user's software to make a "data patch" to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes.

If a Page Address Redirection Byte has a FFH value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value, the data in the page corresponding to that redirection byte is invalid, and the valid data can now be found at the one's complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDH in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. The details for reading and programming the EPROM status memories portion of the DS2502 is given in the Memory Function Commands section.

MEMORY FUNCTION COMMANDS

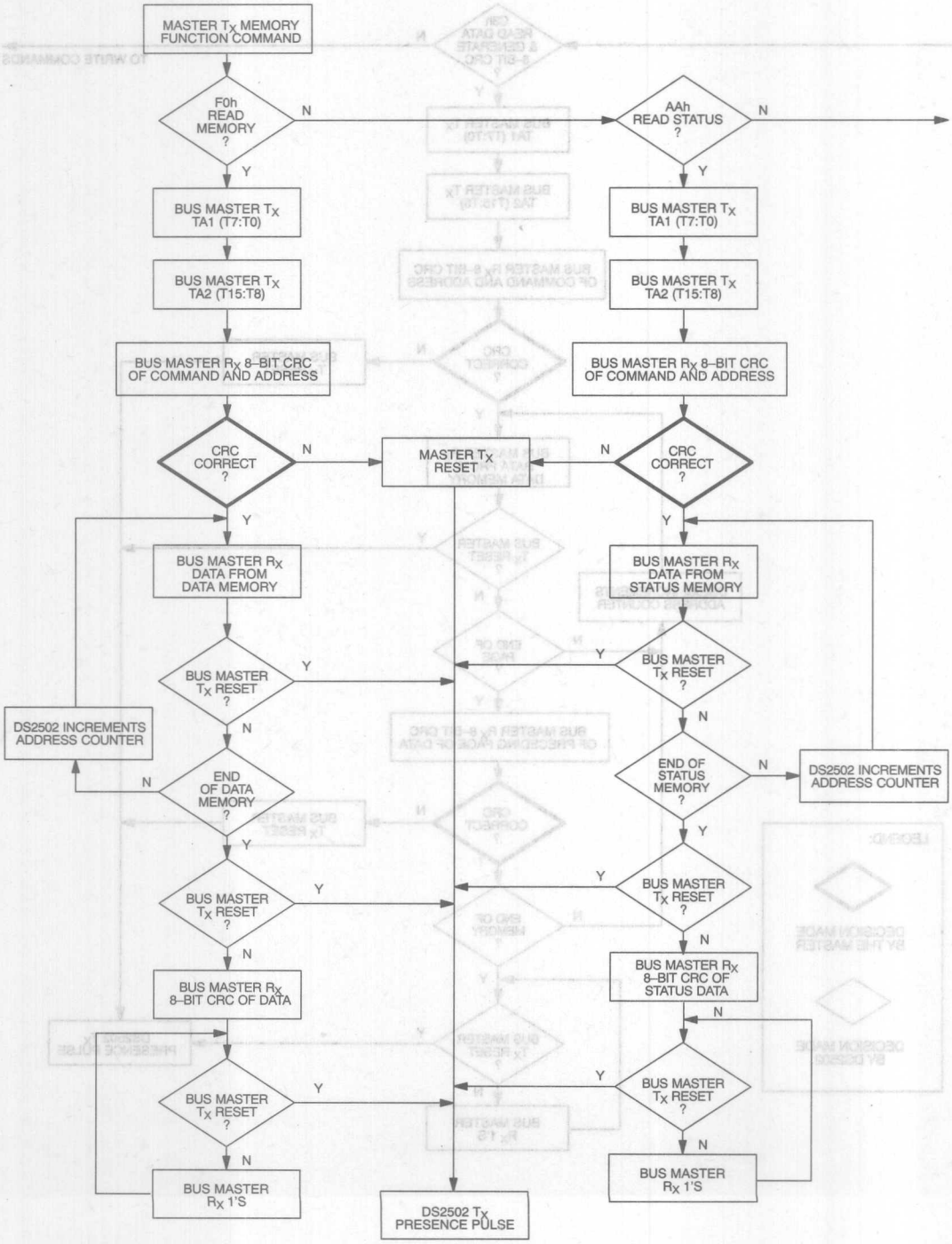
The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the various data fields within the DS2502. The Memory Function Control section, 8–bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three–byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field. The command byte indicates if the device is to be read or written. Writing data involves not only issuing the correct command sequence but also providing a 12 volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS2502 and received back by the bus master are sent least significant bit first.



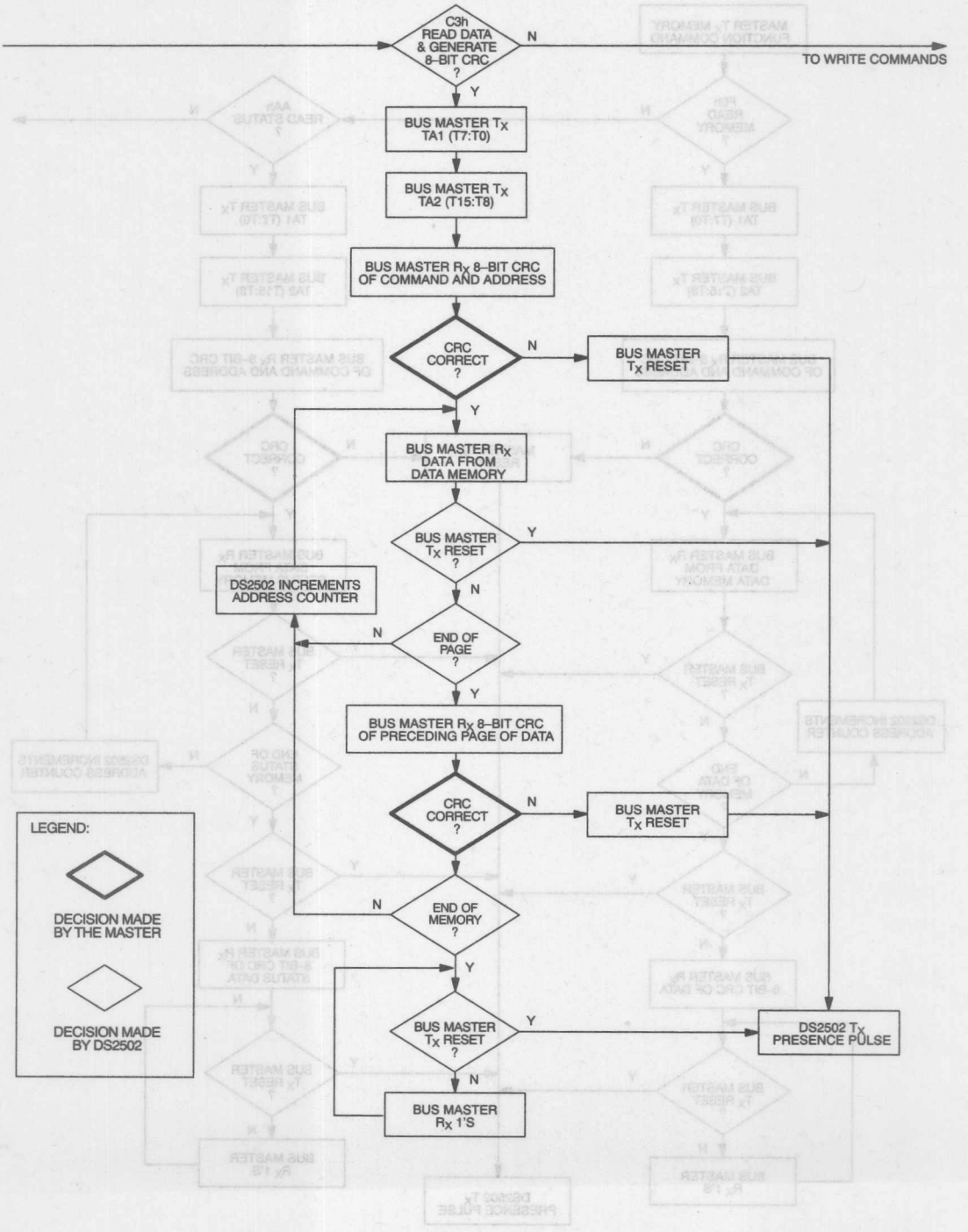
EPROM STATUS BYTES

ADDRESS:	0007h (MSB)	0006h	0005h	0004h	0003h	0002h	0001h	0000h (LSB)
	7	6	5	4	3	2	1	0
	FACTORY–PROGRAMMED 00h	RESERVED FOR FUTURE EXPANSION		PAGE ADDRESS REDIRECTION BYTE FOR PAGE 3	PAGE ADDRESS REDIRECTION BYTE FOR PAGE 2	PAGE ADDRESS REDIRECTION BYTE FOR PAGE 1	PAGE ADDRESS REDIRECTION BYTE FOR PAGE 0	BIT 0 = WRITE PROTECT PAGE 0
								BIT 1 = WRITE PROTECT PAGE 1
								BIT 2 = WRITE PROTECT PAGE 2
								BIT 3 = WRITE PROTECT PAGE 3
								BIT 4–7 = RESERVED

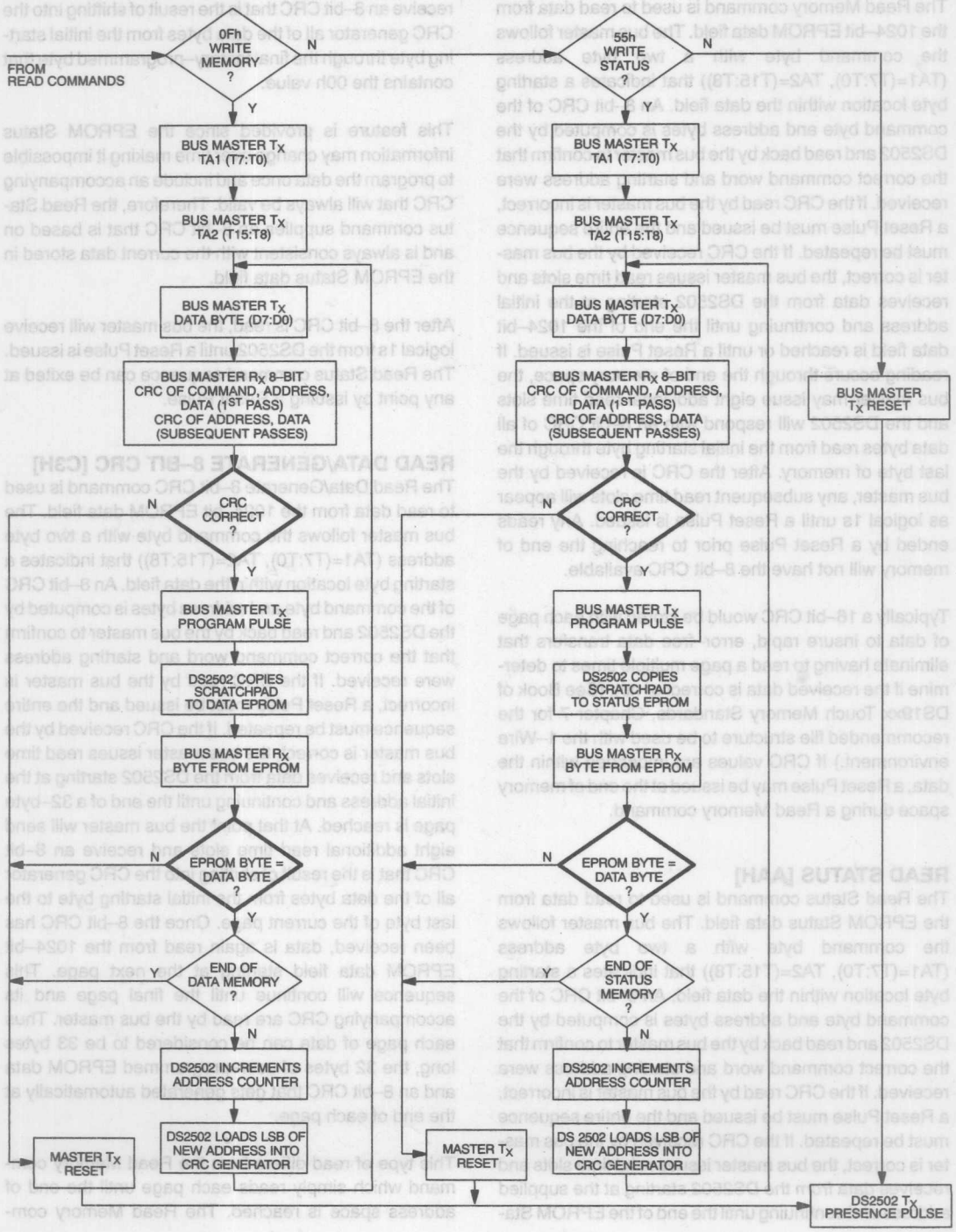
MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION FLOW CHART (cont'd) Figure 6



MEMORY FUNCTION FLOW CHART (cont'd) Figure 6



READ MEMORY [F0H]

The Read Memory command is used to read data from the 1024–bit EPROM data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8–bit CRC of the command byte and address bytes is computed by the DS2502 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2502 starting at the initial address and continuing until the end of the 1024–bit data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue eight additional read time slots and the DS2502 will respond with an 8–bit CRC of all data bytes read from the initial starting byte through the last byte of memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 8–bit CRC available.

Typically a 16–bit CRC would be stored with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Book of DS19xx Touch Memory Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment.) If CRC values are imbedded within the data, a Reset Pulse may be issued at the end of memory space during a Read Memory command.

READ STATUS [AAH]

The Read Status command is used to read data from the EPROM Status data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8–bit CRC of the command byte and address bytes is computed by the DS2502 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2502 starting at the supplied address and continuing until the end of the EPROM Status data field is reached. At that point the bus master will receive an 8–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte through the final factory–programmed byte that contains the 00h value.

This feature is provided since the EPROM Status information may change over time making it impossible to program the data once and include an accompanying CRC that will always be valid. Therefore, the Read Status command supplies an 8–bit CRC that is based on and is always consistent with the current data stored in the EPROM Status data field.

After the 8–bit CRC is read, the bus master will receive logical 1s from the DS2502 until a Reset Pulse is issued. The Read Status command sequence can be exited at any point by issuing a Reset Pulse.

READ DATA/GENERATE 8–BIT CRC [C3H]

The Read Data/Generate 8–bit CRC command is used to read data from the 1024–bit EPROM data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8–bit CRC of the command byte and address bytes is computed by the DS2502 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2502 starting at the initial address and continuing until the end of a 32–byte page is reached. At that point the bus master will send eight additional read time slots and receive an 8–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page. Once the 8–bit CRC has been received, data is again read from the 1024–bit EPROM data field starting at the next page. This sequence will continue until the final page and its accompanying CRC are read by the bus master. Thus each page of data can be considered to be 33 bytes long, the 32 bytes of user–programmed EPROM data and an 8–bit CRC that gets generated automatically at the end of each page.

This type of read differs from the Read Memory command which simply reads each page until the end of address space is reached. The Read Memory com-

mand only generates an 8–bit CRC at the end of memory space that often might be ignored, since in many applications the user would store a 16–bit CRC with the data itself in each page of the 1024–bit EPROM data field at the time the page was programmed.

The Read Data/Generate 8–bit CRC command provides an alternate read capability for applications that are "bit–oriented" rather than "page–oriented" where the 1024–bit EPROM information may change over time within a page boundary making it impossible to program the page once and include an accompanying CRC that will always be valid. Therefore, the Read Data/Generate 8–Bit CRC command concludes each page with the DS2502 generating and supplying an 8–bit CRC that is based on and therefore is always consistent with the current data stored in each page of the 1024–bit EPROM data field. After the 8–bit CRC of the last page is read, the bus master will receive logical 1s from the DS2502 until a Reset Pulse is issued. The Read Data/Generate 8–Bit CRC command sequence can be exited at any point by issuing a Reset Pulse.

WRITE MEMORY [0FH]

The Write Memory command is used to program the 1024–bit EPROM data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). An 8–bit CRC of the command byte, address bytes, and data byte is computed by the DS2502 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 µs) is issued by the bus master. Prior to programming, the entire unprogrammed 1024–bit EPROM data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the 1024–bit EPROM will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480 µs programming pulse is applied and the data line returns to a 5 volt level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2502 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM data address. If the EPROM data byte contains 1s in bit positions where the byte issued by the master contains 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2502 EPROM data byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2502 will automatically increment its address counter to select the next byte in the 1024–bit EPROM data field. The least significant byte of the new two–byte address will also be loaded into the 8–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2502 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8–bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the bus master will read this 8–bit CRC from the DS2502 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Memory command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Memory flow chart will generate an 8–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Memory flow chart due to the DS2502 automatically incrementing its address counter will generate an 8–bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2502) is made entirely by the bus master, since the DS2502 will not be able to determine if the 8–bit CRC calculated by the bus master agrees with the 8–bit CRC calculated by the DS2502. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2502. Also note that the DS2502 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the

programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Memory command, incorrect programming could occur within the DS2502. The Write Memory command sequence can be exited at any point by issuing a Reset Pulse.

WRITE STATUS [55H]

The Write Status command is used to program the EPROM Status data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of status data (D7:D0). An 8–bit CRC of the command byte, address bytes, and data byte is computed by the DS2502 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 μs) is issued by the bus master. Prior to programming, the first seven bytes of the EPROM Status data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM Status data field will be programmed to a logical 0 after the programming pulse has been applied at that byte location. The eighth byte of the EPROM Status Byte data field is factory–programmed to contain 00h.

After the 480 μs programming pulse is applied and the data line returns to a 5 volt level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2502 responds with the data from the selected EPROM Status address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM Status Byte address. If the EPROM Status Byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2502 EPROM Status Byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2502 will automatically increment its address counter to select the next byte in the EPROM Status data field. The least significant byte of the new two–byte address will also be loaded into the 8–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2502 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8–bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the bus master will read this 8–bit CRC from the DS2502 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Status flow chart will generate an 8–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Status flow chart due to the DS2502 automatically incrementing its address counter will generate an 8–bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2502) is made entirely by the bus master, since the DS2502 will not be able to determine if the 8–bit CRC calculated by the bus master agrees with the 8–bit CRC calculated by the DS2502. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2502. Also note that the DS2502 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Status command, incorrect programming could occur within the DS2502. The Write Status command sequence can be ended at any point by issuing a Reset Pulse.

1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2502 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signalling (signal type and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS2502 is an open drain part with an internal circuit equivalent to that shown in Figure 7. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 8a and 8b. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths.

A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second. If the bus master is also required to perform programming of the EPROM portions of the DS2502, a programming supply capable of delivering up to 10 milliamps at 12 volts for 480 µs is required. The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

TRANSACTION SEQUENCE

The sequence for accessing the DS2502 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read/Write Memory/Status

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2502 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

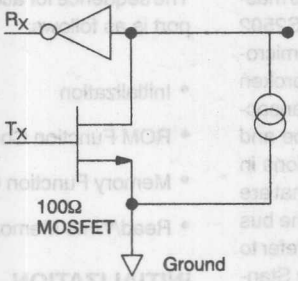
Read ROM [33H]

This command allows the bus master to read the DS2502's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can be used only if there is a single DS2502 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result).

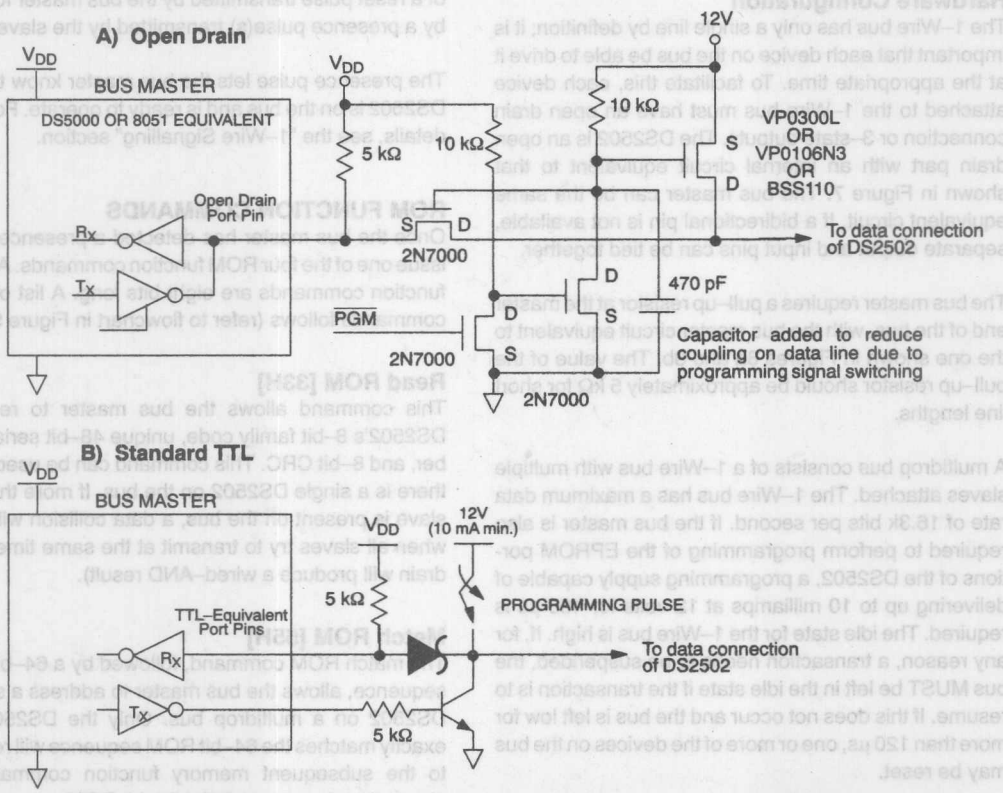
Match ROM [55H]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS2502 on a multidrop bus. Only the DS2502 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

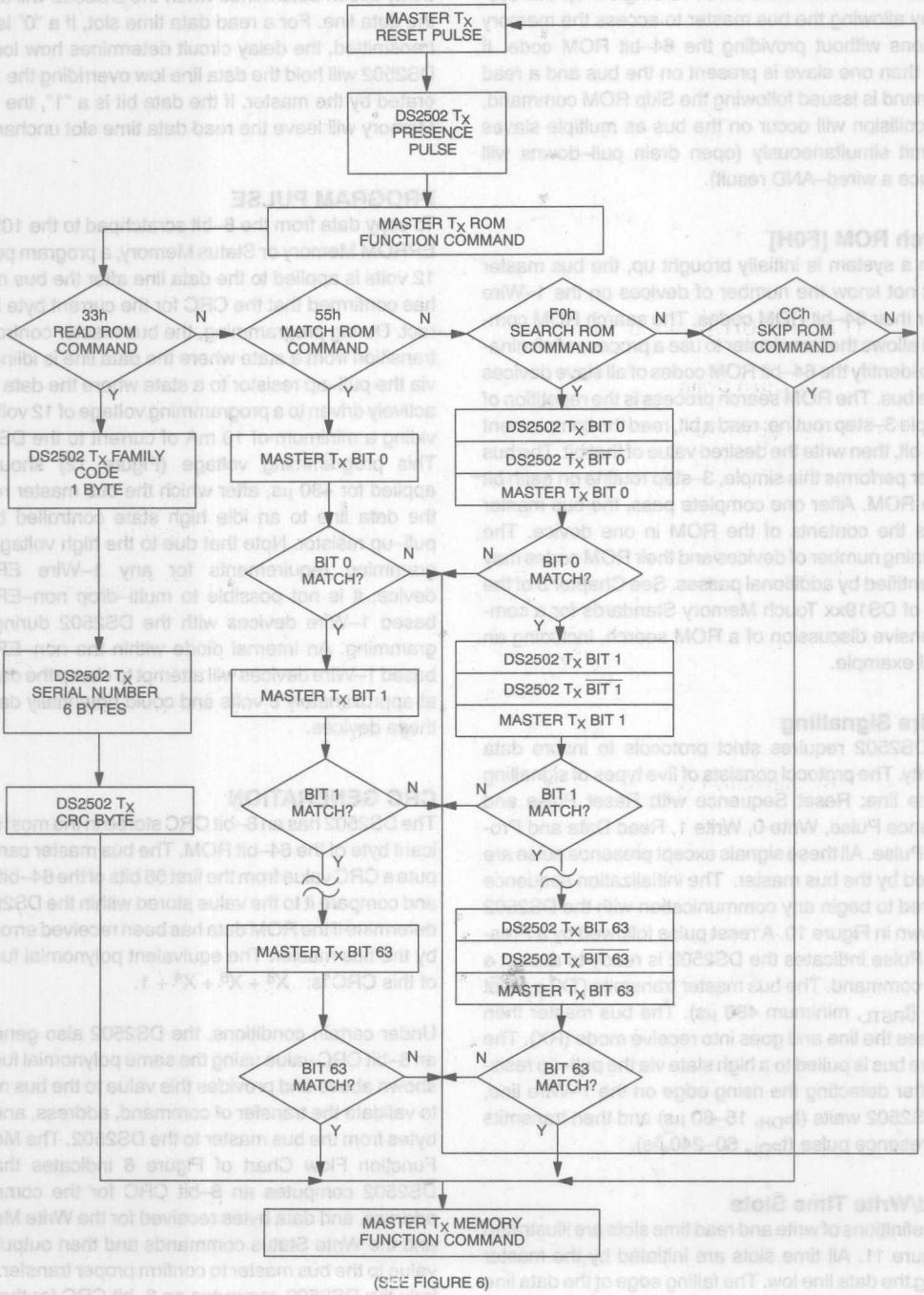
DS2502 EQUIVALENT CIRCUIT Figure 7



BUS MASTER CIRCUIT Figure 8



ROM FUNCTIONS FLOW CHART Figure 9



Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM search, including an actual example.

1–Wire Signalling

The DS2502 requires strict protocols to insure data integrity. The protocol consists of five types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and Program Pulse. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS2502 is shown in Figure 10. A reset pulse followed by a Presence Pulse indicates the DS2502 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the 1–Wire line, the DS2502 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2502 to the master by triggering a delay circuit in the DS2502. During write time slots, the delay circuit determines when the DS2502 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2502 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8–bit scratchpad to the 1024–bit EPROM Memory or Status Memory, a program pulse of 12 volts is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pull–up resistor to a state where the data line is actively driven to a programming voltage of 12 volts providing a minimum of 10 mA of current to the DS2502. This programming voltage (Figure 12) should be applied for 480 µs, after which the bus master returns the data line to an idle high state controlled by the pull–up resistor. Note that due to the high voltage programming requirements for any 1–Wire EPROM device, it is not possible to multi–drop non–EPROM based 1–Wire devices with the DS2502 during programming. An internal diode within the non–EPROM based 1–Wire devices will attempt to clamp the data line at approximately 8 volts and could potentially damage these devices.

CRC GENERATION

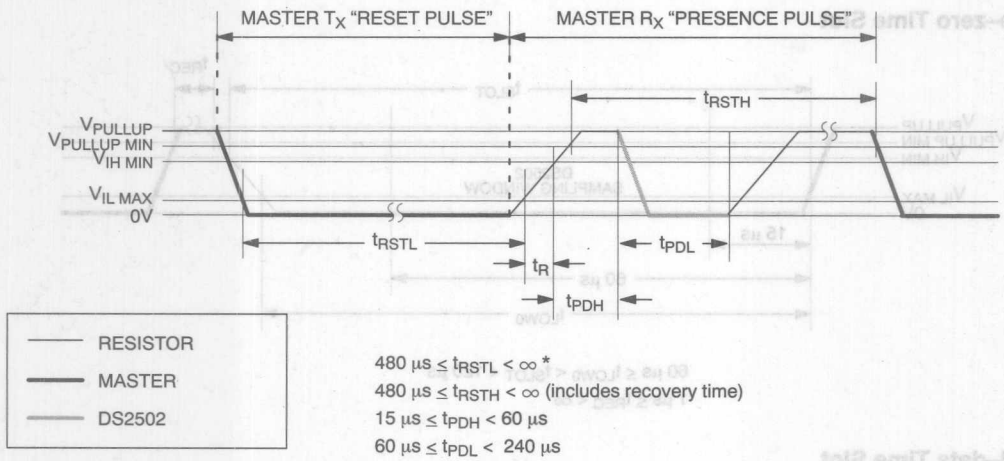
The DS2502 has an 8–bit CRC stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS2502 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$.

Under certain conditions, the DS2502 also generates an 8–bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of command, address, and data bytes from the bus master to the DS2502. The Memory Function Flow Chart of Figure 6 indicates that the DS2502 computes an 8–bit CRC for the command, address, and data bytes received for the Write Memory and the Write Status commands and then outputs this value to the bus master to confirm proper transfer. Similarly the DS2502 computes an 8–bit CRC for the com-

mand and address bytes received from the bus master for the Read Memory, Read Status, and Read Data/ Generate 8–Bit CRC commands to confirm that these bytes have been received correctly. The CRC generator on the DS2502 is also used to provide verification of error–free data transfer as each page of data from the 1024–bit EPROM is sent to the bus master during a Read Data/Generate 8–Bit CRC command, and for the eight bytes of information in the status memory field.

In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8–bit CRC value stored in the 64–bit ROM portion of the DS2502 (for ROM reads) or the 8–bit CRC value computed within the DS2502. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS2502 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2502 does not match the value generated by the bus master. Proper use of the CRC as outlined in the flow chart of Figure 6 can result in a communication channel with a very high level of integrity. For more details on generating CRC values including example implementations in both hardware and software, see the Book of DS19xx Touch Memory Standards.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10

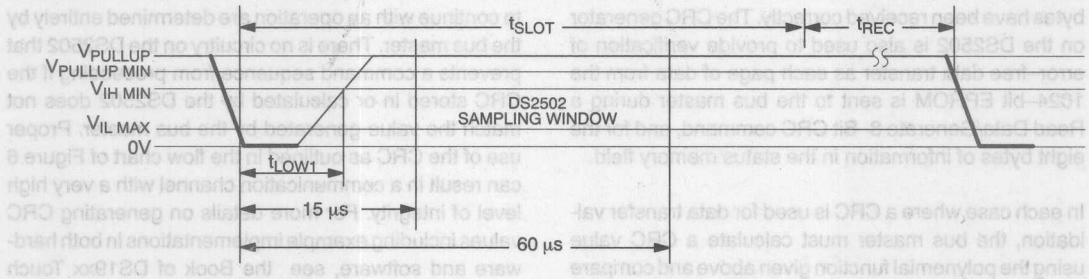


480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

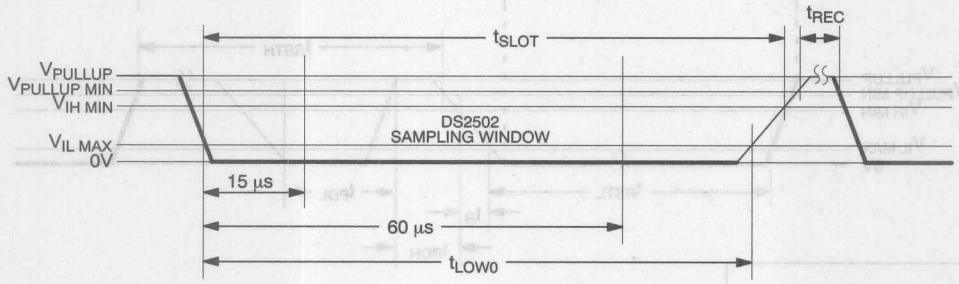
READ/WRITE TIMING DIAGRAM Figure 11

Write–one Time Slot



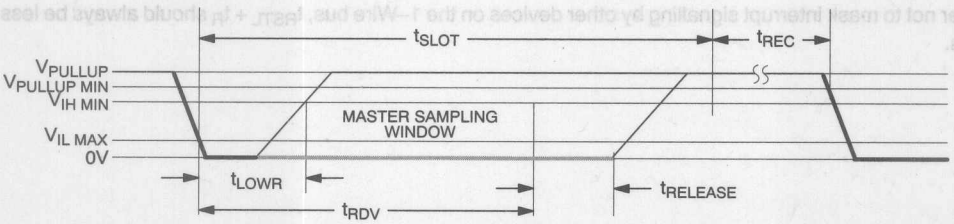
60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

Write–zero Time Slot



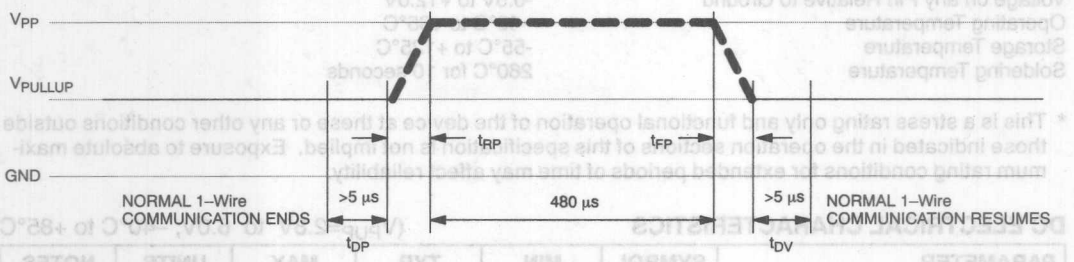
60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs
1 µs ≤ t_{REC} < ∞

Read–data Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOWR} < 15 µs
0 ≤ $t_{RELEASE}$ < 45 µs
1 µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs

PROGRAM PULSE TIMING DIAGRAM Figure 12



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +12.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Voltage @ 10 mA	V_{PP}	11.0	11.5	12.0	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Delay to Program	t_{DP}	5			µs	10
Delay to Verify	t_{DV}	5			µs	10
Program Pulse Width	t_{PP}	480			µs	10
Program Voltage Rise Time	t_{RP}	5			µs	10
Program Voltage Fall Time	t_{FP}	5			µs	10

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. Maximum 1–Wire voltage for programming parameters is 11.5V ± 0.5V; temperature range is –40°C to +85°C.

PRELIMINARY

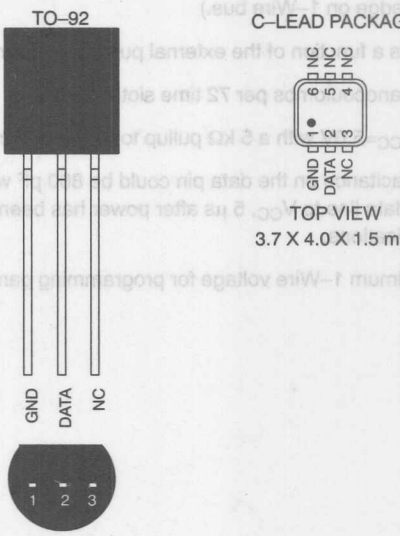
DALLAS SEMICONDUCTOR

DS2505
16Kbit Add–Only Memory

FEATURES

- 16384–bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Built–in multidrop controller ensures compatibility with other MicroLAN™ products
- EPROM partitioned into sixty–four 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- 8–bit family code specifies DS2505 communications requirements to reader
- Presence detector acknowledges when the reader first applies voltage
- Low cost PR35 or 8–pin SOIC surface mount package
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –20°C to +50°C

PIN ASSIGNMENT



BOTTOM VIEW

See Mech. Drawing Pg. 340

ORDERING INFORMATION

DS2505	TO–92 Package
DS2505P	6–pin C–lead Package
DS2505T	Tape & Reel version of DS2505
DS2505V	Tape & Reel version of DS2505P

SILICON LABEL™ DESCRIPTION

The DS2505 16K–bits Add–Only Memory identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2505 consists of a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC,

and an 8–bit Family Code (0BH) plus 16K–bits of user–programmable EPROM. The power to program and read the DS2505 is derived entirely from the 1–Wire communication line. Data is transferred serially via the 1–Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write–protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a standalone database. The 48–bit serial number that is factory–lasered into each DS2505 provides a guaranteed unique identity which allows for absolute traceability. The PR35 and SOIC packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, maintenance records, asset tracking, product revision status and access codes.

OVERVIEW

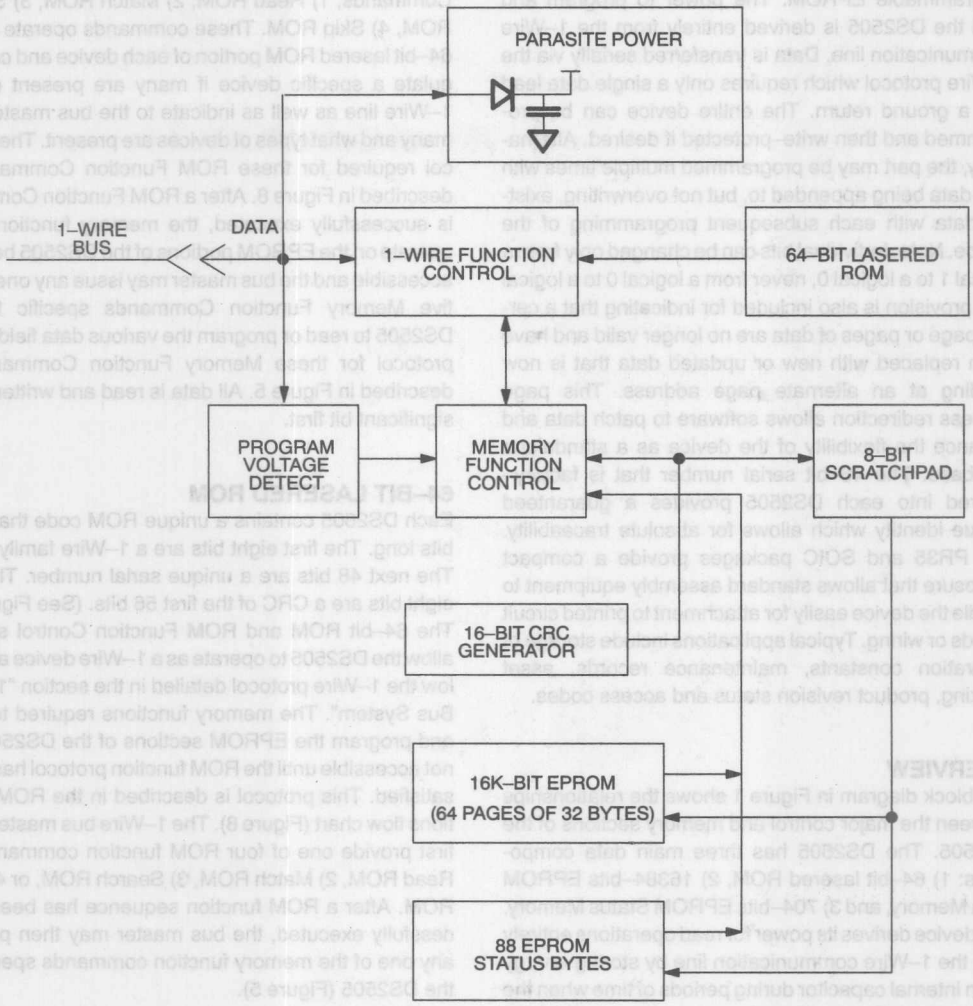
The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2505. The DS2505 has three main data components: 1) 64–bit lasered ROM, 2) 16384–bits EPROM Data Memory, and 3) 704–bits EPROM Status Memory. The device derives its power for read operations entirely from the 1–Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1–Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1–Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1–Wire line a special high voltage detect circuit within the DS2505 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1–Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 8. After a ROM Function Command is successfully executed, the memory functions that operate on the EPROM portions of the DS2505 become accessible and the bus master may issue any one of the five Memory Function Commands specific to the DS2505 to read or program the various data fields. The protocol for these Memory Function Commands is described in Figure 5. All data is read and written least significant bit first.

64–BIT LASERED ROM

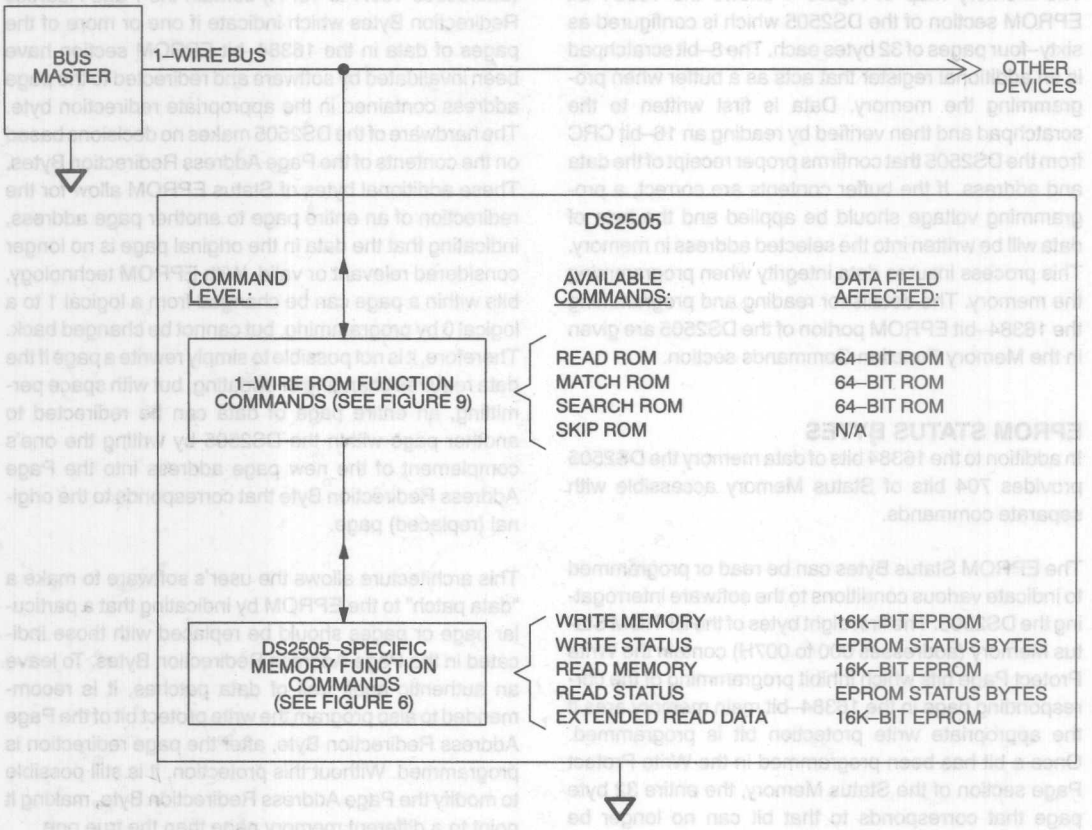
Each DS2505 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 64–bit ROM and ROM Function Control section allow the DS2505 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The memory functions required to read and program the EPROM sections of the DS2505 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 8). The 1–Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS2505 (Figure 5).

The 1–Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1–Wire Cyclic Redundancy Check is available in the Book of DS19xx Touch Memory Standards. The shift register acting as the CRC accumulator is initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the eighth bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeroes.

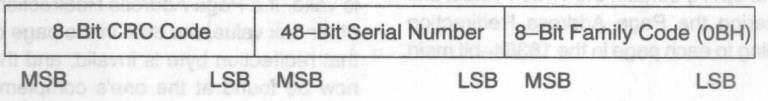
DS2505 BLOCK DIAGRAM Figure 1



HIERARCHICAL STRUCTURE FOR 1–WIRE PROTOCOL Figure 2



64–BIT LASERED ROM Figure 3



16384–BITS EPROM

The memory map in Figure 4 shows the 16384–bit EPROM section of the DS2505 which is configured as sixty–four pages of 32 bytes each. The 8–bit scratchpad is an additional register that acts as a buffer when programming the memory. Data is first written to the scratchpad and then verified by reading an 16–bit CRC from the DS2505 that confirms proper receipt of the data and address. If the buffer contents are correct, a programming voltage should be applied and the byte of data will be written into the selected address in memory. This process insures data integrity when programming the memory. The details for reading and programming the 16384–bit EPROM portion of the DS2505 are given in the Memory Function Commands section.

EPROM STATUS BYTES

In addition to the 16384 bits of data memory the DS2505 provides 704 bits of Status Memory accessible with separate commands.

The EPROM Status Bytes can be read or programmed to indicate various conditions to the software interrogating the DS2505. The first eight bytes of the EPROM Status Memory (addresses 000 to 007H) contain the Write Protect Page bits which inhibit programming of the corresponding page in the 16384–bit main memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page section of the Status Memory, the entire 32 byte page that corresponds to that bit can no longer be altered but may still be read.

The next eight bytes of the EPROM Status Memory (addresses 020 to 027H) contain the Write Protect bits which inhibit altering the Page Address Redirection Byte corresponding to each page in the 16384–bit main memory area.

The following eight bytes within the EPROM Status Memory (addresses 040 to 047H) are reserved for use by the Touch Memory EXecutive TMEX. Their purpose is to indicate which memory pages are already in use. Originally, all of these bits are unprogrammed, indicating that the device does not store any data. As soon as data is written to any page of the device under control of TMEX, the bit inside this bitmap corresponding to that page will be programmed to 0, marking this page as used. These bits are application flags only and have no impact on the internal logic of the DS2505.

The next sixty–four bytes of the EPROM Status Memory (addresses 100H to 13FH) contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 16384–bit EPROM section have been invalidated by software and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS2505 makes no decisions based on the contents of the Page Address Redirection Bytes. These additional bytes of Status EPROM allow for the redirection of an entire page to another page address, indicating that the data in the original page is no longer considered relevant or valid. With EPROM technology, bits within a page can be changed from a logical 1 to a logical 0 by programming, but cannot be changed back. Therefore, it is not possible to simply rewrite a page if the data requires changing or updating, but with space permitting, an entire page of data can be redirected to another page within the DS2505 by writing the one's complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page.

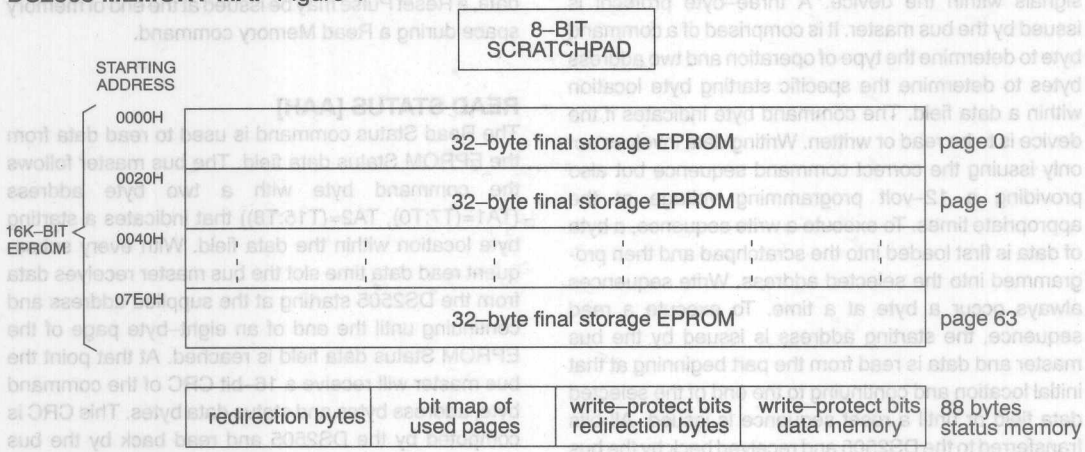
This architecture allows the user's software to make a "data patch" to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes. To leave an authentic audit trail of data patches, it is recommended to also program the write protect bit of the Page Address Redirection Byte, after the page redirection is programmed. Without this protection, it is still possible to modify the Page Address Redirection Byte, making it point to a different memory page than the true one.

If a Page Address Redirection Byte has a FFH value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value, the data in the page corresponding to that redirection byte is invalid, and the valid data can now be found at the one's complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDH in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. The details for reading and programming the EPROM status memory portion of the DS2505 are given in the Memory Function Commands section.

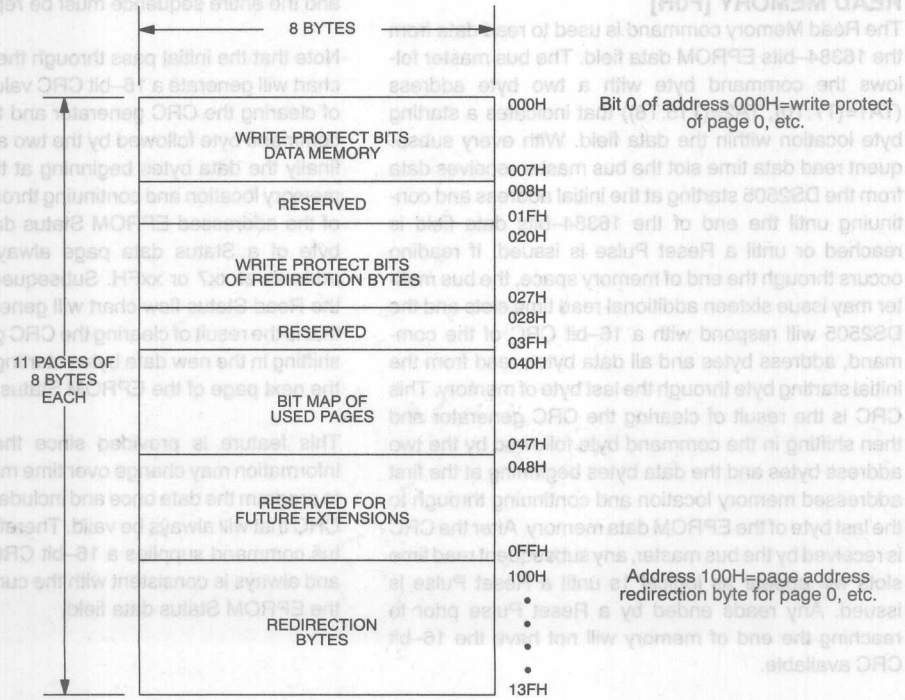
The Status Memory address range of the DS2505 extends from 000 to 13FH. The memory locations 008H to 01FH, 028H to 03FH, 048H to 0FFH and 140H to

7FFH are physically not implemented. Reading these locations will usually result in FFH bytes. Attempts to write to these locations will be ignored. If the bus master sends a starting address higher than 7FFH, the five most significant address bits are set to zeros by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2505 and the CRC calculated by the bus master, indicating an error condition.

DS2505 MEMORY MAP Figure 4



STATUS MEMORY MAP



MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 5) describes the protocols necessary for accessing the various data fields within the DS2505. The Memory Function Control section, 8–bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three–byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field. The command byte indicates if the device is to be read or written. Writing data involves not only issuing the correct command sequence but also providing a 12–volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS2505 and received back by the bus master are sent least significant bit first.

READ MEMORY [F0H]

The Read Memory command is used to read data from the 16384–bits EPROM data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With every subsequent read data time slot the bus master receives data from the DS2505 starting at the initial address and continuing until the end of the 16384–bits data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue sixteen additional read time slots and the DS2505 will respond with a 16–bit CRC of the command, address bytes and all data bytes read from the initial starting byte through the last byte of memory. This CRC is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes and the data bytes beginning at the first addressed memory location and continuing through to the last byte of the EPROM data memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 16–bit CRC available.

Typically a 16–bit CRC would be stored with each page of data to insure rapid, error–free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Book of DS19xx Touch Memory Standards, Chapter 7 for the recommended file structure to be used with the 1–Wire environment.) If CRC values are imbedded within the data, a Reset Pulse may be issued at the end of memory space during a Read Memory command.

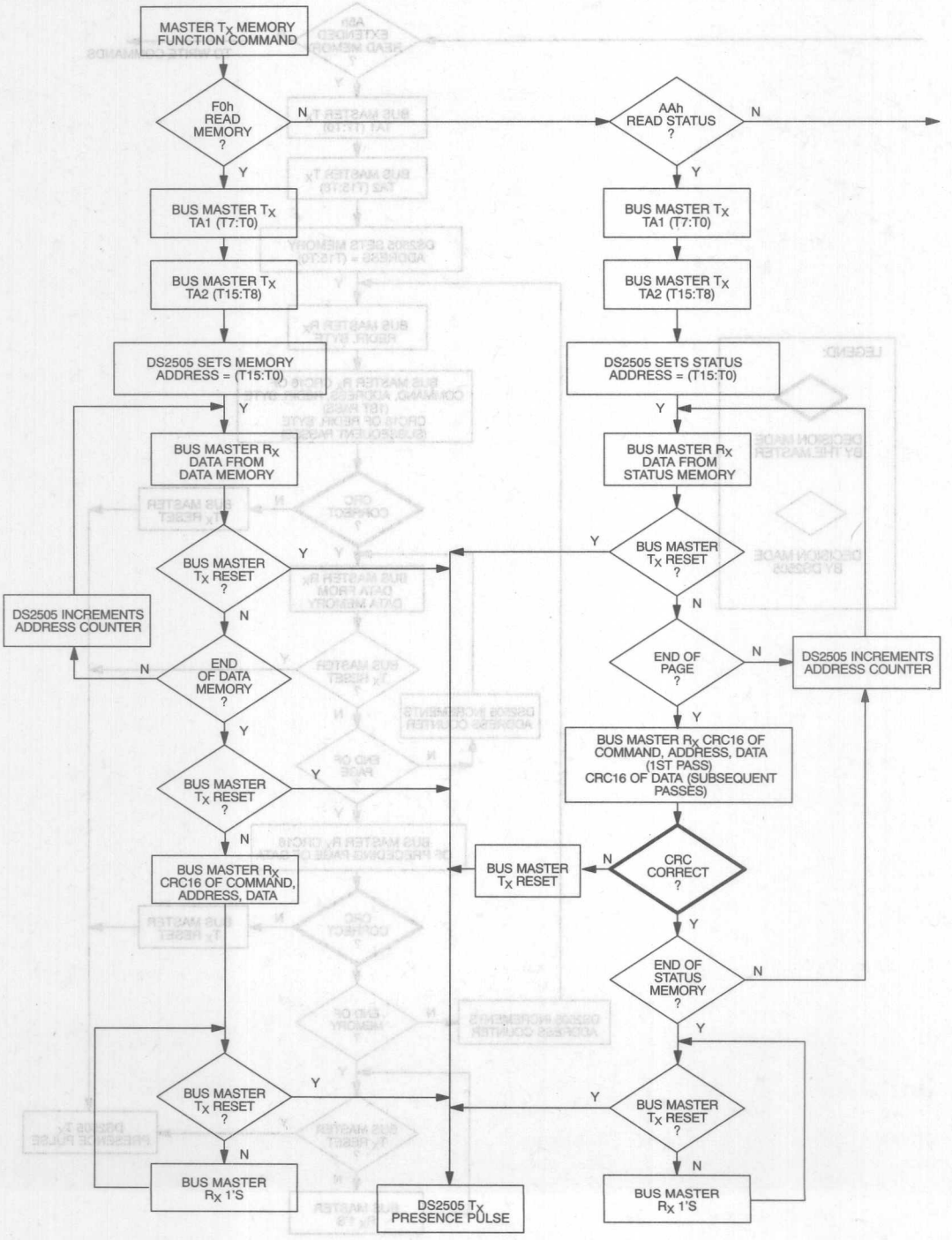
READ STATUS [AAH]

The Read Status command is used to read data from the EPROM Status data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With every subsequent read data time slot the bus master receives data from the DS2505 starting at the supplied address and continuing until the end of an eight–byte page of the EPROM Status data field is reached. At that point the bus master will receive a 16–bit CRC of the command byte, address bytes and status data bytes. This CRC is computed by the DS2505 and read back by the bus master to check if the command word, starting address and data were received correctly. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated.

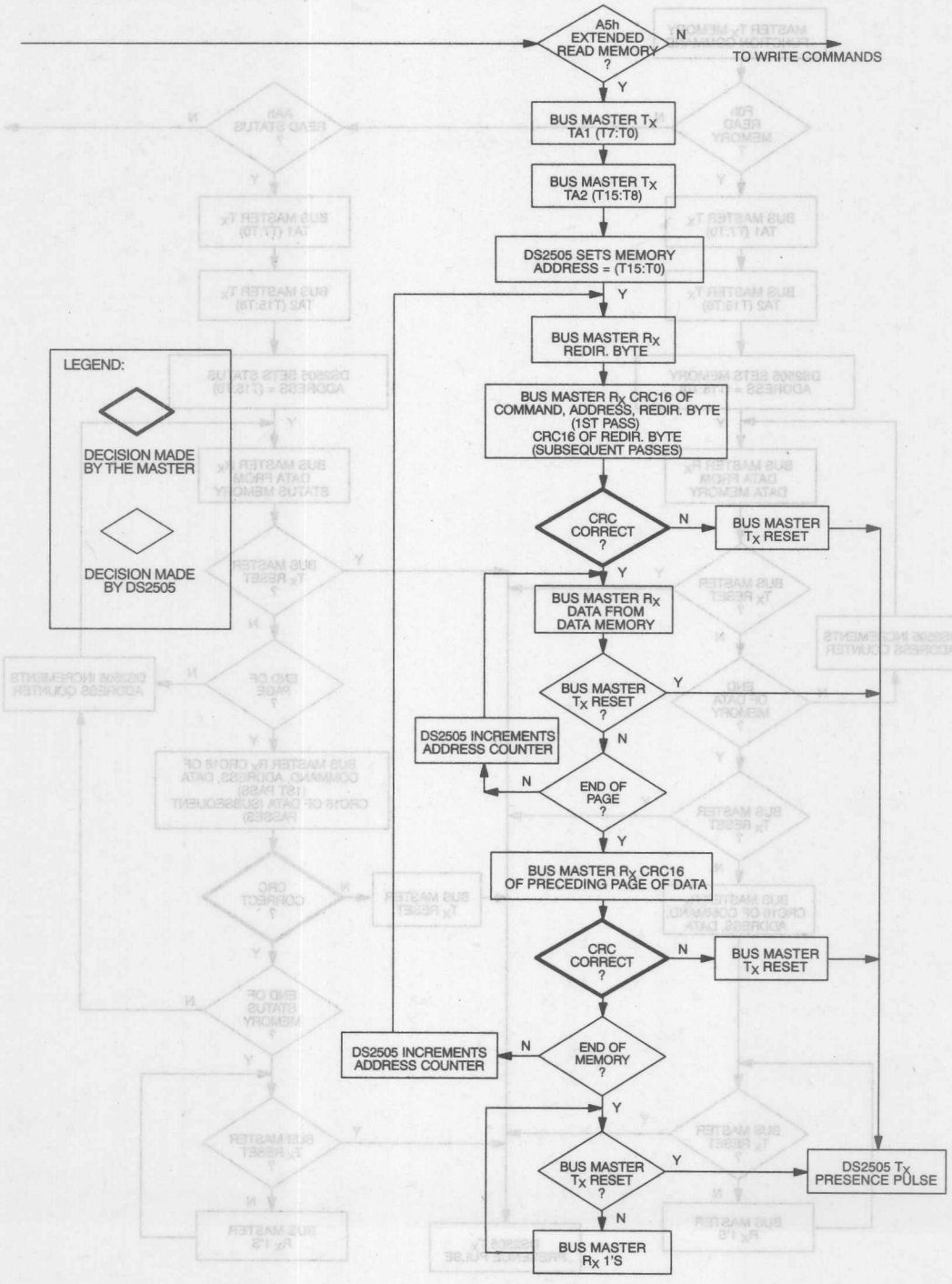
Note that the initial pass through the Read Status flow chart will generate a 16–bit CRC value that is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes, and finally the data bytes beginning at the first addressed memory location and continuing through to the last byte of the addressed EPROM Status data page. The last byte of a Status data page always has an ending address of xx7 or xxFH. Subsequent passes through the Read Status flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes starting at the first byte of the next page of the EPROM Status data field.

This feature is provided since the EPROM Status information may change over time making it impossible to program the data once and include an accompanying CRC that will always be valid. Therefore, the Read Status command supplies a 16–bit CRC that is based on and always is consistent with the current data stored in the EPROM Status data field.

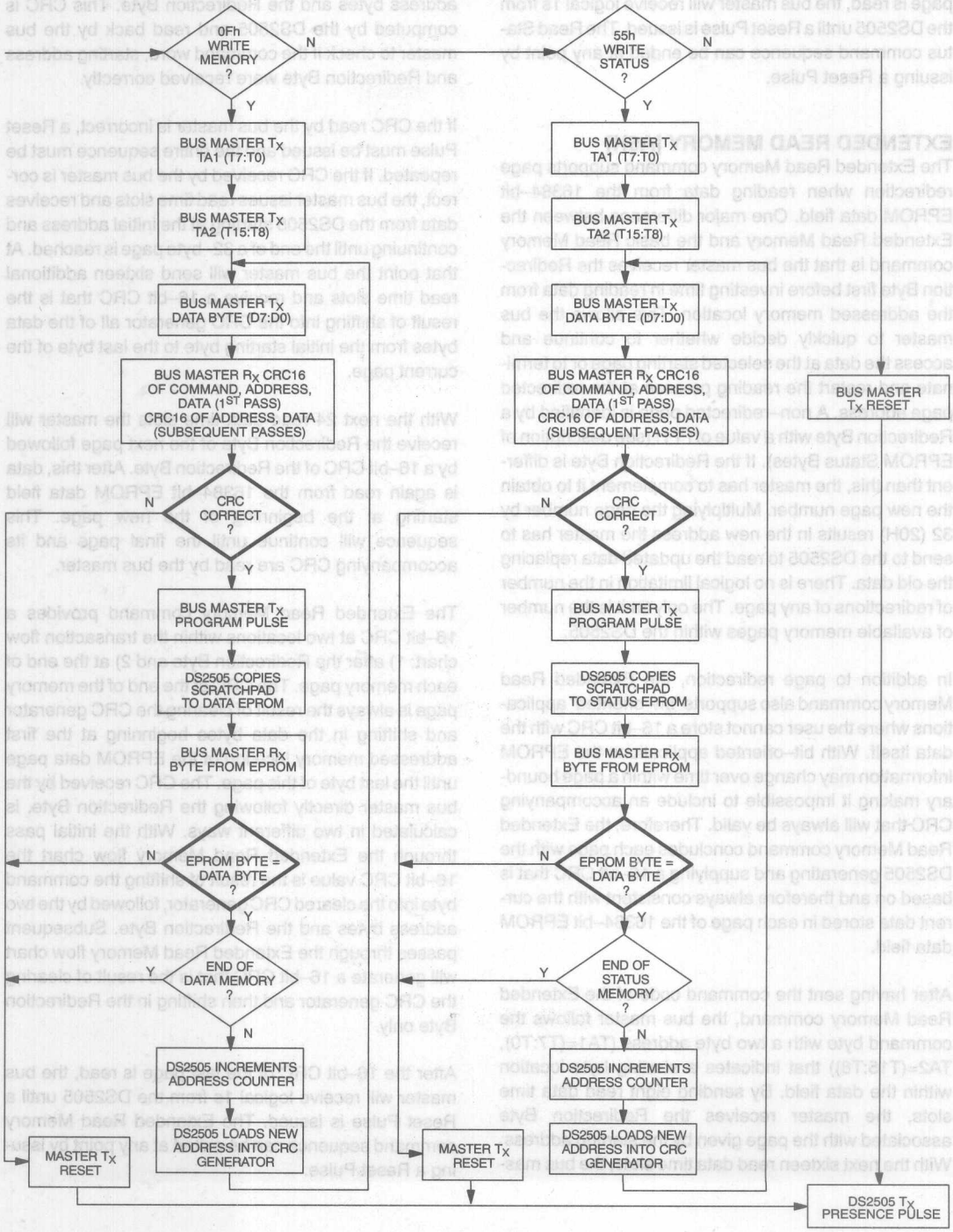
MEMORY FUNCTION FLOW CHART Figure 5



MEMORY FUNCTION FLOW CHART (cont'd) Figure 5



MEMORY FUNCTION FLOW CHART (cont'd) Figure 5



After the 16–bit CRC of the last EPROM Status data page is read, the bus master will receive logical 1s from the DS2505 until a Reset Pulse is issued. The Read Status command sequence can be ended at any point by issuing a Reset Pulse.

EXTENDED READ MEMORY [A5H]

The Extended Read Memory command supports page redirection when reading data from the 16384–bit EPROM data field. One major difference between the Extended Read Memory and the basic Read Memory command is that the bus master receives the Redirection Byte first before investing time in reading data from the addressed memory location. This allows the bus master to quickly decide whether to continue and access the data at the selected starting page or to terminate and restart the reading process at the redirected page address. A non–redirected page is identified by a Redirection Byte with a value of FFH (see description of EPROM Status Bytes). If the Redirection Byte is different than this, the master has to complement it to obtain the new page number. Multiplying the page number by 32 (20H) results in the new address the master has to send to the DS2505 to read the updated data replacing the old data. There is no logical limitation in the number of redirections of any page. The only limit is the number of available memory pages within the DS2505.

In addition to page redirection, the Extended Read Memory command also supports "bit–oriented" applications where the user cannot store a 16–bit CRC with the data itself. With bit–oriented applications the EPROM information may change over time within a page boundary making it impossible to include an accompanying CRC that will always be valid. Therefore, the Extended Read Memory command concludes each page with the DS2505 generating and supplying a 16–bit CRC that is based on and therefore always consistent with the current data stored in each page of the 16384–bit EPROM data field.

After having sent the command code of the Extended Read Memory command, the bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. By sending eight read data time slots, the master receives the Redirection Byte associated with the page given by the starting address. With the next sixteen read data time slots, the bus master receives a 16–bit CRC of the command byte, address bytes and the Redirection Byte. This CRC is computed by the DS2505 and read back by the bus master to check if the command word, starting address and Redirection Byte were received correctly.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2505 starting at the initial address and continuing until the end of a 32–byte page is reached. At that point the bus master will send sixteen additional read time slots and receive a 16–bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page.

With the next 24 read data time slots the master will receive the Redirection Byte of the next page followed by a 16–bit CRC of the Redirection Byte. After this, data is again read from the 16384–bit EPROM data field starting at the beginning of the new page. This sequence will continue until the final page and its accompanying CRC are read by the bus master.

The Extended Read Memory command provides a 16–bit CRC at two locations within the transaction flow chart: 1) after the Redirection Byte and 2) at the end of each memory page. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. The CRC received by the bus master directly following the Redirection Byte, is calculated in two different ways. With the initial pass through the Extended Read Memory flow chart the 16–bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only.

After the 16–bit CRC of the last page is read, the bus master will receive logical 1s from the DS2505 until a Reset Pulse is issued. The Extended Read Memory command sequence can be exited at any point by issuing a Reset Pulse.

WRITE MEMORY [0FH]/SPEED WRITE MEMORY [F3]

The Write Memory command is used to program the 16384–bit EPROM data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). A 16–bit CRC of the command byte, address bytes, and data byte is computed by the DS2505 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

The highest starting address within the DS2505 is 07FFH. If the bus master sends a starting address higher than this, the five most significant address bits are set to zero by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2505 and the CRC calculated by the bus master, indicating an error condition.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 µs) is issued by the bus master. Prior to programming, the entire unprogrammed 16384–bit EPROM data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the 16384–bit EPROM will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480 µs programming pulse is applied and the data line returns to the idle level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2505 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM data address. If the EPROM data byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2505 EPROM data byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2505 will automatically increment its address counter to select the next byte in the 16384–bit EPROM data field. The new two–byte address will also be loaded into the 16–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2505 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16–bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16–bit CRC from the DS2505 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Memory command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Memory flow chart will generate a 16–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Memory flow chart due to the DS2505 automatically incrementing its address counter will generate a 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2505) is made entirely by the bus master, since the DS2505 will not be able to determine if the 16–bit CRC calculated by the bus master agrees with the 16–bit CRC calculated by the DS2505. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2505. Also note that the DS2505 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Memory command, incorrect programming could occur within the DS2505. The Write Memory command sequence can be ended at any point by issuing a Reset Pulse.

To save time when writing more than one consecutive byte of the DS2505's data memory it is possible to omit reading the 16–bit CRC which allows verification of data and address before the data is copied to the EPROM memory. This saves 16 time slots or 976 µs for every byte to be programmed. This speed–programming mode is accessed with the command code F3H instead of 0FH. It follows basically the same flow chart as the

Write Memory command, but skips sending the CRC immediately preceding the program pulse. This command should only be used if the electrical contact between bus master and the DS2505 is firm since a poor contact may result in corrupted data inside the EPROM memory.

WRITE STATUS [55H]/SPEED WRITE STATUS [F5]

The Write Status command is used to program the EPROM Status data field. The bus master will follow the command byte with a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of status data (D7:D0). A 16–bit CRC of the command byte, address bytes, and data byte is computed by the DS2505 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1–Wire bus for 480 µs) is issued by the bus master. Prior to programming, the EPROM Status data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM Status data field will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480 µs programming pulse is applied and the data line returns to the idle level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2505 responds with the data from the selected EPROM Status address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM Status Byte address. If the EPROM Status Byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2505 EPROM Status byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2505 will automatically increment its address counter to select the next byte in the EPROM Status data field. The new two–byte address will also be loaded into the 16–bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2505 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16–bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16–bit CRC from the DS2505 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Status flow chart will generate a 16–bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Status flow chart due to the DS2505 automatically incrementing its address counter will generate a 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2505) is made entirely by the bus master, since the DS2505 will not be able to determine if the 16–bit CRC calculated by the bus master agrees with the 16–bit CRC calculated by the DS2505. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2505. Also note that the DS2505 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Status command, incorrect programming could occur within the DS2505. The Write Status command sequence can be ended at any point by issuing a Reset Pulse.

To save time when writing more than one consecutive byte of the DS2505's status memory it is possible to omit reading the 16–bit CRC which allows verification of data and address before the data is copied to the EPROM memory. This saves 16 time slots or 976 µs for every byte to be programmed. This speed–programming

mode is accessed with the command code F5H instead of 55H. It follows basically the same flow chart as the Write Status command, but skips sending the CRC immediately preceding the program pulse. This command should only be used if the electrical contact between bus master and the DS2505 is firm since a poor contact may result in corrupted data inside the EPROM status memory.

1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2505 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signalling (signal type and timing). A 1–Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS2505 is an open drain part with an internal circuit equivalent to that shown in Figure 6. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 7a and 7b. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths.

A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second. If the bus master is also required to perform programming of the EPROM portions of the DS2505, a programming supply capable of delivering up to 10 milliamps at 12 volts for 480 μs is required. The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 μs, one or more of the devices on the bus may be reset.

Transaction Sequence

The sequence for accessing the DS2505 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read/Write Memory/Status

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2505 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

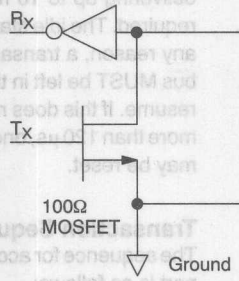
ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 8):

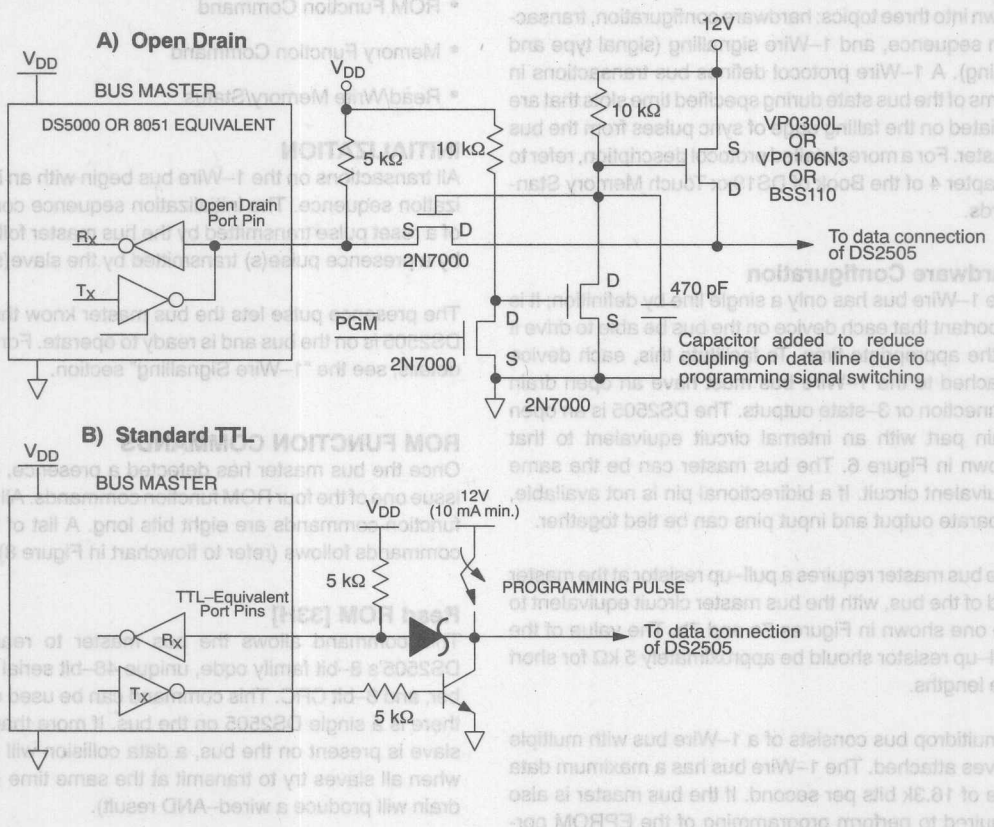
Read ROM [33H]

This command allows the bus master to read the DS2505's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can be used only if there is a single DS2505 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired–AND result).

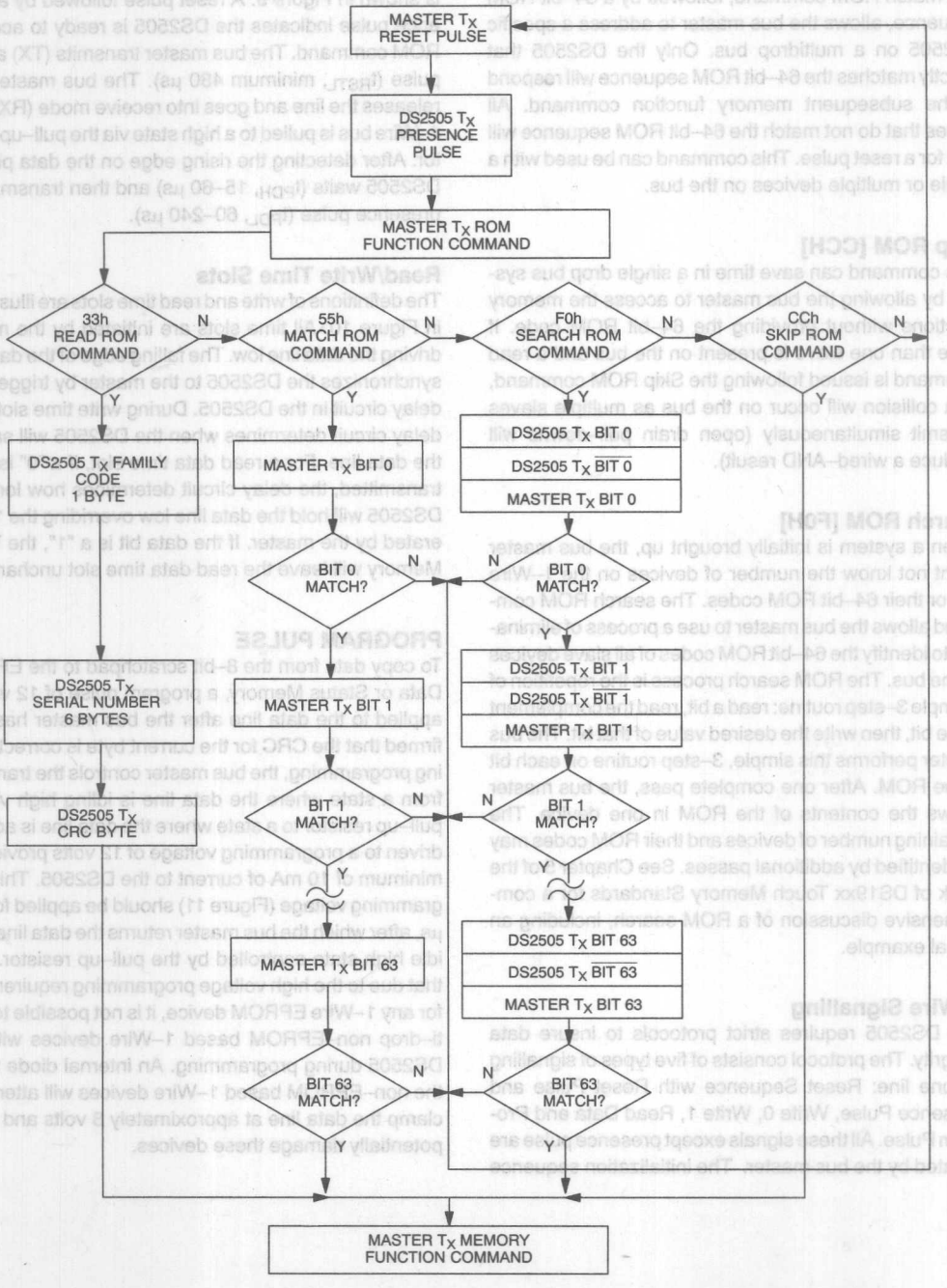
DS2505 EQUIVALENT CIRCUIT Figure 6



BUS MASTER CIRCUIT Figure 7



ROM FUNCTIONS FLOW CHART Figure 8



Match ROM [55H]

The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS2505 on a multidrop bus. Only the DS2505 that exactly matches the 64–bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull–downs will produce a wired–AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx Touch Memory Standards for a comprehensive discussion of a ROM search, including an actual example.

1–Wire Signalling

The DS2505 requires strict protocols to insure data integrity. The protocol consists of five types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and Program Pulse. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS2505 is shown in Figure 9. A reset pulse followed by a presence pulse indicates the DS2505 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1–Wire bus is pulled to a high state via the pull–up resistor. After detecting the rising edge on the data pin, the DS2505 waits (t_{PDH}, 15–60 µs) and then transmits the presence pulse (t_{PDL}, 60–240 µs).

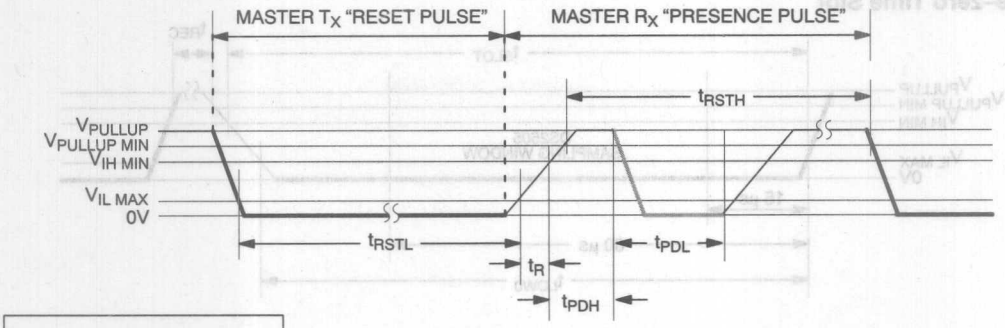
Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 10. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2505 to the master by triggering a delay circuit in the DS2505. During write time slots, the delay circuit determines when the DS2505 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2505 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8–bit scratchpad to the EPROM Data or Status Memory, a program pulse of 12 volts is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pull–up resistor to a state where the data line is actively driven to a programming voltage of 12 volts providing a minimum of 10 mA of current to the DS2505. This programming voltage (Figure 11) should be applied for 480 µs, after which the bus master returns the data line to an idle high state controlled by the pull–up resistor. Note that due to the high voltage programming requirements for any 1–Wire EPROM device, it is not possible to multi–drop non–EPROM based 1–Wire devices with the DS2505 during programming. An internal diode within the non–EPROM based 1–Wire devices will attempt to clamp the data line at approximately 8 volts and could potentially damage these devices.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9

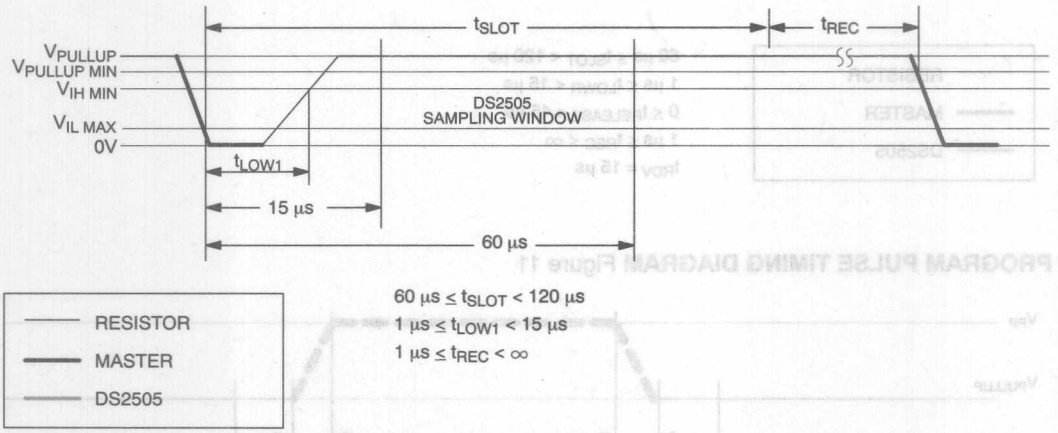


480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

READ/WRITE TIMING DIAGRAM Figure 10

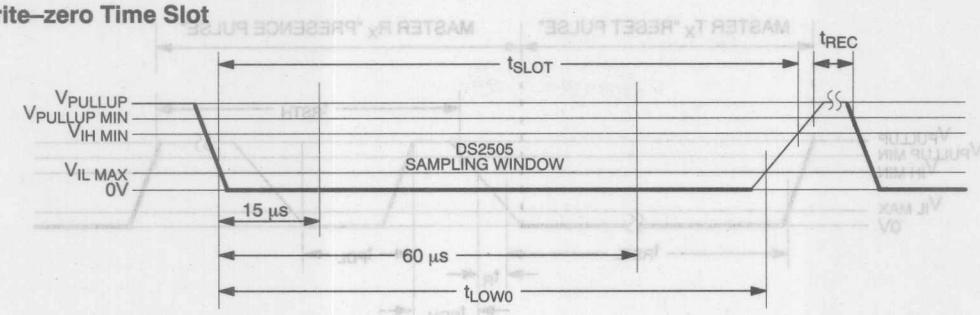
Write–one Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM (cont'd) Figure 10

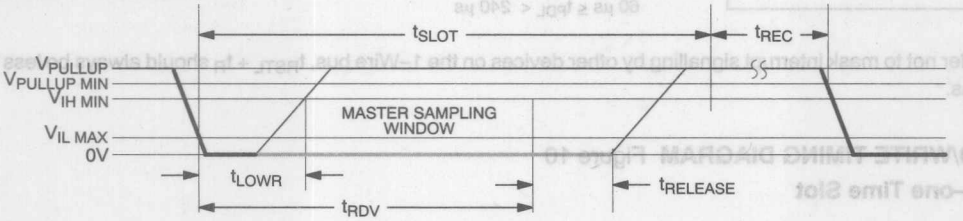
Write–zero Time Slot

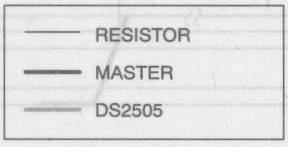


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

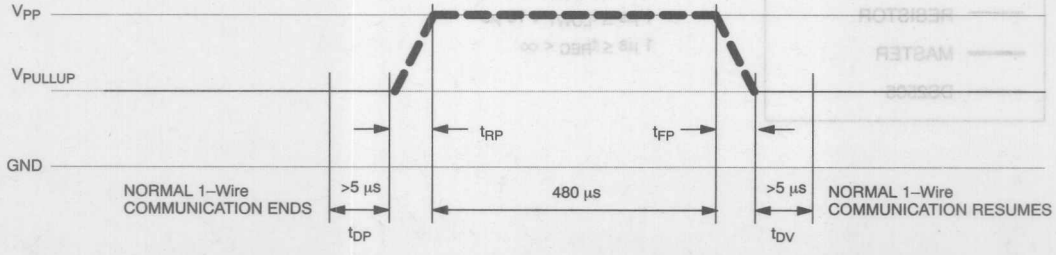
$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

PROGRAM PULSE TIMING DIAGRAM Figure 11



CRC GENERATION

With the DS2505 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is a 8–bit type and is stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS2505 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8–bit CRC is received in the true (non–inverted) form when reading the ROM of the DS2505. It is computed once at the factory and lasered into the ROM.

The other CRC is a 16–bit type, generated according to the standardized CRC16–polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used to safeguard user–defined EPROM data when reading data memory or status memory. It is the same type of CRC as is used with NVRAM based Touch Memories to safeguard data packets of the Touch Memory File Structure. In contrast to the 8–bit CRC, the 16–bit CRC is always returned in the complemented (inverted) form. A CRC–generator inside the DS2505 chip (Figure 12) will calculate a new 16–bit CRC at every situation shown in the command flow chart of Figure 5.

The DS2505 provides this CRC–value to the bus master to validate the transfer of command, address, and data to and from the bus master. When reading the data memory of the DS2505 with the Read Memory command, the 16–bit CRC is only transmitted as the end of the memory is reached. This CRC is generated by clearing the CRC generator, shifting in the command, low address, high address and every data byte starting at the first addressed memory location and continuing until the end of the implemented data memory is reached.

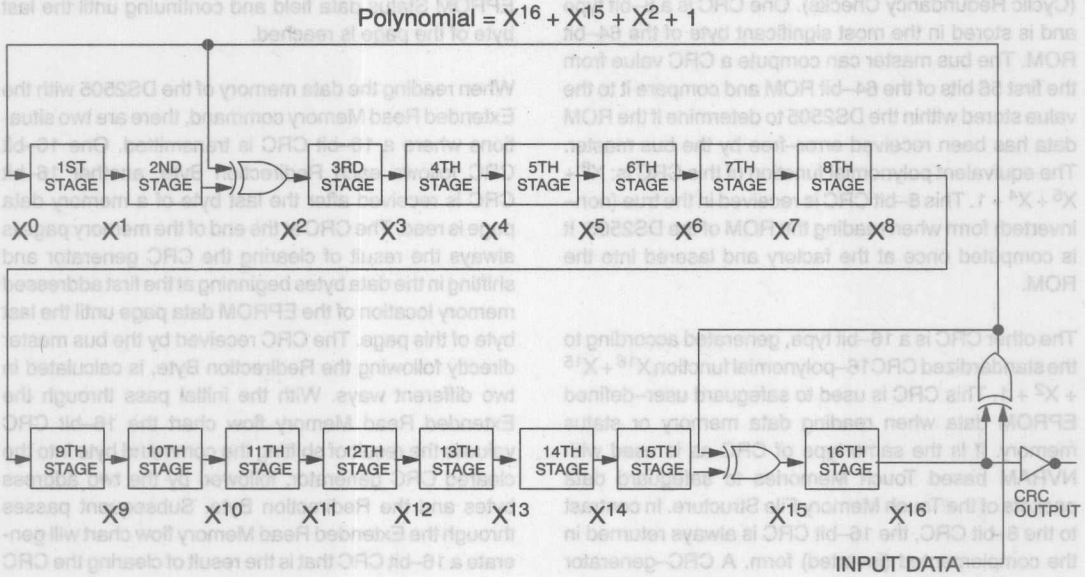
When reading the status memory with the Read Status command, the 16–bit CRC is transmitted when the end of each 8–byte page of the status memory is reached. At the initial pass through the Read Status flow chart the 16–bit CRC will be generated by clearing the CRC generator, shifting in the command byte, low address, high address and the data bytes beginning at the first addressed memory location and continuing until the last byte of the addressed EPROM Status data page is reached. Subsequent passes through the Read Status flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes starting at the first byte of the next page of the EPROM Status data field and continuing until the last byte of the page is reached.

When reading the data memory of the DS2505 with the Extended Read Memory command, there are two situations where a 16–bit CRC is transmitted. One 16–bit CRC follows each Redirection Byte, another 16–bit CRC is received after the last byte of a memory data page is read. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. The CRC received by the bus master directly following the Redirection Byte, is calculated in two different ways. With the initial pass through the Extended Read Memory flow chart the 16–bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16–bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only.

When writing to the DS2505 (either data memory or status memory), the bus master receives a 16–bit CRC to verify the correctness of the data transfer before applying the programming pulse. With the initial pass through the Write Memory/Status flow chart the 16–bit CRC will be generated by clearing the CRC–generator, shifting in the command, address low, address high and the data byte. Subsequent passes through the Write Memory/Status flow chart due to the DS2505 automatically incrementing its address counter will generate an 16–bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS2505 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2505 does not match the value generated by the bus master. For more details on generating CRC values including example implementations in both hardware and software, see the Book of DS19xx Touch Memory Standards.

CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 122



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +12.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1 , 6
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Voltage @ 10 mA	V_{PP}	11.0	11.5	12.0	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V; –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Delay to Program	t_{DP}	5			µs	10
Delay to Verify	t_{DV}	5			µs	10
Program Pulse Width	t_{PP}	480			µs	10
Program Voltage Rise Time	t_{RP}	5			µs	10
Program Voltage Fall Time	t_{FP}	5			µs	10

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–Wire bus.)
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. Maximum 1–Wire voltage for programming parameters is 11.5V ± 0.5V; temperature range is –20°C to +50°C.

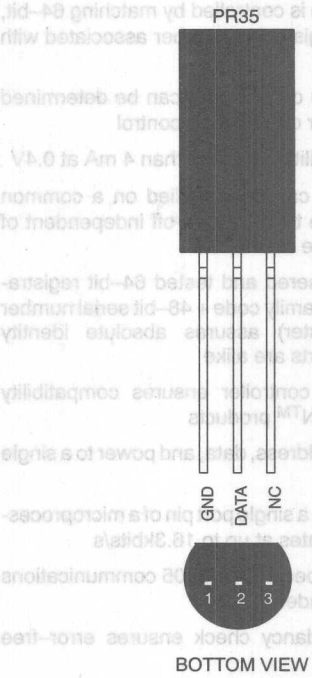
DALLAS SEMICONDUCTOR

DS2506
64Kbit Add–Only Memory

FEATURES

- 65536–bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Built–in multidrop controller ensures compatibility with other MicroLAN™ products
- EPROM partitioned into two hundred fifty–six 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- 8–bit family code specifies DS2506 communications requirements to reader
- Presence detector acknowledges when the reader first applies voltage
- Low cost PR35 package
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –20°C to +50°C

PIN ASSIGNMENT



BOTTOM VIEW

ORDERING INFORMATION

DS2506 PR35 package

SILICON LABEL™ DESCRIPTION

The DS2506 Add–Only Memory operates nearly identically to the DS2505. The main differences are: 64K bit of memory organized as 256 pages of 32 bytes and a family code of 0F hexadecimal. For further details please refer to the DS2505 data sheet.

051794 1/1

DALLAS SEMICONDUCTOR

DS2405
Addressable Switch

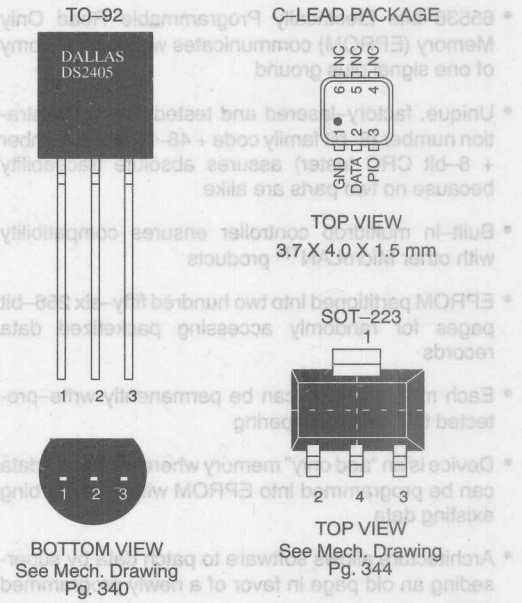
FEATURES

- Open drain PIO pin is controlled by matching 64–bit, laser–engraved registration number associated with each device
- Logic level of open drain output can be determined over 1–Wire bus for closed–loop control
- PIO pin sink capability is greater than 4 mA at 0.4V
- Multiple DS2405's can be identified on a common 1–Wire bus and be turned on or off independent of other devices on the bus
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute identity because no two parts are alike
- Built–in multidrop controller ensures compatibility with other MicroLAN™ products
- Reduces control, address, data, and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
- 8–bit family code specifies DS2405 communications requirements to reader
- 8–bit cyclic redundancy check ensures error–free selection
- Zero standby power required
- Low cost TO–92, SOT–223, or 6–pin C–Lead surface mount package
- 1–Wire communication operates over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C

ORDERING INFORMATION

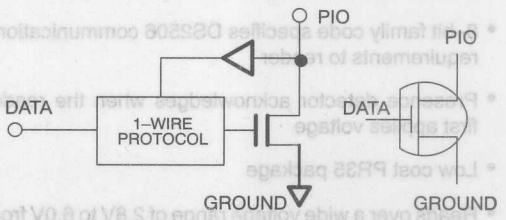
DS2405	TO–92 package
DS2405Z	4–pin SOT–223 package
DS2405P	6–pin C–lead package
DS2405T	Tape & Reel version of DS2405
DS2405Y	Tape & Reel version of DS2405Z
DS2405V	Tape & Reel version of DS2405P

PIN ASSIGNMENT



PIN DESCRIPTION

TO–92		C–LEAD	
Pin 1	– Ground	Pin 1	– Ground
Pin 2	– Data	Pin 2	– Data
Pin 3	– PIO	Pin 3	– PIO
Pin 4	– Ground	Pin 4–6	– No Connect



SILICON LABEL™ DESCRIPTION

The DS2405 Addressable Switch is an open drain N–channel transistor that can be turned on or off by matching the 64–bit factory–lasered registration number within each part. The 64–bit number consists of an 8–bit family code, a unique 48–bit serial number, and an 8–bit cyclic redundancy check. Communication with the DS2405 follows the standard Dallas Semiconductor 1–Wire protocol and can be accomplished with a single port pin of a microcontroller. Multiple DS2405 devices can reside on a common 1–Wire bus creating a MicroLan™ . The network controller circuitry is embedded within the chip including a search algorithm to determine the identity of each DS2405 on the network. The open drain output (PIO pin) for each DS2405 on the MicroLan can be independently toggled on or off whether there is one or many devices sharing the same 1–Wire bus. The logic level of the PIO pin for each device on the MicroLan can also be individually sensed and reported to the bus master.

OVERVIEW

The DS2405 Addressable Switch provides a means for assigning an electronically readable identification to a particular node or location with additional control capability provided by an open–drain N–channel MOSFET that can be remotely switched and sensed via communication over the 1–Wire bus. The DS2405 contains a factory–lasered registration number that includes a unique 48–bit serial number, an 8–bit CRC, and an 8–bit family code (05h). The 64–bit ROM portion of the DS2405 not only creates an absolutely unique electronic identification for the device itself but also is a means to locate and change or obtain the state of the switch that is associated with the 64–bit ROM. The structure of the 64–bit ROM is shown in Figure 1. The device derives its power entirely from the 1–Wire bus by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. The DS2405 uses the standard Dallas Semiconductor 1–Wire protocol for data transfers, with all data being read and written least significant bit first. Communication to and from the DS2405 requires a single bidirectional line that is typically the port pin of the microcontroller. The 1–Wire bus master (microcontroller) must first issue one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, and 5) Active–Only Search ROM. These commands operate on the 64–bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1–Wire line as well as indicate to the bus how many and what type of each device is present. The protocol required for these ROM function commands is described in Figure 4. After a ROM function command is successfully executed, the open–drain output can be toggled or its current status determined via the 1–Wire bus.

1–WIRE BUS SYSTEM

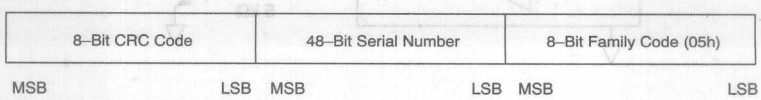
The 1–Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2405 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal type and timing). For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx Touch Memory Standards.

Hardware Configuration

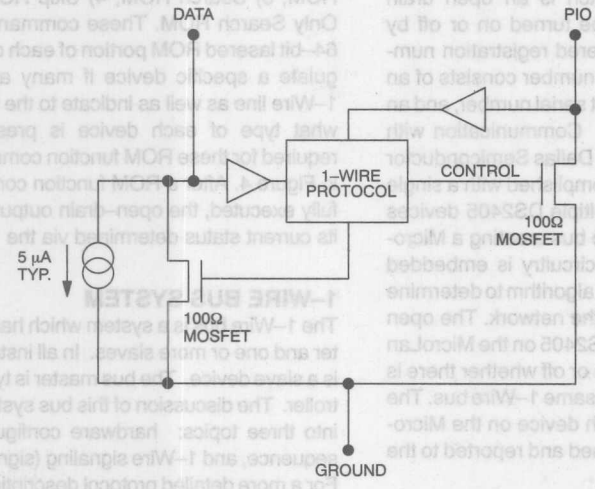
The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have an open drain connection or 3–state outputs. The DS2405 is an open drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pull–up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pull–up resistor should be approximately 5 kΩ for short line lengths. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus has a maximum data rate of 16.3k bits per second.

The idle state for the 1–Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 μs, one or more of the devices on the bus may be reset. In addition, the state of the PIO pin for one or more of the DS2405s on the bus may return to its default (off) condition.

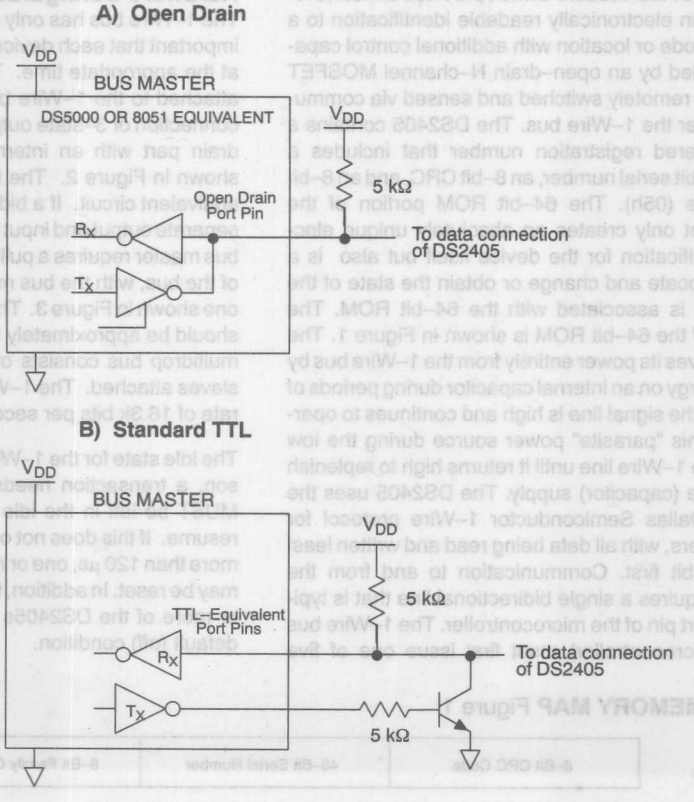
DS2405 MEMORY MAP Figure 1



DS2405 EQUIVALENT CIRCUIT Figure 2



BUS MASTER CIRCUIT Figure 3



TRANSACTION SEQUENCE

The sequence for accessing the DS2405 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that at least one DS2405 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of five ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 4):

Read ROM [33h]

This command allows the bus master to read the DS2405's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can be used only if there is a single DS2405 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The Match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific device on a multidrop bus. All devices that do not match the 64–bit ROM sequence will wait for a reset pulse. The DS2405 that exactly matches the 64–bit ROM sequence will toggle the state of its PIO pin after the 64th bit of the match is entered. If the open–drain N–channel device was off, it will be turned on and vice versa. After the last bit of the ROM sequence is received from the bus master and the PIO pin of the selected DS2405 has toggled, additional read time slots issued by the bus master will cause the DS2405 to output the logic state of its PIO pin onto the 1–Wire bus. If the pulldown is on and the PIO pin is a logical 0, the DS2405 will respond with read 0 time slots. If the pulldown is off and the PIO pin is a logical 1 (external pullup is required), the DS2405 will respond with read 1 time slots. Each additional read time slot issued by the bus master will continue to indicate the state of the PIO pin until a reset pulse is received from the bus master.

Search ROM [F0h]

When a system is initially interrogated, the bus master may not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus. This process of elimination involves repeated application of a simple three–step procedure where the bus master starts by reading a bit position in the 64–bit ROM, followed by reading the complement of that bit position, and finally writing to all the devices still involved in the search the desired logic value for that bit position. An example is shown below and a flowchart for the search algorithm can be found in the "Book of DS19xx Touch Memory Standards."

Four devices are connected to the 1–Wire bus. Their binary ROM contents are:

device 1: xxxxxx10101100
device 2: xxxxxx01010101
device 3: xxxxxx10101111
device 4: xxxxxx10001000

The x's represent the higher remaining bits. Shown are the lowest eight bits of the ROM contents. The least significant bit is to the right in this representation. The search process runs as follows:

1. The master begins the initialization sequence by issuing a Reset Pulse. The Touch Memories respond by issuing Presence pulses.
2. The master will then issue the Search ROM command on the 1–Wire Bus.
3. The master reads one bit from the 1–Wire bus. Each device will respond by placing the value of the first bit of its respective ROM data onto the 1–Wire bus. Devices 1 and 4 will place a 0 onto the 1–Wire bus; that is, they pull it low. Devices 2 and 3 will send a 1 by allowing the line to stay high. The result is the logical AND of all devices on the line; therefore the master reads a 0. The master will issue another read time slot. Since the ROM Search command is being executed, all devices respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1–Wire Bus. Devices 1 and 4 will send a 1; devices 2 and 3 will send a 0. Thus

the 1–Wire bus will be pulled low. The master again reads a 0 for the complement of the first ROM data bit. This tells the master that there are devices on the bus that have a 0 in the first position and others that have a 1. If all devices had a 0 in this bit position, the reading would be 01; if the bit position contained a 1, the result would be 10. (Note that the 11 condition indicates that no devices are present on the 1–Wire bus.)

4. The master now decides to write a 0 on the 1–Wire bus. This deselects Devices 2 and 3 for the remainder of the search pass, leaving only devices 1 and 4 participating in the search process.
5. The master performs two more reads and receives a 0 followed by a 1 bit. This indicates that all active devices have a 0 in this bit position of their ROM.
6. The master then writes a 0 to keep devices 1 and 4 selected.
7. The master executes two reads and receives two 0 bits. This again indicates that both 1 and 0 exist as the third bit of the ROM of the active devices.
8. The master again writes a 0. This deselects device 1, leaving device 4 as the only active device.
9. Subsequent reads to the end of the ROM will not show bit conflicts. Therefore, they directly tell the master the ROM contents of the active device. After having learned any new ROM bit, the master has to resend this bit to keep the device selected. As soon as all ROM bits of the device are known and the last bit is resent by the master, the device is ready to output the state of the PIO pin using additional read time slots.
10. The master must learn the other devices' ROM data. Therefore, it starts another ROM Search sequence by repeating steps 1 through 7.
11. At the highest bit position, where the master wrote a 0 at the first pass (step 8), it now writes a 1. This deselects device 4, leaving device 1 active.
12. As in step 9, subsequent reads to the end of the ROM will not show bit conflicts. This completes the second ROM Search pass where the master has learned another ROM's contents.
13. The master must learn the other devices' ROM data. Therefore, it starts another ROM Search sequence by repeating steps 1 to 3.
14. At the second highest bit position where the master wrote a 0 at the first pass (step 4), it now writes a 1. This deselects devices 1 and 4, leaving devices 2 and 3 active.
15. The master sends two read time slots and receives two 0 bits, indicating a bit conflict.
16. The master again decides to write a 0. This deselects device 3, leaving device 2 as the only active device.
17. As in step 9, subsequent reads to the end of the ROM will not show bit conflicts. This completes the third ROM Search pass where the master has learned another ROM's contents.
18. The master must learn the other devices' ROM data. Therefore it starts another ROM Search sequence by repeating steps 13 to 15.
19. At the highest bit position where the master wrote a 0 at the previous pass (step 16), it now writes a 1. This deselects device 2, leaving device 3 active.
20. As in step 17, subsequent reads to the end of the ROM will not show bit conflicts. This completes the fourth ROM Search pass where the master has learned another ROM's contents.

After one complete pass, the bus master knows the contents of the 64–bit ROM in one device. Subsequent passes will reveal the total number of devices and their individual ROM codes. In addition, after each complete pass of the search that successfully determines the 64–bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM has been issued since all other devices will have dropped out of the search process and are waiting for a reset pulse. The DS2405 that was discovered by the search process will not toggle the state of its PIO pin at the end of the search, but additional read time slots issued by the bus master after the search is completed will cause the DS2405 to output the logic state of its PIO pin onto the 1–Wire bus. If the pulldown is on and the PIO pin is a logical 0, the DS2405 will respond with read 0 time slots. If the pulldown is off and the PIO pin is a logical 1 (external pullup is required), the DS2405 will respond with read 1 time slots. Each additional read time slot issued by the bus master will continue to indicate the state of the PIO pin until a reset pulse is received from the bus master. The combination of Match ROM and Search ROM allows the user to change the state of the PIO pin and report the current state (Match ROM) or simply report the current state of the PIO pin without changing it (Search ROM).

Active–Only Search ROM [ECh]

The Active–Only Search ROM command operates similarly to the Search ROM command except that only devices with their output pulldown turned on are allowed to participate in the search. This provides an efficient means for the bus master to determine devices on a multidrop system that are active (PIO pin driven low). After each pass of the active–only search that successfully determines the 64–bit ROM for a specific device on the multidrop bus with its output pulldown turned on, that particular device can be individually accessed as if a Match ROM had been issued since all other devices will have dropped out of the active–only search process and are waiting for a reset pulse. The DS2405 that was discovered by the active–only search process will not toggle the state of its PIO pin at the end of the search, but additional read time slots issued by the bus master after the search is completed will cause the DS2405 to output the logic state of its internal CONTROL signal (see Figure 2) onto the 1–wire bus. Since the Active–Only Search ROM command only operates on devices with their pulldown on, the internal CONTROL signal for each of these parts is always a logical 1. With CONTROL=1, the selected DS2405 will respond to the bus master with read 0 time slots after an active–only search pass is successfully completed. Each additional read time slot issued by the bus master will continue to appear as a read 0 until a reset pulse is received from the bus master. If the CONTROL signal is a logical 0 for any DS2405, that device will not participate in the Active–Only Search. The combination of Search ROM and Active–Only Search ROM allows the user to search in the most efficient manner depending on the requirements. If the bus master interrogates a multidrop system comprised of DS2405s whose PIO conditions are unknown, the Active–Only Search can quickly determine which devices are turned on. The two commands also allow the bus master to separately determine the state of the PIO pin and the internal CONTROL signal which may be useful in detecting certain conditions. If Search ROM returns read 0 time slots (PIO=logical 0) for a given device, it may be due to that particular DS2405 driving its PIO pin low, or under certain conditions the logical 0 may be caused by some other device holding PIO low. If that same device is found using an active–only search, CONTROL must be a logical 1 and the PIO pin is being held low by the DS2405. If that same device is not found using an active–only search, CONTROL must be a logical 0 and the PIO pin is being held low by some other device or perhaps a fault condition such as a PIO shorted to ground. A second fault condition may be detected if Search ROM for a given device returns read 1 time slots (PIO=logical 1) but Active–Only Search ROM is successful (CONTROL=logical 1) and returns read 0 time slots for the same device, indicating the possibility that PIO may be shorted to a positive voltage.

Skip ROM [CCh]

The complete 1–Wire protocol for all Dallas Semiconductor Touch Memories contains a Skip ROM command. Since the DS2405 contains only the 64–bit ROM with no additional data fields, the Skip ROM is not applicable and will cause no further activity on the 1–Wire bus if executed. The DS2405 does not interfere with other 1–Wire parts on a multidrop bus that do respond to a Skip ROM (for example, a DS2405 and DS1994 on the same bus).

1–WIRE SIGNALLING

The DS2405 requires strict protocols to insure data integrity. The protocol consists of four types of signalling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1 and read data. All these signals except presence pulse are initiated by the bus master.

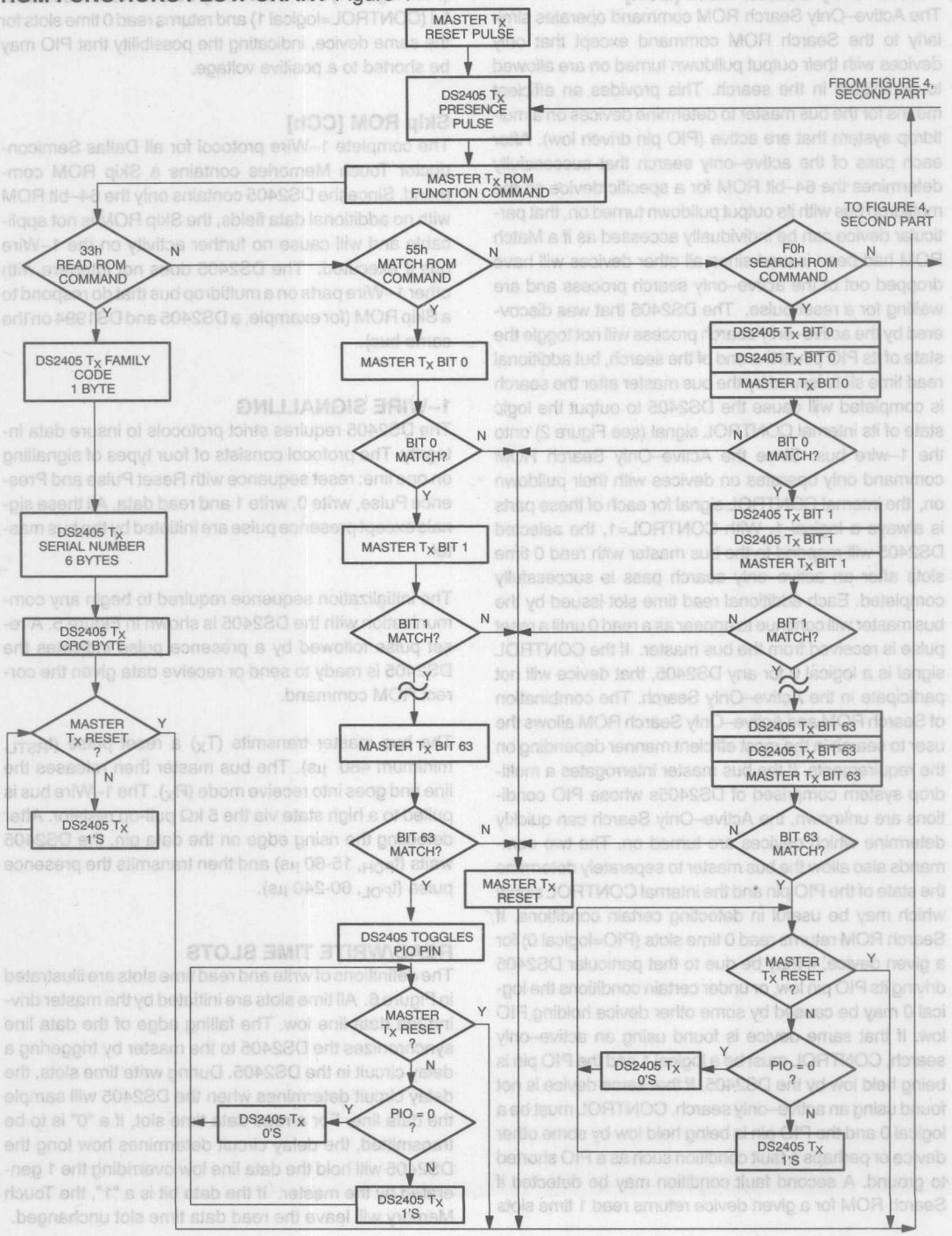
The initialization sequence required to begin any communication with the DS2405 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS2405 is ready to send or receive data given the correct ROM command.

The bus master transmits (T_X) a reset pulse (t_{RSTL}, minimum 480 μs). The bus master then releases the line and goes into receive mode (R_X). The 1–Wire bus is pulled to a high state via the 5 kΩ pull-up resistor. After detecting the rising edge on the data pin, the DS2405 waits (t_{PDH}, 15-60 μs) and then transmits the presence pulse (t_{PDL}, 60-240 μs).

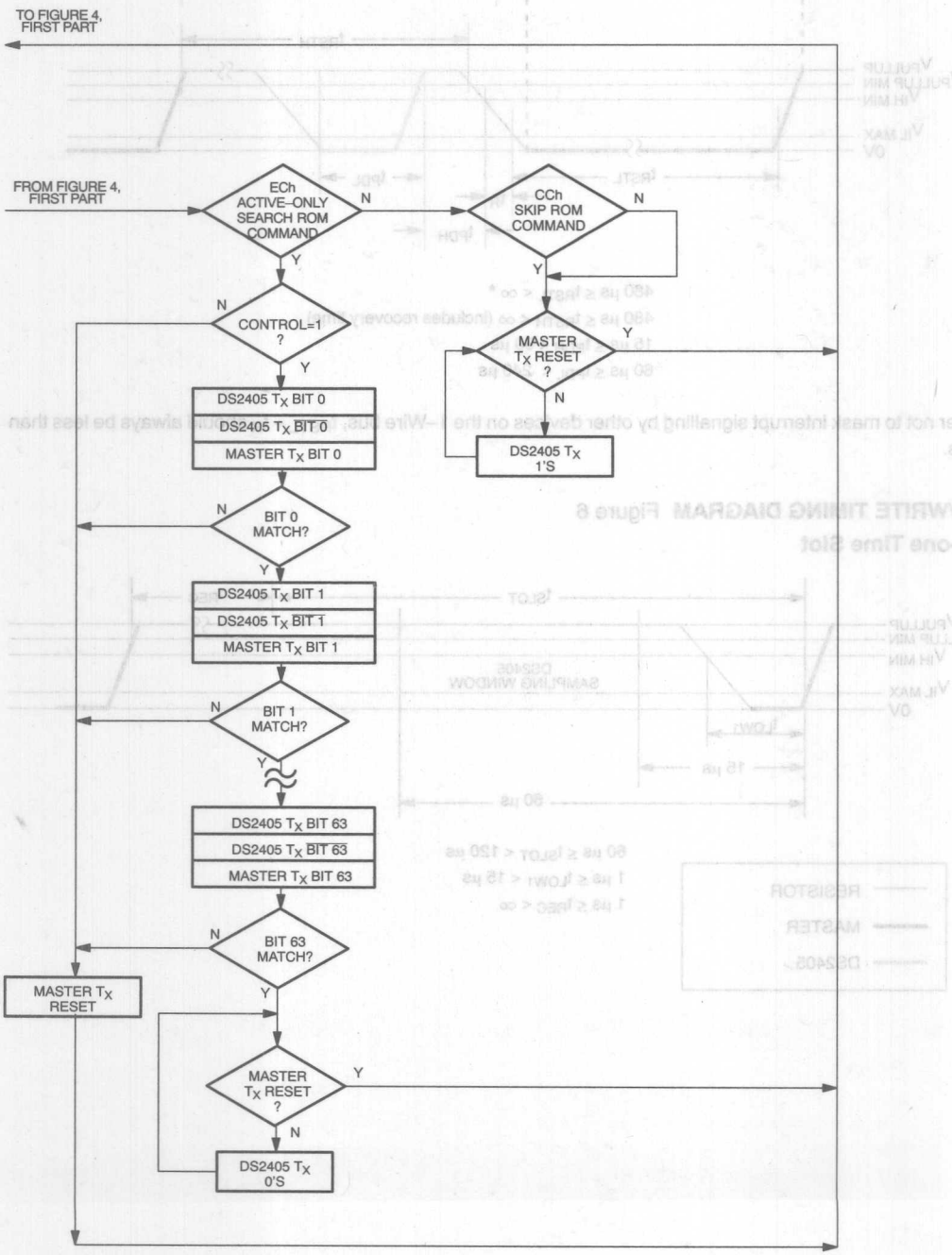
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2405 to the master by triggering a delay circuit in the DS2405. During write time slots, the delay circuit determines when the DS2405 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2405 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the Touch Memory will leave the read data time slot unchanged.

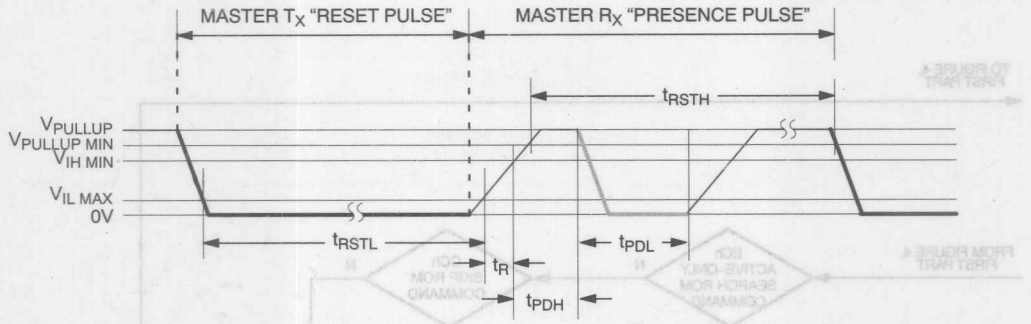
ROM FUNCTIONS FLOW CHART Figure 4



ROM FUNCTIONS FLOW CHART (cont'd) Figure 4



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5

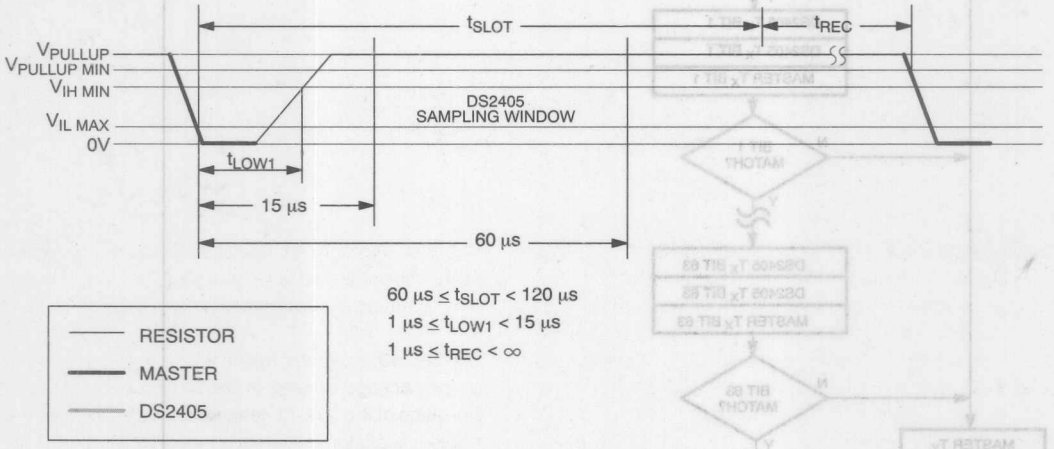


480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

READ/WRITE TIMING DIAGRAM Figure 6

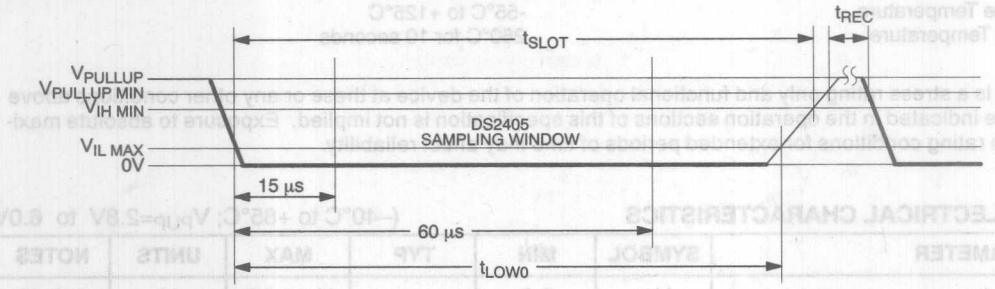
Write–one Time Slot



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM (cont'd) Figure 6

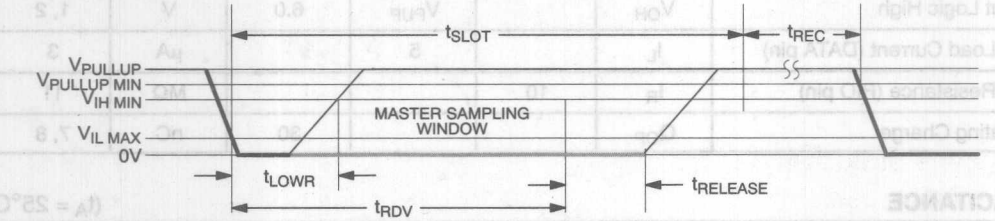
Write–zero Time Slot

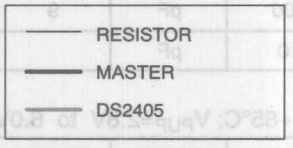


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Read–data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

$t_{RDV} = 15\ \mu s$

CRC GENERATION

To validate the data transmitted from the DS2405, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS2405. If the two CRC values match, the transmission is error–free.

The equivalent polynomial function of this CRC is:

$$CRC = x^8 + x^5 + x^4 + 1$$

For more details, see the Book of DS19xx Touch Memory Standards.

LOT QUANTITIES AND CUSTOM DS2405

The DS2405 is available in registered whole lots sealed in tamper–detecting cartons with the beginning number and range which that particular lot spans specified on the label. Nominal lot size is 4,200 pieces with devices packed in either 500–piece bags or mounted on reels for use by automatic assembly equipment.

The DS2405 can be made available with a custom brand on the package which provides a human–readable representation of the factory–lasered 64–bit ROM code inside. Additional customization of a portion of the unique 48–bit serial number by the customer is available. Dallas Semiconductor will register and assign a specific customer ID in the 12 most significant bits of the 48–bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non–selectable and will be automatically incremented by one. Certain quantities and conditions apply for these special order parts. Contact your Dallas Semiconductor sales representative for more information.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Solder Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current (DATA pin)	I_L		5		µA	3
Input Resistance (PIO pin)	I_R	10			MΩ	11
Operating Charge	Q_{OP}			30	nC	7, 8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance DATA pin	C_D			800	pF	9
Capacitance PIO pin	C_P			10	pF	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum (15 µs total from falling edge on 1–Wire bus).
6. V_{IH} is a function of the external pull–up resistor and the V_{CC} supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.
9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.
10. V_{IH} for PIO pin should always be greater than or equal to V_{PUP}–0.3 volts.
11. Input resistance is to ground.

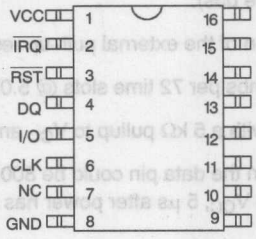
DALLAS SEMICONDUCTOR

DS2404S–C01
Dual Port Memory Plus Time

FEATURES

- Bridge for electronic equipment to the 1–Wire MicroLAN
- 4096 bits of nonvolatile dual–port memory including real time clock/calendar in binary format, programmable interval timer, and programmable power–on cycle counter
- 1–Wire interface for MicroLAN communication at 16.3k bits per second
- 3–Wire host interface for high–speed data communications at 2M bits per second
- Unique, factory–lasered and tested 64–bit registration number (8–bit family code + 48–bit serial number + 8–bit CRC tester) assures absolute traceability because no two parts are alike
- Memory partitioned into 16 pages of 256–bits for packetizing data
- 256–bit scratchpad with strict read/write protocols ensures integrity of data transfer
- Programmable alarms can be set to generate interrupts for interval timer, real time clock, and/or cycle counter
- Space saving 16–pin SOIC package
- Operating temperature range from –40°C to +85°C
- Operating voltage range from 2.8 to 5.5 Volts

PIN ASSIGNMENT



16–PIN SOIC (300 Mil)
See Mech. Drawing Pg. 338

PIN DESCRIPTION

Pin #	Pin Name	Description
Pin 1&16	- V_{CC}	2.8 to 5.5 Volts
Pin 2	- $\overline{IRQ}$	Interrupt Output
Pin 3	- $\overline{RST}$	3-Wire Reset Input
Pin 4	- DQ	3-Wire Input/Output
Pin 5	- I/O	1-wire Input/Output
Pin 6	- CLK	3-Wire Clock Input
Pin 7 & 12	- NC	No Connection
Pin 8 & 13	- GND	Ground
Pin 9	- V_{BATB}	Battery Backup Input
Pin 10	- V_{BATO}	Battery Operate Input
Pin 11	- 1 Hz	1 Hz Output
Pin 14 & 15	- X_1,X_2	Crystal Connections

DESCRIPTION

In order to provide universal access to the MicroLAN, the DS2404S–C01 Dual Port Memory Plus Time has been developed. This device has both 1–Wire and a 3–Wire serial microcontroller interface. The DS2404S–C01 can be used to make complex functions involving microcontrollers behave as if they were Touch Memories.

Being a custom–ROM version of the DS2404, the DS2404S–C01 has the family code 84H. In addition to this, the 12 most significant bit of the serialization field are coded 001H, leaving 28 bits for serialization. The communication with the DS2404S–C01 through the 1–Wire port is identical to the DS1994; all functions of the DS1994 are available.

The second port of the DS2404S–C01 is a 3–wire serial interface providing the signals Data, Clock, and Reset for communication speeds up to 2 Mbit/s. The 3–wire interface directly accesses the scratchpad, memory locations and special registers without requiring a ROM command to address the device. For the 3–wire interface the same command codes and transaction flowcharts apply as for the 1–Wire interface; the lasered ROM itself and the commands of the network layer are not accessible. The arbitration between ports is done according to the method first come, first serve. Housed in a 16–pin SOIC package, the DS2404S–C01 provides a separate open drain IRQ pin for interrupt signalling and a 1 Hz clock output. Depending on the application the device can either operate on V_{CC} from 2.8V to 5.5V with battery backup or on battery only. For further details please refer to the DS2404 or DS1994 data sheet.

FULL DATA SHEET AVAILABLE – CALL 214–450–8167 PRELIMINARY

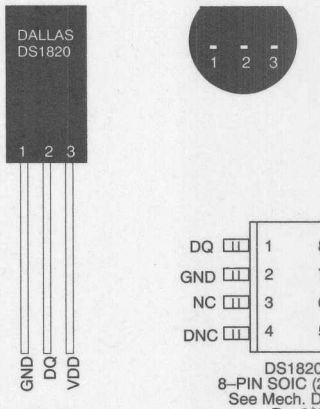
DALLAS SEMICONDUCTOR

DS1820
One–Wire Digital Thermometer

FEATURES

- Unique 1–Wire interface requires only one port pin for communication
- Multidrop capability simplifies distributed temperature sensing applications
- Requires no external components
- Can be powered from data line
- Zero standby power required
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit digital value.
- Converts temperature to digital word in 1 second (typ.)
- User–definable, nonvolatile temperature alarm settings
- Alarm search command identifies and addresses devices whose temperature is outside of programmed limits (temperature alarm condition)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

PIN ASSIGNMENT



DS1820
PR–35 PACKAGE

DS1820S
8–PIN SOIC (200 MIL)
See Mech. Drawing
Pg. 337

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Optional V_{DD}
NC	–	No Connect
DNC	–	Do Not Connect

DESCRIPTION

The DS1820 Digital Thermometer provides 9–bit temperature readings which indicate the temperature of the device.

Information is sent to/from the DS1820 over a 1–Wire interface, so that only one wire (and ground) needs to be connected from a central microprocessor to a DS1820. Power for reading, writing, and performing temperature conversions can be derived from the data line itself with no need for an external power source.

Because each DS1820 contains a unique silicon serial number, multiple DS1820s can exist on the same 1–Wire bus. This allows for placing temperature sensors in many different places. Applications where this feature is useful include HVAC environmental controls, sensing temperatures inside buildings, equipment or machinery, and in process monitoring and control.

DALLAS SEMICONDUCTOR

DS2223/DS2224
EconoRAM

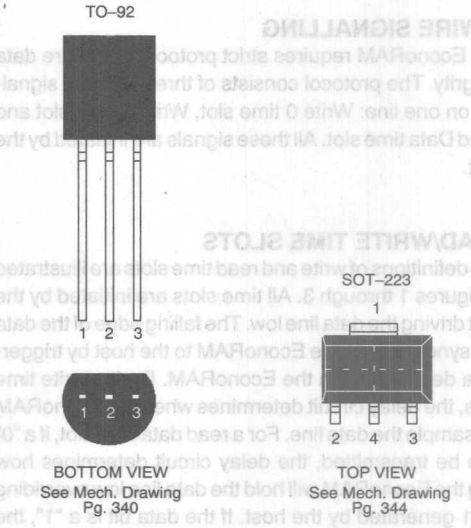
FEATURES

- Low–cost, general–purpose, 256–bit memory
  - DS2223 has 256–bit SRAM
  - DS2224 has 32–bit ROM, 224–bit SRAM
- Reduces control, address and data interface to a single pin
- Each DS2224 32–bit ROM is factory–lasered with a unique serial number
- DS2224 portion of ROM with custom code and unique serial number available
- Minimal operating power: 45 nanocoulombs per transaction @1.5V typical
- Less than 15 nA standby current at 25°C
- Nonvolatile data retention easily achieved via low–cost alkaline batteries or capacitors
- Directly connects to a port pin of popular microcontrollers
- Operation from 1.2 to 5.5 volts
- Popular TO–92 or SOT–223 surface mount package
- Operates over industrial temperature range –40°C to +85°C

DESCRIPTION

The DS2223 and DS2224 EconoRAMs are fully static, micro–powered, read/write memories in low–cost TO–92 or SOT–223 packages. The DS2223 is organized as a serial 256 x 1 bit static read/write memory. The DS2224's first 32 bits are lasered with a unique ID code at the time of manufacture; the remaining 224 bits are static read/write memory. Signaling necessary for reading or writing is reduced to just one interface lead.

PACKAGE OUTLINE



PIN CONNECTIONS

Pin 1	GND	– Ground
Pin 2	DQ	– Data In/Out
Pin 3	V_{CC}	– Supply
Pin 4	GND	– Ground

ORDERING INFORMATION

DS2223	256–bit SRAM – TO–92 Package
DS2223Z	256–bit SRAM – SOT–223 Package
DS2223T	1000 piece tape–and–reel of DS2223
DS2223Y	2500 piece tape–and–reel of DS2223Z
DS2224	32–bit serial number (ROM), 224–bit SRAM – TO–92 Package
DS2224Z	32–bit serial number (ROM), 224–bit SRAM – SOT–223 Package
DS2224T	1000 piece tape–and–reel of DS2224
DS2224Y	2500 piece tape–and–reel of DS2224Z

OPERATION

All communications to and from the EconoRAM are accomplished via a single interface lead. EconoRAM data is read and written through the use of time slots. All data is preceded by a command byte to specify the type of transaction. **Once a specific transaction has been initiated, either a read or a write, it must be completed for all memory locations before another transaction can be started.**

1–WIRE SIGNALLING

The EconoRAM requires strict protocols to insure data integrity. The protocol consists of three types of signalling on one line: Write 0 time slot, Write 1 time slot and Read Data time slot. All these signals are initiated by the host.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figures 1 through 3. All time slots are initiated by the host driving the data line low. The falling edge of the data line synchronizes the EconoRAM to the host by triggering a delay circuit in the EconoRAM. During write time slots, the delay circuit determines when the EconoRAM will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the EconoRAM will hold the data line low overriding the 1 generated by the host. If the data bit is a "1", the EconoRAM will leave the read data time slot unchanged.

COMMAND BYTE

The command byte to specify the type of transaction is transmitted LSB first from the host to the EconoRAM using write time slots. The first bit of the command byte (see Figure 4) is a logic 1. This indicates to the EconoRAM that a command byte is being written. The next two bits are the select bits which denote the physical address of the EconoRAM that is to be accessed (set to 00 currently). The remaining five bits determine whether a read or a write operation is to follow. If a write operation is to be performed, all five bits are set to a logic 1 level. If a read operation is to be performed, any or all of these bits are set to a logic 0 level. All eight bits of the command byte are transmitted to the EconoRAM with a separate time slot for each bit.

READ OR WRITE TRANSACTION

Read or write transactions are performed by initializing the EconoRAM to a known state, issuing a command byte, and then generating the time slots to either read EconoRAM contents or write new data. Each transaction consists of 264 time slots. Eight time slots transmit the command byte, the remaining 256 time slots transfer the data bits. (See Figure 5.) Once a transaction is started, it must be completed before a new transaction can begin.

To initially set the EconoRAM into a known state, 264 Write Zero time slots must be sent by the host. These Write Zero time slots will not corrupt the data in the EconoRAM since a command byte has not been written. This operation will increment the address pointer internal to the EconoRAM to its maximum count value. Upon reaching this maximum value, the EconoRAM will ignore all additional Write Zero time slots issued to it and the internal address pointer will remain locked at the top count value. This condition is removed by the reception of a Write One time slot, typically the first bit of a command byte.

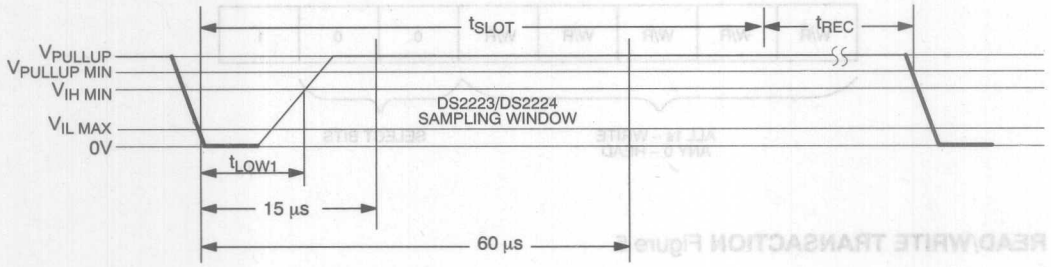
Once the EconoRAM has been set into a known state, the command byte is transmitted to the EconoRAM with eight write time slots. This resets the address pointer internal to the EconoRAM and prepares it for the appropriate operation, either a read or a write.

After the command byte has been received by the EconoRAM, the host controls the transfer of data. In the case of a read transaction, the host issues 256 read time slots. In the case of a write transaction, the host issues 256 write time slots according to the data to be written. All data is read and written least significant bit first.

Although the DS2224 has the first 32 bits replaced by lasered ROM rather than SRAM, it requires 256 write time slots for a complete write transaction. The data being sent during the first 32 write time slots has no effect on the DS2224 other than advancing the internal address pointer. As stated previously, it is not possible to change from read to write or vice versa before a transaction is completed.

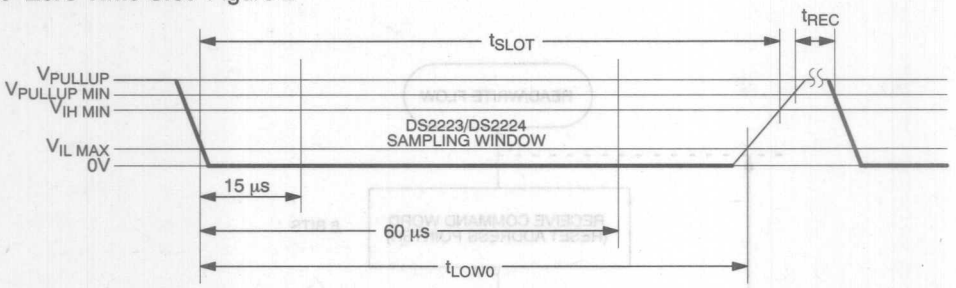
READ/WRITE TIMING DIAGRAM

Write–One Time Slot Figure 1



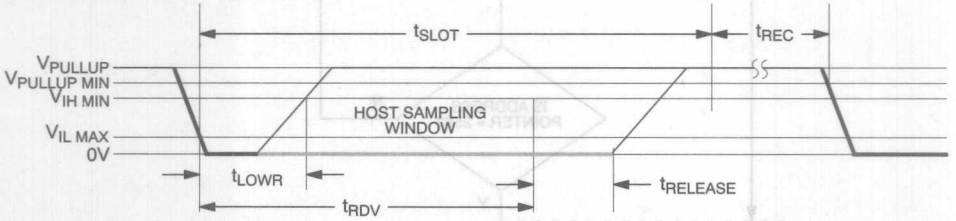
$60\ \mu s \le t_{SLOT} < \infty$
$1\ \mu s \le t_{LOW1} < 15\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

Write–Zero Time Slot Figure 2



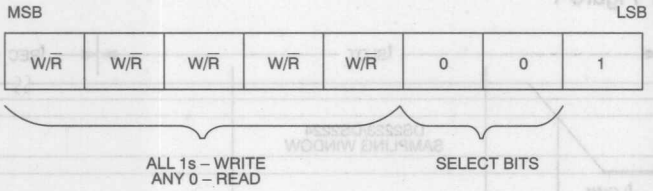
$60\ \mu s \le t_{LOW0} < t_{SLOT} < \infty$
$1\ \mu s \le t_{REC} < \infty$

Read–Data Time Slot Figure 3

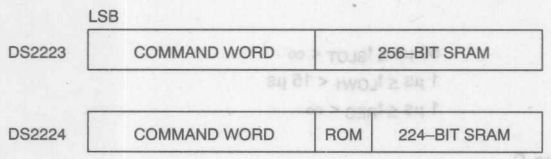


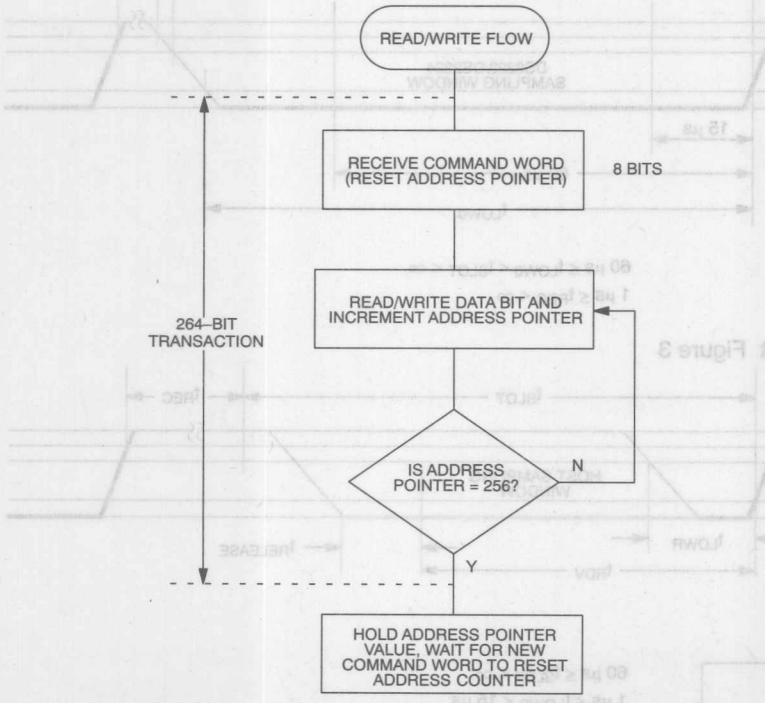
$60\ \mu s \le t_{SLOT} < \infty$
$1\ \mu s \le t_{LOWR} < 15\ \mu s$
$0 \le t_{RELEASE} < 45\ \mu s$
$1\ \mu s \le t_{REC} < \infty$
$t_{RDV} = 15\ \mu s$

COMMAND WORD Figure 4

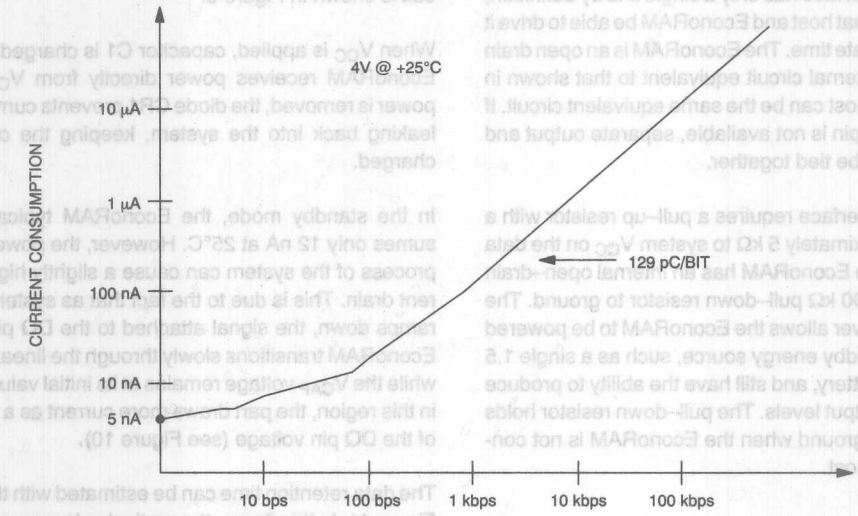


READ/WRITE TRANSACTION Figure 5

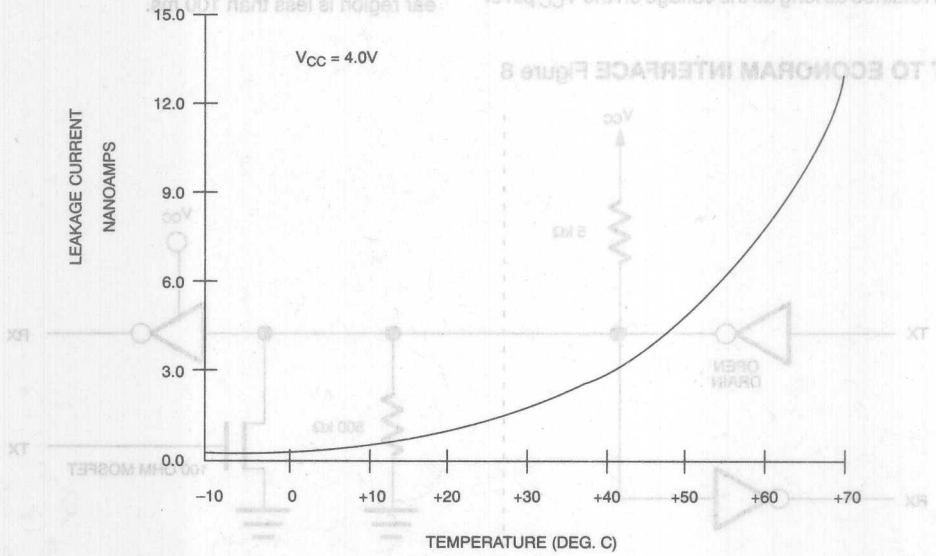




TYPICAL CURRENT CONSUMPTION VS. BIT RATE Figure 6



TYPICAL LEAKAGE CURRENT VS. TEMPERATURE Figure 7



1–WIRE INTERFACE

The 1–Wire interface has only a single line by definition; it is important that host and EconoRAM be able to drive it at the appropriate time. The EconoRAM is an open drain part with an internal circuit equivalent to that shown in Figure 8. The host can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The 1–Wire interface requires a pull–up resistor with a value of approximately 5 kΩ to system V_{CC} on the data signal line. The EconoRAM has an internal open–drain driver with a 500 kΩ pull–down resistor to ground. The open–drain driver allows the EconoRAM to be powered by a small standby energy source, such as a single 1.5 volt alkaline battery, and still have the ability to produce CMOS/TTL output levels. The pull–down resistor holds the DQ pin at ground when the EconoRAM is not connected to the host.

APPLICATION EXAMPLES

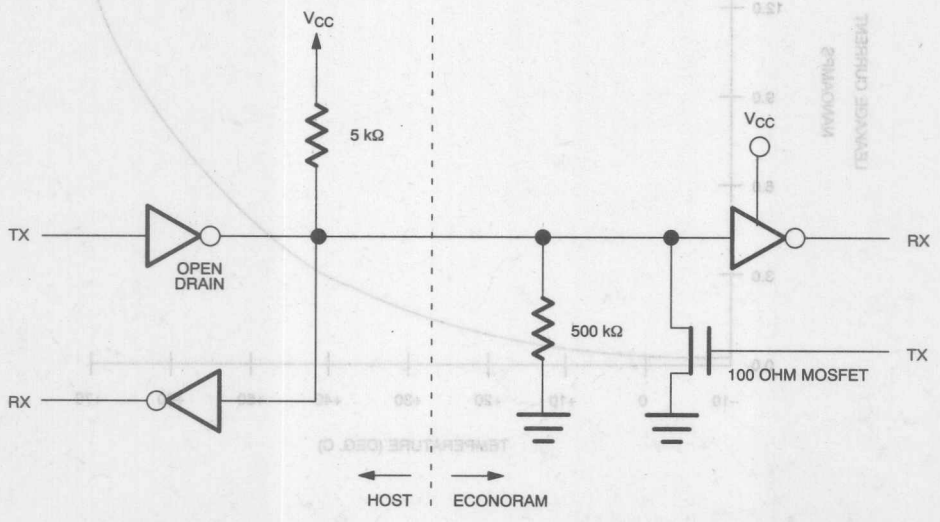
EconoRAMs are extremely conservative with power. Data can be retained in these small memories for as long as a month using the energy stored in a capacitor. Data is retained as long as the voltage on the V_{CC} pin of the EconoRAM (V_{CAP}) is at least 1.2 volts. A typical circuit is shown in Figure 9.

When V_{CC} is applied, capacitor C1 is charged and the EconoRAM receives power directly from V_{CC}. After power is removed, the diode CR1 prevents current from leaking back into the system, keeping the capacitor charged.

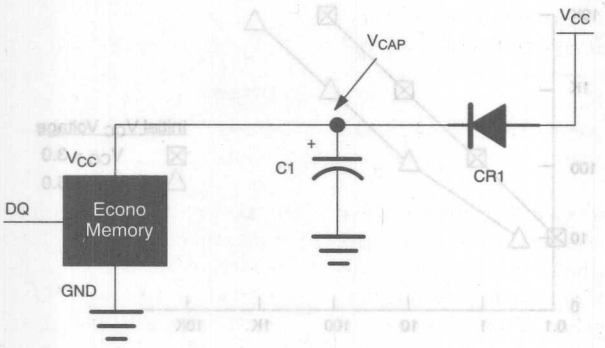
In the standby mode, the EconoRAM typically consumes only 12 nA at 25°C. However, the power–down process of the system can cause a slightly higher current drain. This is due to the fact that as system power ramps down, the signal attached to the DQ pin of the EconoRAM transitions slowly through the linear region, while the V_{CAP} voltage remains at its initial value. While in this region, the part draws more current as a function of the DQ pin voltage (see Figure 10).

The data retention time can be estimated with the aid of Figure 11. In this figure, the vertical axis represents the value of the capacitor C1; the horizontal axis is the data retention time in hours. The two curves represent initial V_{CAP} voltages of 3 and 5 volts. These curves are based on the assumption that the time the DQ pin is in the linear region is less than 100 ms.

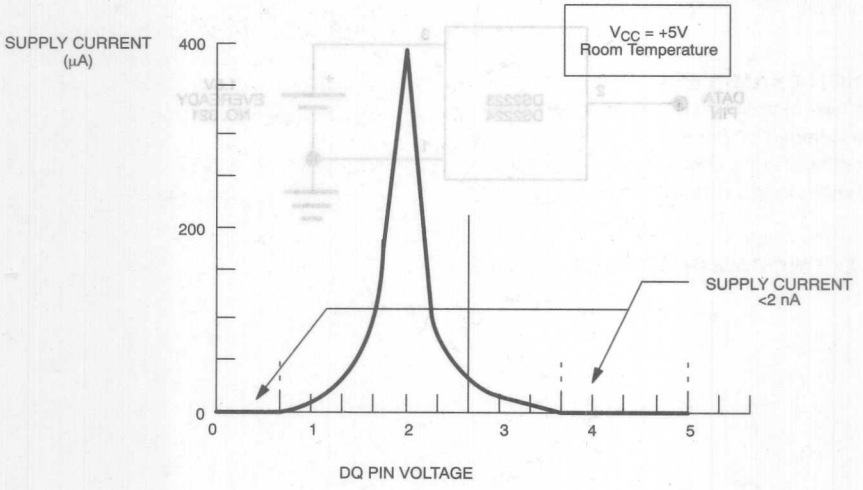
HOST TO ECONORAM INTERFACE Figure 8



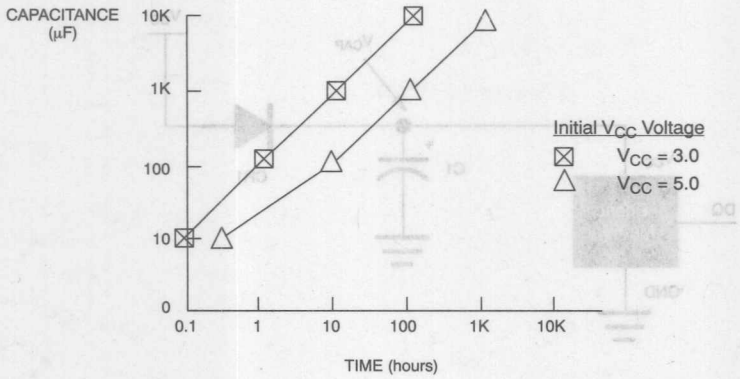
SUGGESTED CIRCUIT Figure 9



ICC VS. DQ VOLTAGE Figure 10

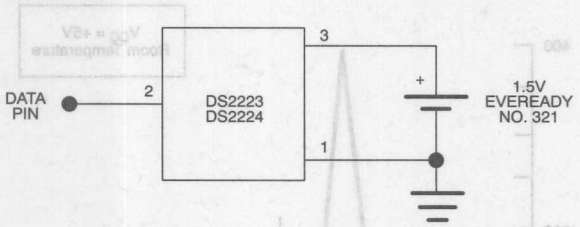


DATA RETENTION TIME VS. CAPACITANCE Figure 11



Using Battery Backup

14 mA–Hr => 144 million transactions



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +6.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Pin	DQ	–0.5		6.0	V	1
Supply Voltage	V_{CC}	1.2		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	–0.5	0.4	0.8	V	1
Input Logic High	V_{IH}	V_{CC}–0.5		6.0	V	1
Sink Current	I_L	1	2		mA	4
Output Logic Low	V_{OL}			0.4	V	1
Output Logic High	V_{OH}	V_{PUP}		5.5	V	1, 2
Input Resistance	I_R		500		kΩ	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		2	25	nA	6

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=1.4V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	–0.5		0.2	V	1
Input Logic High	V_{IH}	1.0		6.0	V	1
Sink Current	I_L	1	2		mA	7
Output Logic Low	V_{OL}			0.4	V	4
Output Logic High	V_{OH}	V_{PUP}		5.5	V	1, 2
Input Resistance	I_R		500		kΩ	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		2	15	nA	6

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=1.4V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	70			µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60			µs	
Data Setup Time	t_{SU}			1	µs	8
Recovery Time	t_{REC}	1			µs	

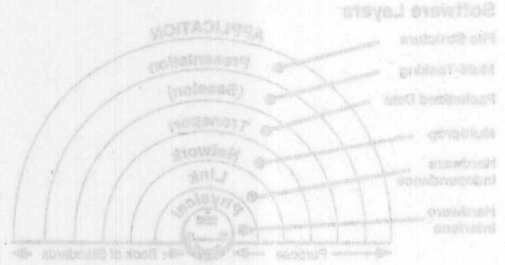
AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60			µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60			µs	
Data Setup Time	t_{SU}			1	µs	8
Recovery Time	t_{REC}	1			µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage to system sypply.
3. Input pull–down resistance to ground.
4. @ V_{OL}=0.4V
5. 36 nanocoulombs per 264 time slots @ 1.5V (see Figure 6).
6. See Figure 7 for typical values over temperature.
7. @ V_{OL}=0.2V
8. Read data setup time refers to the time the host must pull the 1–Wire line low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum (15 µs total from falling edge on the 1–Wire line).



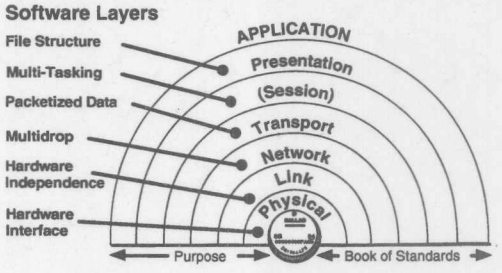
DALLAS SEMICONDUCTOR

DS0620
TMEX Professional Developer's Upgrade Kit for DS9092K

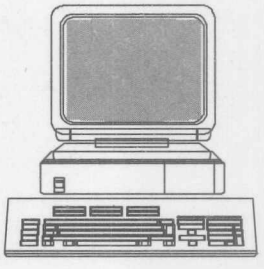
FEATURES

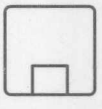
- Software support package for the Touch Memory EXecutive (TMEX)
- Language–independent support for the Touch Memory Extended File Structure on IBM PCs, compatibles, and MS DOS handhelds
- Supports MS Windows with universally callable DLLs
- Supports MS DOS with installable interrupt service routines
- Includes Touch Memory utilities similar to FORMAT, DIR, TYPE, COPY, RENAME, DELETE, CHKDSK, and DISKCOPY, and utilities to examine file attributes and perform storage optimization and defragmentation
- Includes example programs for MS DOS written in C, Pascal, and QuickBasic, and MS Windows examples written in C, Pascal, and Visual Basic

TOUCH MEMORY EXECUTIVE TMEX



Platforms for: PC (DOS and Windows)





DEVELOPER'S UPGRADE KIT

DESCRIPTION

The DS0620 TMEX Professional Developer's Kit provides the software needed to implement the Touch Memory EXecutive (TMEX) on IBM PCs, compatibles, and popular MS DOS handheld computers. Documentation of TMEX is provided in the Book of DS19xx Touch Memory Standards, second edition, available in the DS9092K Touch Memory Starter Kit. Additional documentation on diskette describes the many coding examples, utility programs, and special versions of TMEX for particular handheld MS DOS computers.

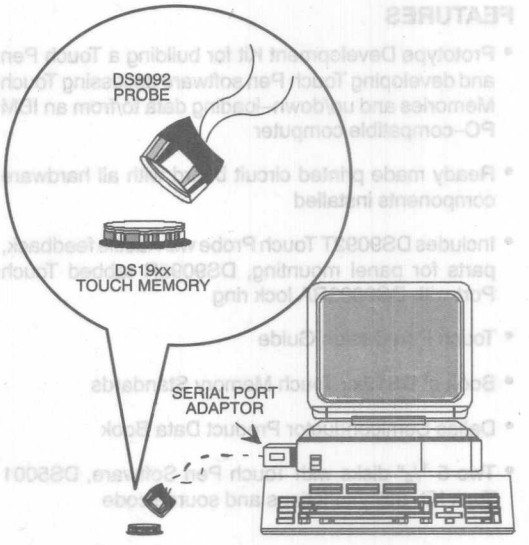
Low–level drivers are supplied with TMEX for use with the DS9097 COM Port Adapter, which attaches to any serial port of a PC. Low–level user–written drivers for specialized Touch Memory I/O hardware can easily be interfaced with the high–level TMEX code provided in this kit to provide full functionality. The DS0620 is supplied on 3 1/2" high density MS–DOS diskettes. The code provided with the DS0620 is licensed for individual use. Licenses are available for multiple installations – contact Dallas Semiconductor for details.

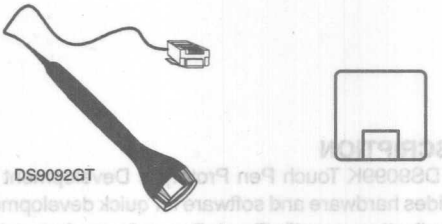
DALLAS SEMICONDUCTOR

DS9092K
Touch Memory Starter Kit

FEATURES

- Evaluation Kit for accessing Touch Memories from an IBM PC–compatible computer
- Assortment of Touch Memory devices
- Assortment of Touch Memory attachment accessories
- DS9092 Touch Memory Probe
- DS9092GT Touch Memory Probe with Hand Grip
- PC serial port adapter
- Book of DS19xx Touch Memory Standards
- Data sheets and application notes
- $3^1/_2$" disk with demonstration software, utility functions and source code





DESCRIPTION

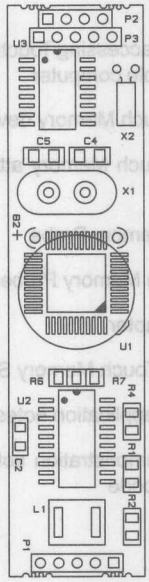
The DS9092K Touch Memory Starter Kit provides hardware and software for quick evaluation of any of Dallas Semiconductor's Touch Memory family using a PC–compatible DOS computer. Included in the kit are Touch Memory devices, a DS9092 and DS9092GT Touch Probe, a PC serial port adapter, an assortment of Touch memory attachment accessories, demonstration software and utility programs. The demonstration programs can be executed to read or write a Touch Memory device through the serial port via a 25–pin adapter which connects to the DS9092GT probe. The utility disk allows the user to quickly develop his own Touch Memory programs from the code provided.

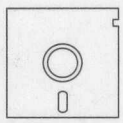
DALLAS SEMICONDUCTOR

DS9099K
Touch Pen Development Kit
DS9099
Touch Pen Chip Set

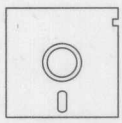
FEATURES

- Prototype Development Kit for building a Touch Pen and developing Touch Pen software accessing Touch Memories and up/down–loading data to/from an IBM PC–compatible computer
- Ready made printed circuit board with all hardware components installed
- Includes DS9092T Touch Probe with tactile feedback, parts for panel mounting, DS9092R tabbed Touch Port with DS9093RA lock ring
- Touch Pen Design Guide
- Book of DS19xx Touch Memory Standards
- Dallas Semiconductor Product Data Book
- Two 5 1/4" disks with Touch Pen Software, DS5001 Took Kit, utility functions and source code





TOUCH PEN



TOOL KIT

DESCRIPTION

The DS9099K Touch Pen Prototype Development Kit provides hardware and software for quick development of application–specific Touch Pen software for reading and writing Touch Memories as well as for up/down–loading Touch Memory data to/from an IBM PC–compatible computer. Further documentation provided on disk includes the full specification of the Extended File Structure as it is used to access multiple independent files stored in Touch Memories. The DS9099K contains a fully functional Touch Pen evaluation board with the most recent firmware preloaded into the DS5001. There is no enclosure included for the circuit board.

This kit assumes availability of Touch Memories, RS232 COM port adapters DS9097 and DS9062 and the DS9060 RS232–fixture at the developer's site. All of these parts together with operating software are found in the DS9092K Touch Memory Starter Kit (DS9097, Touch Memories, Touch Memory Probe) and the DS5000 TK Soft Microcontroller Evaluation Kit (DS9062 COM port adapter, DS9060 RS232–fixture).

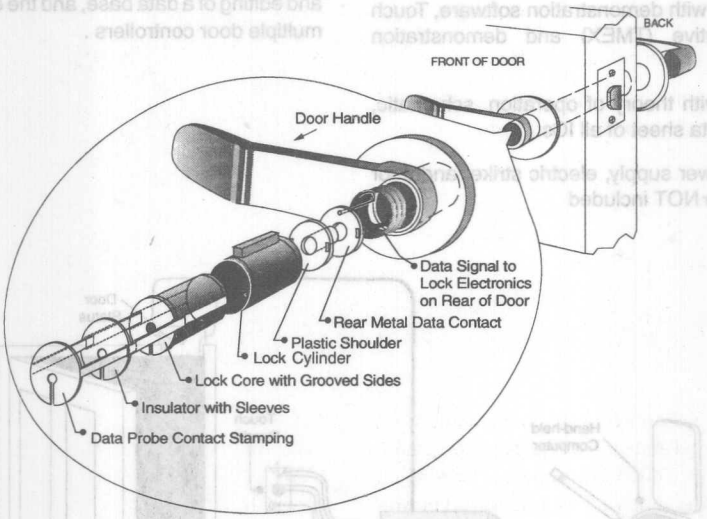
The DS5001FPN4 Microcontroller Chip, DS1227S Kickstarter, DS2404S–C01 Dual Port Memory Plus Time, DS9092T Touch Probe, DS9092R Touch Port, DS9093RA Lock Ring, DS9032 32.786 KHz crystal and CR1632 lithium battery are available as the Touch Pen Chip Set DS9099.

DALLAS SEMICONDUCTOR

DS9102K
Touch Memory Electronic Lock Demo Kit

FEATURES

- Demonstration kit shows the use of Touch Memory as an electronic key and the design of a conventional looking electronic lock that it will operate
- Touch Memory key provides the fastest entry of any key
- Touch Memory probe peacefully coexist with the mechanical lock core face, leaving a mechanical backup if necessary
- Key management is simplified, rekeys in seconds without the addition or removal of parts



DESCRIPTION

The DS9102K Touch Memory Lock Demo Kit provides the user with a starting point for integrating Touch Memory electronics into any mechanical locking system. The electronic circuit board and associated components in this kit provide a reader/writer interface between the Touch Memory key and the electro–mechanical actuator in the desired locking system.

The core electronics in this demo kit are borrowed from the TouchPen design, which is detailed in the "50 Ways to Touch Memory" book second edition. This demo kit focuses on software and implementation of the TouchPen hardware for the application in locks.

DALLAS SEMICONDUCTOR

DS9103K
Touch Memory Access Control Demo Kit

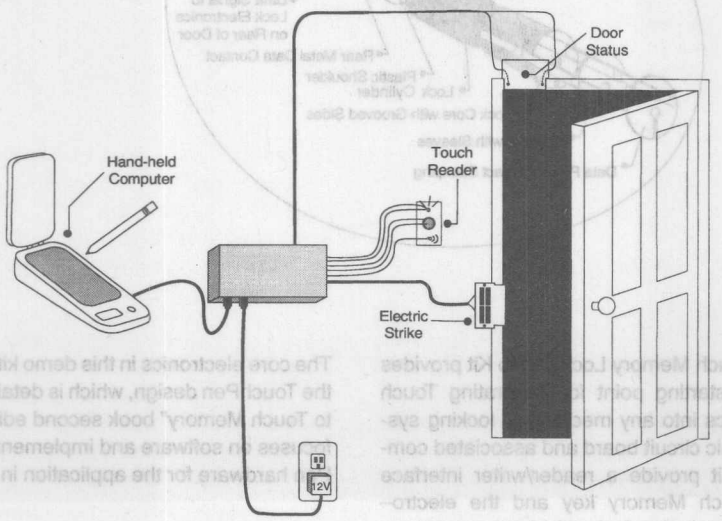
FEATURES

- Demonstration kit shows the use of Touch Memory as an electronic key with other 1–wire devices operating a door controller from an IBM PC–compatible computer
- Three DS1990A–F5 and DS9093F (combined as a Touch Memory Keys)
- Single door access controller circuit board, assembled as three detachable circuit boards: PC Interface, Door Controller, and Door Reader
- Demo circuit board separates for easy trial installation
- Diskette (3 1/2") with demonstration software, Touch Memory EXecutive (TMEX) and demonstration source code
- Users Manual with theory of operation, schematic, parts list, and data sheet of all ICs
- PC, +12 volt power supply, electric strike, and door status switch are NOT included

DESCRIPTION

The DS9103K Touch Memory Access Control Demonstration Kit shows how Touch Memory can be used as an electronic key in an uncomplicated, low–cost, single or multi–door access control system. This system utilizes a 1–wire communication network called a MicroLAN. The PC operates as the MicroLAN host which reads the Touch Memory and controls other 1–wire devices like the DS2405 Addressable Switch to energize relays and collect the status of door position switches.

The demonstration kit software allows for the creation and editing of a data base, and the elemental addition of multiple door controllers .



DALLAS SEMICONDUCTOR

Application Note 74
Reading and Writing Touch Memories via Serial Interfaces

I. INTRODUCTION

Touch Memory is a chip housed in a stainless steel enclosure. The electrical interface is reduced to the absolute minimum, i.e., a single data line plus a ground reference. The energy needed for operation is either "stolen" from the data line ("parasitic power") or is taken from an embedded lithium cell. The logical functions range from a simple serial number to password–protected memory, to 64K bits and beyond of nonvolatile RAM or EPROM, to a Touch Thermometer, to a real time clock plus 4K bits of nonvolatile RAM. Common to all Touch Memories is a globally unique registration number, the serial 1–Wire protocol, presence detect, and communication in discrete time slots. Table 1 gives an overview of the available devices.

For read operations all devices are satisfied with a 5kΩ pull–up resistor to supply energy and to terminate the 1–Wire bus. Touch Memory devices based on non–volatile RAM (DS1991 to DS1996) can also be written using this same interface. Due to their different technology, EPROM based Touch Memories (DS1982 to DS1986) also require pulses of up to 12V for programming. Since they cannot be erased, EPROM Touch Memories are referred to as Add–Only Memories. Another device, the DS1920 Touch Thermometer, gets its energy for temperature conversion through a low impedance active pull–up to 5V. Different requirements for writing or special functions are the reason for several types of interfaces.

TOUCH MEMORY DEVICES Table 1

Device Type	Family Code	Serial Number	Memory Bits Type	Protected NV RAM bits	Real Time Clock	Interval Timer	Cycle Counter
DS1990A	01H	yes	—	—	—	—	—
DS1991	02H	yes	512, NVRAM	3 * 384	—	—	—
DS1992	08H	yes	1K, NVRAM	—	—	—	—
DS1993	06H	yes	4K, NVRAM	—	—	—	—
DS1994	04H	yes	4K, NVRAM	—	yes	yes	yes
DS1995	0AH	yes	16K, NVRAM	—	—	—	—
DS1996	0CH	yes	64K, NVRAM	—	—	—	—
DS1982	09H	yes	1K, EPROM	—	—	—	—
DS1985	0BH	yes	16K, EPROM	—	—	—	—
DS1986	0FH	yes	64K, EPROM	—	—	—	—
DS1920	10H	yes	16, EEPROM	TOUCH THERMOMETER			

II. 1–WIRE INTERFACE

A. General Information

Touch Memories are self–timed silicon devices. The timing logic provides a means of measuring and generating digital pulses of various widths. Data transfers are bit–sequential and half–duplex. Data can be interpreted as commands (according to the prearranged format identified by the family code) that are compared to information already stored in the Touch Memory to make a decision, or can simply be stored in the Touch Memory for later retrieval. Touch Memories are considered slaves, while the host reader/writer is considered a master.

B. DC requirements

Touch Memories operate in an open drain environment on voltage levels ranging from 2.8V (minimum pull–up voltage) to 6V (maximum pull–up voltage). All voltages greater than 2.2V are interpreted as logic 1 or HIGH, voltages less than 0.8V are considered as logic 0 or LOW. The pull–up voltage must be a minimum of 2.8V to recharge an internal storage capacitor that is used to supply power during periods when the data line is low. The size of this capacitor is about 800 pF. This capacity is seen for a short time when a Touch Memory is contacted by a probe. After the capacitor is charged, only a very small fraction of this capacity is recognizable, according to the charge required to refill to full charge. The total time constant to charge the capacitor is defined by the capacitor itself, the internal resistances of about 1 kΩ, the resistance of the cable and contacts, the cable capacitance, and the resistor pulling up the data line.

C. AC requirements

Timing relationships in Touch Memories are defined with respect to time slots. Because the falling slope is the least sensitive to capacitive loading in an open drain environment, Touch Memories use this edge to synchronize their internal timing circuitry. By definition the active part of a 1–Wire time slot (t_{SLOT}) is 60 µs. After the active part of the time slot, the data line needs to be inactive for a minimum of 1 µs at a voltage of 2.8V or higher to recharge the internal capacitor.

Under nominal conditions, a Touch Memory will sample the line 30 µs after the falling edge of the start condition. The internal time base of Touch Memory may deviate from its nominal value. The allowed tolerance band ranges from 15 µs to 60 µs. This means that the actual slave sampling may occur anywhere between 15 and 60 µs after the start condition, which is a ratio of 1 to 4. During this time frame the voltage on the data line must stay below V_{ILMAX} or above V_{IHMIN}.

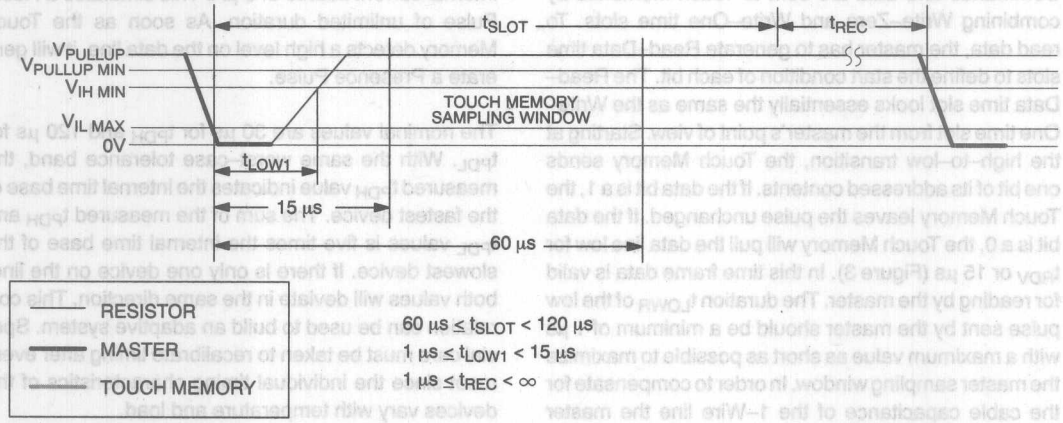
C.1. Write Time Slots

In the 1–Wire system, the logical values of 1 and 0 are represented by certain voltage levels in special waveforms. The waveforms needed to write commands or data to Touch Memories are called write–1 and write–0 time slots. The duration of a low pulse to write a 1 (t_{LOW1}, Figure 1) must be shorter than 15 µs. To write a 0, the duration of the low pulse (t_{LOW0}, Figure 2) must be at least 60 µs to cope with worst–case conditions.

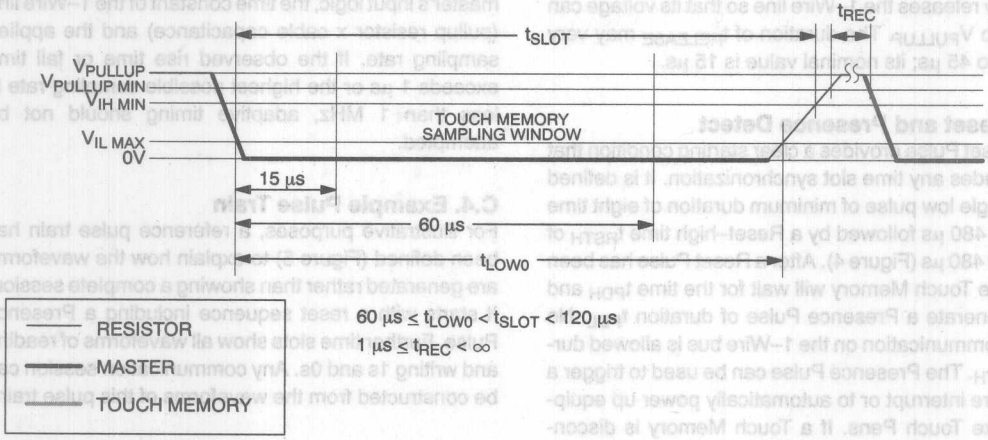
The duration of the active part of a time slot can be extended beyond 60 µs. The maximum extension is limited by the fact that a low pulse of a duration of at least eight active time slots (480 µs) is defined as a Reset Pulse. Allowing the same worst–case tolerance ratio, a low pulse of 120 µs might be sufficient for a reset. This limits the extension of the active part of a time slot to a maximum of 120 µs to prevent misinterpretation with reset.

At the end of the active part of each time slot, Touch Memory needs a recovery time t_{REC} of a minimum of 1 µs to prepare for the next bit. This recovery time is the inactive part of a time slot, since it must be added to the duration of the active part to obtain the time it takes to transfer one bit. The wide tolerance of the time slots and the non–critical recovery time allow even slow microprocessors to meet the timing requirements for 1–Wire communication easily.

WRITE–ONE TIME SLOT Figure 1



WRITE–ZERO TIME SLOT Figure 2



C.2. Read Time Slots

Commands and data are sent to Touch Memories by combining Write–Zero and Write–One time slots. To read data, the master has to generate Read–Data time slots to define the start condition of each bit. The Read–Data time slot looks essentially the same as the Write–One time slot from the master's point of view. Starting at the high–to–low transition, the Touch Memory sends one bit of its addressed contents. If the data bit is a 1, the Touch Memory leaves the pulse unchanged. If the data bit is a 0, the Touch Memory will pull the data line low for t_{RDV} or 15 µs (Figure 3). In this time frame data is valid for reading by the master. The duration t_{LOWR} of the low pulse sent by the master should be a minimum of 1 µs with a maximum value as short as possible to maximize the master sampling window. In order to compensate for the cable capacitance of the 1–Wire line the master should sample as close to 15 µs after the synchronization edge as possible. Following t_{RDV} there is an additional time interval, $t_{RELEASE}$, after which the Touch Memory releases the 1–Wire line so that its voltage can return to V_{PULLUP}. The duration of $t_{RELEASE}$ may vary from 0 to 45 µs; its nominal value is 15 µs.

C.3. Reset and Presence Detect

The Reset Pulse provides a clear starting condition that supersedes any time slot synchronization. It is defined as a single low pulse of minimum duration of eight time slots or 480 µs followed by a Reset–high time t_{RSTH} of another 480 µs (Figure 4). After a Reset Pulse has been sent, the Touch Memory will wait for the time t_{PDH} and then generate a Presence Pulse of duration t_{PDL}. No other communication on the 1–Wire bus is allowed during t_{RSTH}. The Presence Pulse can be used to trigger a hardware interrupt or to automatically power up equipment like Touch Pens. If a Touch Memory is disconnected from the probe, it will pull its data line low via an internal current source of 5 µA. This simulates a Reset Pulse of unlimited duration. As soon as the Touch Memory detects a high level on the data line, it will generate a Presence Pulse.

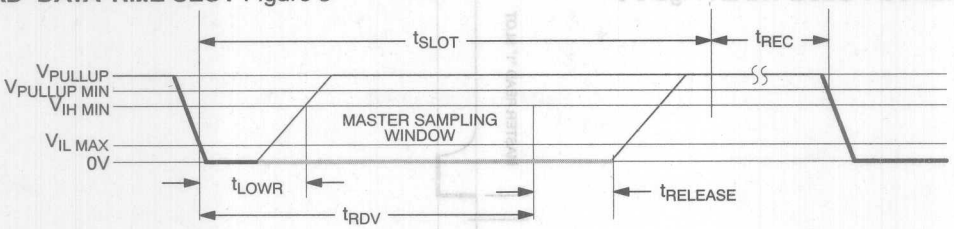
The nominal values are 30 µs for t_{PDH} and 120 µs for t_{PDL}. With the same worst–case tolerance band, the measured t_{PDH} value indicates the internal time base of the fastest device. The sum of the measured t_{PDH} and t_{PDL} values is five times the internal time base of the slowest device. If there is only one device on the line, both values will deviate in the same direction. This correlation can be used to build an adaptive system. Special care must be taken to recalibrate timing after every reset since the individual timing characteristics of the devices vary with temperature and load.

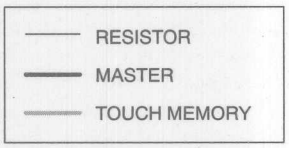
The accuracy of the time measurements required for adaptive timing is limited by the characteristics of the master's input logic, the time constant of the 1–Wire line (pullup resistor x cable capacitance) and the applied sampling rate. If the observed rise time or fall time exceeds 1 µs or the highest possible sampling rate is less than 1 MHz, adaptive timing should not be attempted.

C.4. Example Pulse Train

For illustrative purposes, a reference pulse train has been defined (Figure 5) to explain how the waveforms are generated rather than showing a complete session. It starts with a reset sequence including a Presence Pulse. Further time slots show all waveforms of reading and writing 1s and 0s. Any communication session can be constructed from the waveforms of this pulse train.

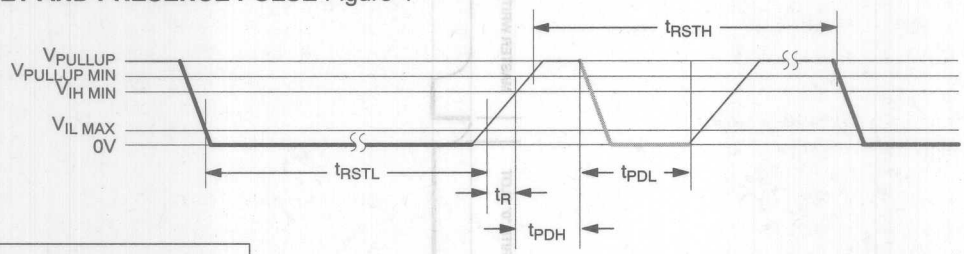
READ–DATA TIME SLOT Figure 3

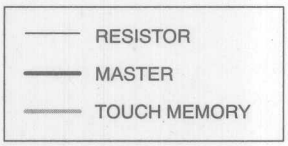




$60\ \mu s \le t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{LOWR} < 15\ \mu s$
$0 \le t_{RELEASE} < 45\ \mu s$
$1\ \mu s \le t_{REC} < \infty$
$t_{RDV} = 15\ \mu s$

RESET AND PRESENCE PULSE Figure 4

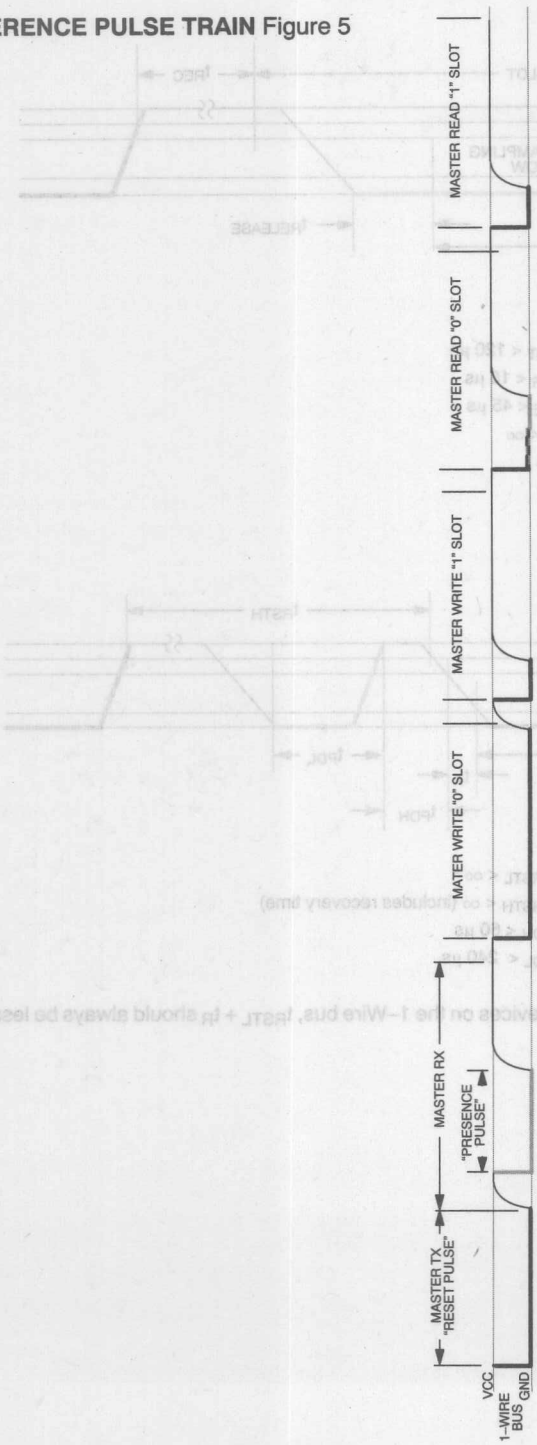




$480\ \mu s \le t_{RSTL} < \infty$ *
$480\ \mu s \le t_{RSTH} < \infty$ (includes recovery time)
$15\ \mu s \le t_{PDH} < 60\ \mu s$
$60\ \mu s \le t_{PDL} < 240\ \mu s$

* In order not to mask interrupt signalling by other devices on the 1–Wire bus, $t_{RSTL} + t_R$ should always be less than 960 μs.

REFERENCE PULSE TRAIN Figure 5



III. FUNDAMENTALS

A. TTL Interface

This category includes all logic families and microprocessors that use positive logic with a maximum 0.8V for a logical 0 or LOW and a minimum of 2.2V for a logical 1 or HIGH. These voltages combined with a current source capability of at least 1 mA and a sink capability of more than 4 mA interface to a broad class of digital electronics.

Since the 1–Wire bus is an open drain system, an open drain/collector driver is required to connect the output port to the bus (Figure 6). This driver can be a general purpose NPN transistor with a resistor connected between base and output port or an n–channel MOSFET or any open drain/collector driver available in the logic family as long as the pullup voltage is equal to the driver voltage. Even a tri–state driver with its logic input tied to ground can be used, connecting the output gate to the tri–state control input. Depending on the characteristics of the driver (inverting/non–inverting), it may be required to complement the logic value of the output gate to compensate for the driver's signal inversion.

Reading from the 1–Wire bus can usually be accomplished by directly connecting the 1–Wire bus to the input port of the master. If the pullup–voltage of the 1–wire bus is too low or if the capacity of the cable produces slopes too slow for the logic family, it may be required to employ a comparator as interface and to adjust the reference voltage to optimize noise margins and timing characteristics. If the comparator inverts the signal, this inversion needs to be compensated by the software.

Generally it is recommended to test this type of interface carefully, starting with reset pulses generated by software and watching the slopes with an oscilloscope. If the timing specifications of Figure 4 are met, and the presence pulse is seen, one may proceed and test the software to generate the Write–Zero and Write–One time slots. After this works properly, the next step is reading the ROM. This is done by performing a reset cycle first, followed by 2 Write–One time slots, 2 Write–Zero time slots, 2 Write–One time slots and 2 Write–Zero time slots (this is equivalent to sending 33H, least significant bit first). After this, 64 Read Data time slots need to be generated.

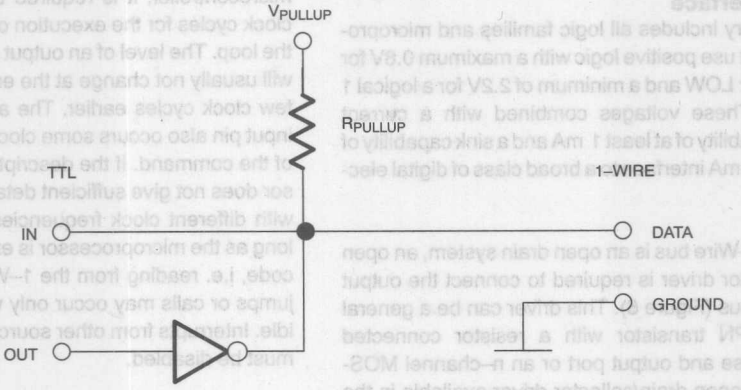
Since all timing depends on the clock frequency of the microcontroller, it is required to count the number of clock cycles for the execution of each command within the loop. The level of an output pin of a microprocessor will usually not change at the end of a command, but a few clock cycles earlier. The actual reading from any input pin also occurs some clock cycles before the end of the command. If the description of the microprocessor does not give sufficient details on this, a test series with different clock frequencies may be required. As long as the microprocessor is executing time–sensitive code, i.e. reading from the 1–Wire bus or writing to it, jumps or calls may occur only while the 1–Wire bus is idle. Interrupts from other sources than the 1–Wire bus must be disabled.

B. RS232 Interface

This section covers all interfaces that use a special controller to generate all timing and reference signals required for serial communication. The typical controller for this type of interface is the UART 8250. It relieves the microprocessor of the burden of time–critical software execution. The microprocessor simply puts the character code to be transmitted into the transmit register of the UART and the UART will do the work. A character is received by the microprocessor just by reading the UART's receive register. If the serial transmission is finished or if there is data for the microprocessor, this condition is signalled by the UART through flags that can be polled or by interrupts.

To function properly, the UART requires configuration with respect to baud rate, number of data bits per character, parity and number of start and stop bits. These terms are common for serial communication, but fit the needs of 1–Wire networks with their time slots and separate synchronization if a bit rather than a character is framed by the start condition. For 1–Wire communication the UART is set up for a high baud rate and each character delivered by the UART represents a bit on the 1–Wire bus. The microprocessor must separate the bits of a byte, least significant bit first, and write them as appropriate characters to the UART. To read data, the microprocessor has to assemble the bits received through characters back into bytes. These functions are not time–sensitive and can easily be programmed in a high level language.

TTL INTERFACING Figure 6



RS232 Conventions

Unlike TTL logic, RS232 has been established to transport data over long lines. Therefore different current drive characteristics and higher voltages are required to represent the logic levels 0 and 1.

The values to be expected are:

+3V to +15V for 0,
which is identical to the polarity of the start bit and
–3V to –15V for 1,
which is identical to the polarity of the stop bit and the idle state. The voltage range from –3V to +3V is undefined.

All voltages are measured with respect to ground. The receive channel and the transmit channel are independent wires, called RXD and TXD. Since RS232 ports are often used for communication via phone lines, several control signals are also included in the standard. Not all of these control signals need to be implemented with a communication device. For 1–Wire applications only the control signals DTR (Data Terminal Ready) and RTS (Request to send) are needed. Other signals often found with RS232 are DSR (Data Set Ready), which is the response to DTR, and CTS (Clear To Send), which is the response to RTS. How these signals are provided on a connector is detailed in Table 2. Full documentation on RS232 is beyond the scope of this application note. For a complete description please refer to other literature.

Table 2

SIGNAL	9–PIN CONNECTOR	25–PIN CONNECTOR	DESCRIPTION	FUNCTION
RXD	2	3	Receive Data	input
TXD	3	2	Transmit Data	output
DTR	4	20	Data Terminal Ready	output
RTS	7	4	Request to Send	output
GND	5	7	Ground	(reference)
DSR	6	6	Data Set Ready	input
CTS	8	5	Clear to Send	input

Hardware simplified model

The standard hardware of a RS232 interface is shown in Figure 7a. The UART is hooked to the system bus like an 8–bit memory device. The three address inputs A0 to A2 make the UART appear as a block of 8 read/write memory locations. On the other side there are the serial communication signals and the control signals mentioned above. Since the UART is a 5V–device, special drivers and receivers for handling higher voltages are required. Circuit diagrams of bipolar integrated drivers (1488) and receivers (1489) are shown on Figures 7b and 7c. CMOS drivers and receivers are also available as standard products.

By design, the output current of an RS232 driver is limited to ±10 mA typically. Since the voltage definitions for 1 and 0 on the RS232 channel are reversed with respect to the conventions of positive logic, RS232 drivers and receivers are actually inverting devices. The inversion in the transmit channel is compensated through an inversion in the receive channel. Thus a 1 written to the transmit register will appear as a 1 at the serial output, as –15V at TXD, as a 1 at the serial input of the receiver and finally be read as a 1 in the receive register of the receiving UART.

For energy efficiency with battery operated equipment, the RS232 drivers and receivers are often replaced by simple 5V inverting drivers. This is definitely not compatible with the RS232 standard, but may be sufficient to control a modem or to transfer data through a short cable. Interfaces like this are called 5V RS232 within this application note. They run on the same software as the standard RS232, but are electrically almost the same as the TTL interface.

Programmer's model

To write software for the 8250 UART one must know the basic address where the registers of the UART are hardwired to. This address is generally an equipment specific variable, and therefore will be referenced by the name SPA (Serial Port Address) rather than by a physical address. Of the 8 theoretically accessible addresses within the UART only 7 are really implemented, using the relative addresses 0 to 6. The names of these registers are as follows:

address:

SPA	+0	Receive (read)/Transmit (write) Data Register
	+1	Interrupt Enable Register
	+2	Interrupt Identification Register (read only)
	+3	Line Control Register
	+4	Modem Control Register
	+5	Line Status Register
	+6	Modem Status Register

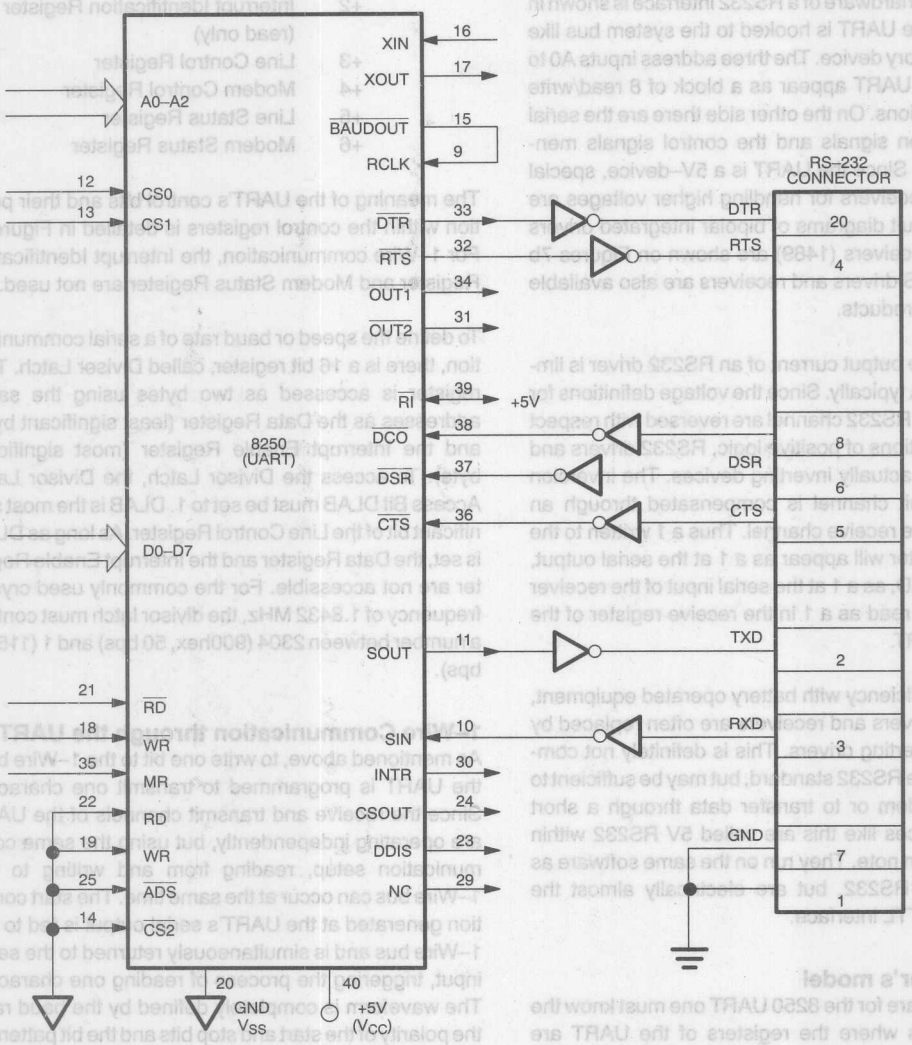
The meaning of the UART's control bits and their position within the control registers is detailed in Figure 8. For 1–Wire communication, the Interrupt Identification Register and Modem Status Register are not used.

To define the speed or baud rate of a serial communication, there is a 16 bit register, called Divisor Latch. This register is accessed as two bytes using the same addresses as the Data Register (least significant byte) and the Interrupt Enable Register (most significant byte). To access the Divisor Latch, the Divisor Latch Access Bit DLAB must be set to 1. DLAB is the most significant bit of the Line Control Register. As long as DLAB is set, the Data Register and the Interrupt Enable Register are not accessible. For the commonly used crystal frequency of 1.8432 MHz, the divisor latch must contain a number between 2304 (900hex, 50 bps) and 1 (115.2k bps).

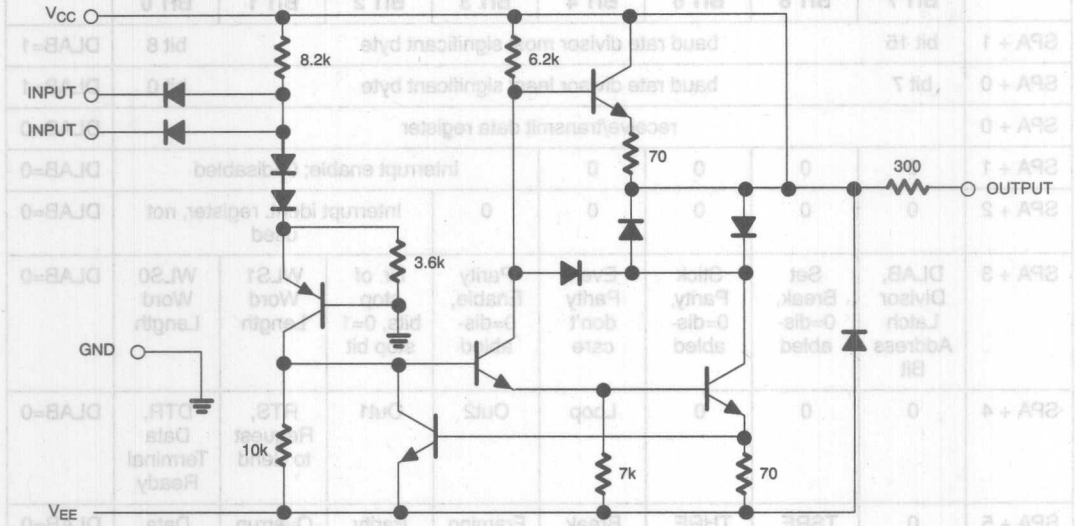
1–Wire Communication through the UART

As mentioned above, to write one bit to the 1–Wire bus, the UART is programmed to transmit one character. Since the receive and transmit channels of the UART are operating independently, but using the same communication setup, reading from and writing to the 1–Wire bus can occur at the same time. The start condition generated at the UART's serial output is fed to the 1–Wire bus and is simultaneously returned to the serial input, triggering the process of reading one character. The waveform is completely defined by the baud rate, the polarity of the start and stop bits and the bit pattern of the character. The serial output of the UART is high (~5V, idle) between characters, low (~0V) for the start bit and equal to the value of the data bit being transmitted. An idle (~5V) to low (~0V) transition at the UART's serial input triggers the process of receiving a character. The first bit is understood as start bit; the remaining bits are shifted into the receive register in the same polarity as they arrive at the serial input. Bits received after the receive register is full, are ignored.

HARDWARE OVERALL CONCEPT Figure 7a



TYPICAL DRIVER Figure 7b



TYPICAL RECEIVER Figure 7c

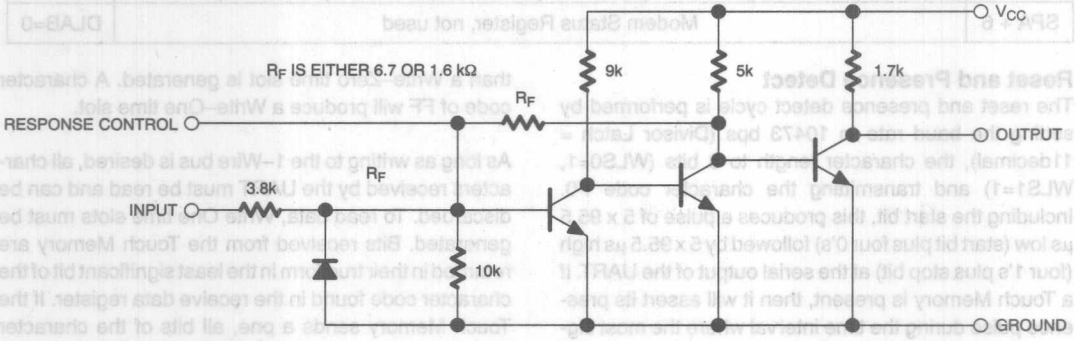


Figure 8

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
SPA + 1	bit 15			baud rate divisor most significant byte				bit 8	DLAB=1
SPA + 0	bit 7			baud rate divisor least significant byte				bit 0	DLAB=1
SPA + 0				receive/transmit data register					DLAB=0
SPA + 1	0	0	0	0	Interrupt enable; 0=disabled				DLAB=0
SPA + 2	0	0	0	0	0	Interrupt ident. register, not used			DLAB=0
SPA + 3	DLAB, Divisor Latch Address Bit	Set Break, 0=disabled	Stick Parity, 0=disabled	Even Parity don't care	Parity Enable, 0=disabled	Nr. of stop bits, 0=1 stop bit	WLS1 Word Length	WLS0 Word Length	DLAB=0
SPA + 4	0	0	0	Loop	Out2	Out1	RTS, Request to Send	DTR, Data Terminal Ready	DLAB=0
SPA + 5	0	TSRE, transmit shift register empty	THRE, transmit hold register empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Data Ready	DLAB=0
SPA + 6	Modem Status Register, not used								DLAB=0

Reset and Presence Detect

The reset and presence detect cycle is performed by setting the baud rate to 10473 bps (Divisor Latch = 11decimal), the character length to 8 bits (WLS0=1, WLS1=1) and transmitting the character code F0. Including the start bit, this produces a pulse of 5 x 95.5 µs low (start bit plus four 0's) followed by 5 x 95.5 µs high (four 1's plus stop bit) at the serial output of the UART. If a Touch Memory is present, then it will assert its presence pulse during the time interval where the most significant bits of the character code are transmitted. If after the transmission the receive data register reads F0, then there is no Touch Memory. If one or more bits of the transmitted F are changed to 0s, than a presence pulse was received.

Read/Write one Bit

To generate data time slots, the UART must be set to a baud rate of 115.2k bps (Divisor Latch = 1). With a character length of 6 bits (WLS0=1, WLS1=0), any transmitted character will consist of a pulse train of 8 x 8.68 µs, beginning with a low start bit, followed by true data bits and a high stop bit. This matches the waveform for fast 1–Wire communication. If the character code is 00, than a Write–Zero time slot is generated. A character code of FF will produce a Write–One time slot.

As long as writing to the 1–Wire bus is desired, all characters received by the UART must be read and can be discarded. To read data, Write One time slots must be generated. Bits received from the Touch Memory are returned in their true form in the least significant bit of the character code found in the receive data register. If the Touch Memory sends a one, all bits of the character code will read one. If the Touch Memory sends a zero, one or more of the least significant bits of the character code will be zero, depending on the internal time base of the Touch Memory.

Not all UARTs behave exactly the same as the 8250. Some of them do not support the character length of 6 bits. To circumvent potential problems from this restriction, the software examples in this document always use the character length of 8 bits. This extends the transmission of one bit by 17.36 µs and reduces the effective baud rate from 14.4k bps to 11.5k bps, but remains well within the specification of 1–Wire timing.

IV. CIRCUITS FOR 5V INTERFACES (TTL AND RS232)

A. TTL read all

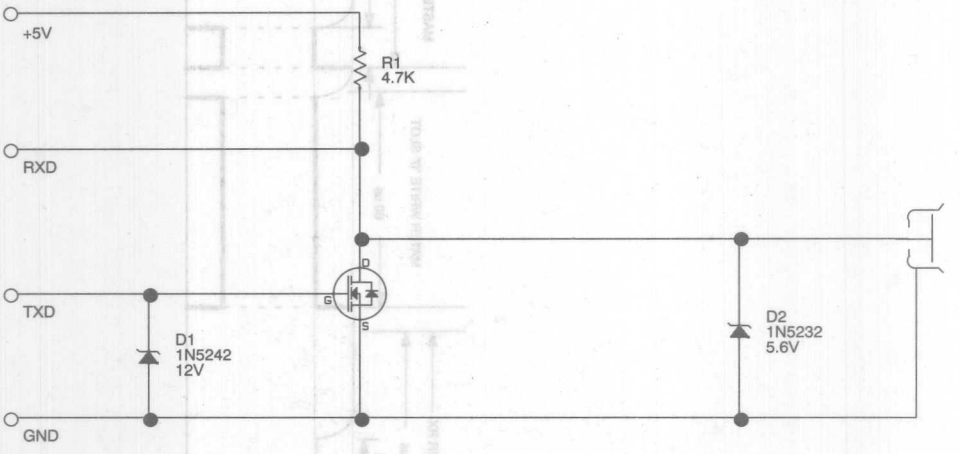
This is the simplest interface for Touch Memory applications. It is suitable for reading all Touch Memories and writing NVRAM based devices. The circuit diagram (Figure 9) conforms to the principle of Figure 6. The diodes D1 and D2 protect transistor Q1 and the input of the microprocessor, respectively, against damage from electrostatic discharge (ESD). R1 is the 1–Wire pullup resistor. If the microprocessor runs on 5V, the same supply can directly be connected to R1. If only a higher supply voltage than 5V is available, any monolithic or discrete positive 5V regulator can be used to provide the pullup voltage for the 1–Wire bus.

The characteristics of the components are not critical. The transistor 2N7000 has been chosen since it is a very common product and has a low threshold voltage.

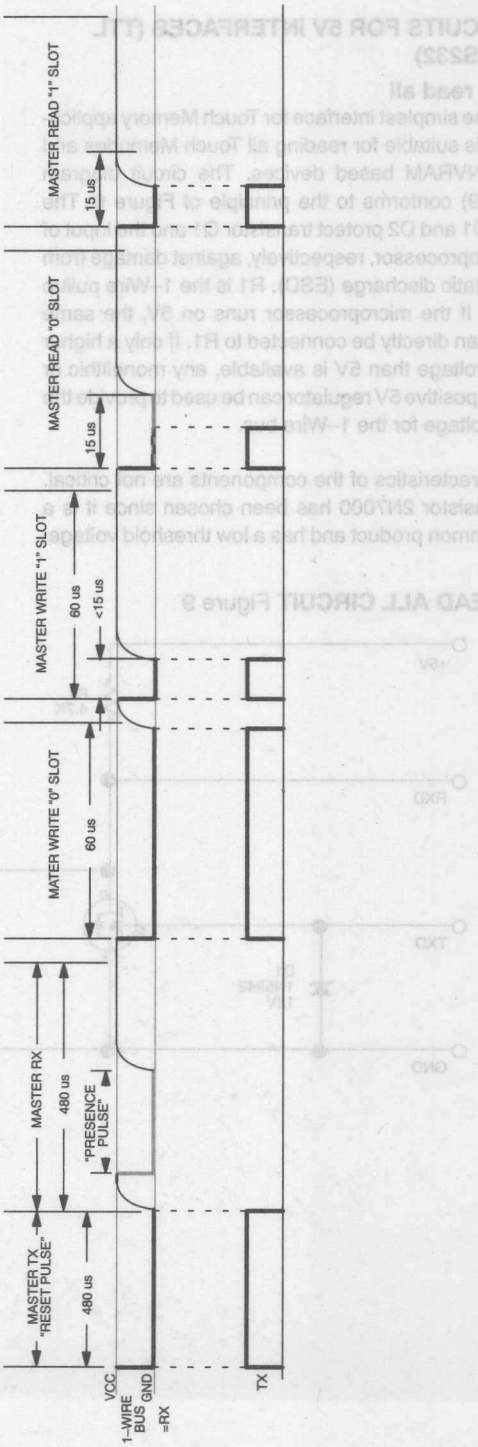
If desired, a small signal bipolar transistor or any available open–drain or open–collector inverting driver can be used instead of Q1. If Q1 is an npn–transistor, a resistor bypassed by a small capacitor between the TX–input and the base terminal is required to limit the input current.

The logic level high at TX will produce a low on the 1–Wire bus. To generate a Write–One or Read Data time slot, a short high pulse ($1\ \mu s < t < 15\ \mu s$) must be applied to the TX input. A Write–Zero Time Slot is formed by a 60 μs high pulse at TX. Data from Touch Memories is received in its true form. If idle, TX must be held at a logic low level. The reference pulse train and other relevant waveforms for this circuit are shown on Figure 9a. The timing for this type of interface is directly generated by the microprocessor. A software example for this type of interface is found later in this document.

TTL READ ALL CIRCUIT Figure 9



TTL READ ALL WAVEFORMS Figure 9a



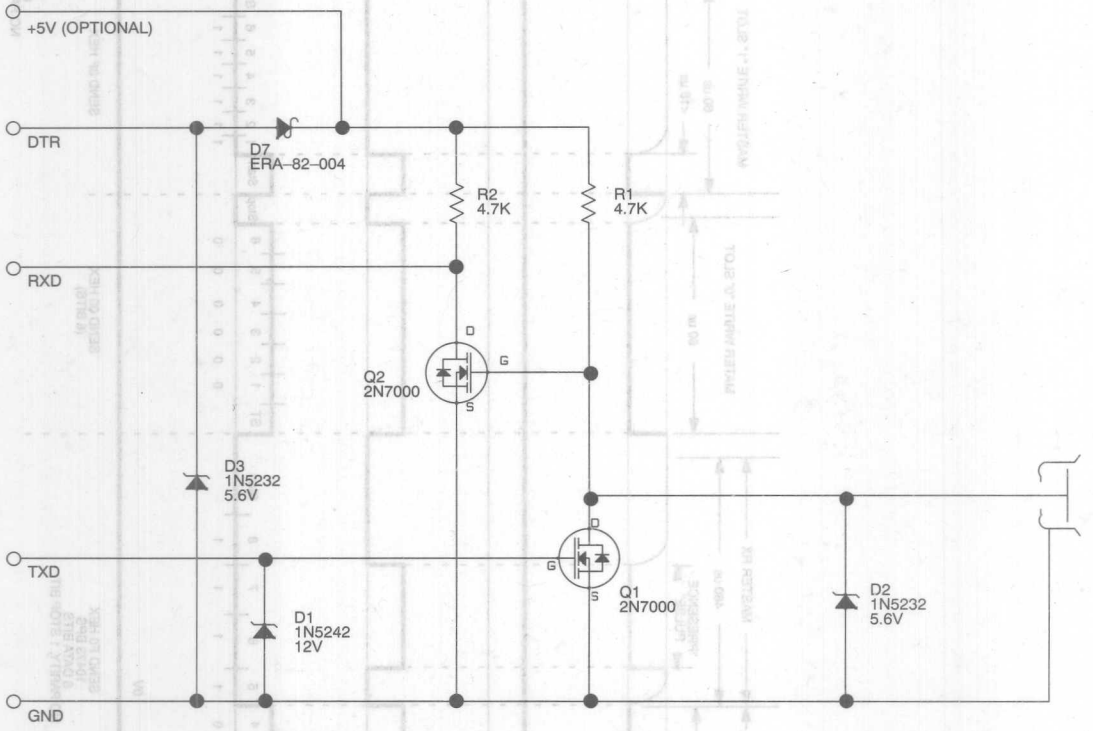
B. 5V RS232 read all

This interface is required for equipment that uses a UART to provide all timing but does not conform to the voltage levels of the RS232 standard. The logic levels, however, are the correct polarity so that it can be operated with the same software as the standard RS232 interface.

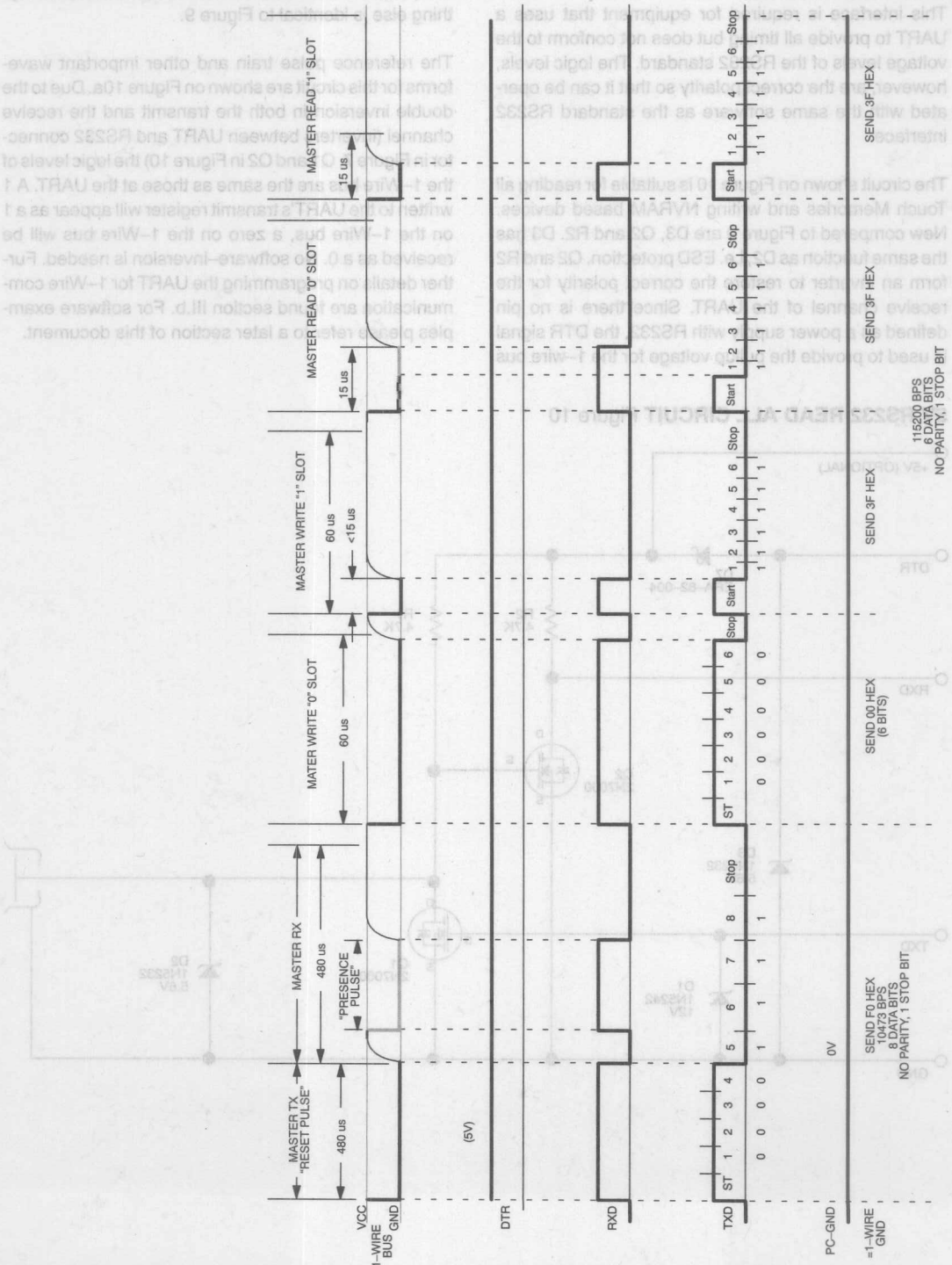
The circuit shown on Figure 10 is suitable for reading all Touch Memories and writing NVRAM based devices. New compared to Figure 9 are D3, Q2 and R2. D3 has the same function as D2, i.e. ESD protection. Q2 and R2 form an inverter to restore the correct polarity for the receive channel of the UART. Since there is no pin defined as a power supply with RS232, the DTR signal is used to provide the pullup voltage for the 1–wire bus and power for the inverter in the receive channel. Everything else is identical to Figure 9.

The reference pulse train and other important waveforms for this circuit are shown on Figure 10a. Due to the double inversion in both the transmit and the receive channel (inverters between UART and RS232 connector in Figure 7, Q1 and Q2 in Figure 10) the logic levels of the 1–Wire bus are the same as those at the UART. A 1 written to the UART's transmit register will appear as a 1 on the 1–Wire bus, a zero on the 1–Wire bus will be received as a 0. No software–inversion is needed. Further details on programming the UART for 1–Wire communication are found section III.b. For software examples please refer to a later section of this document.

5V RS232 READ ALL CIRCUIT Figure 10



5V RS232 READ ALL WAVEFORMS Figure 10a

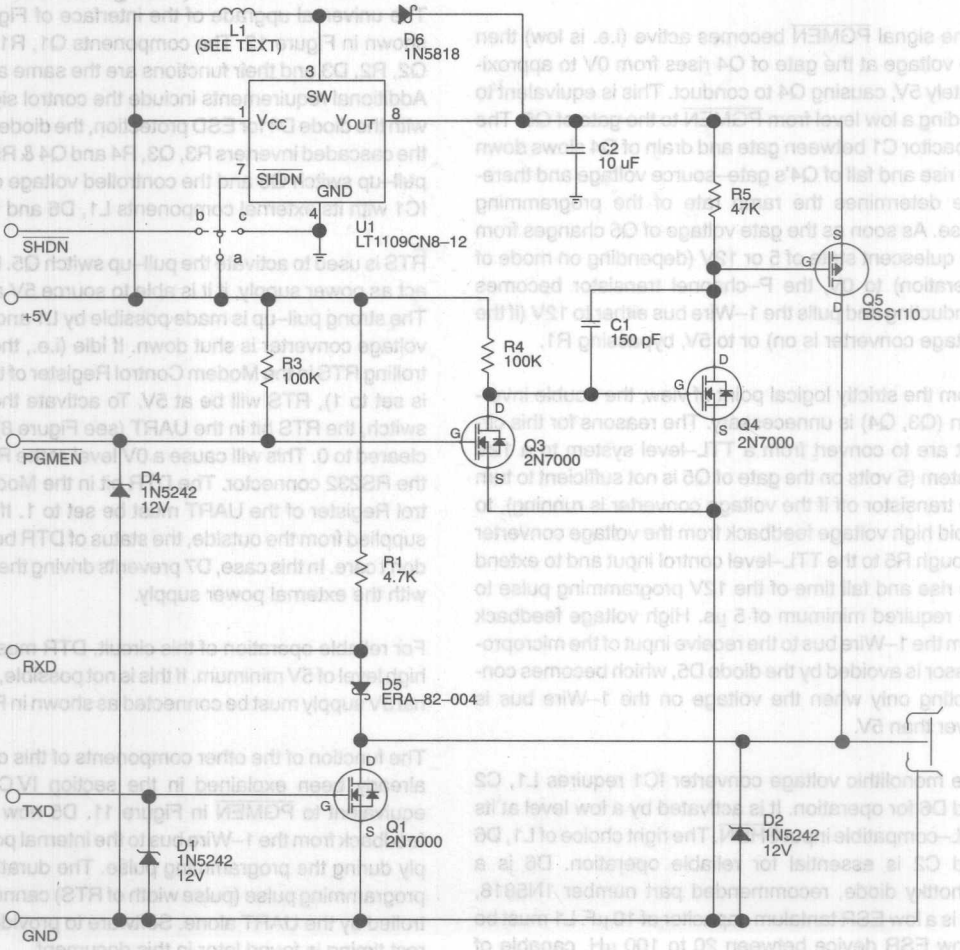


C. TTL R/W all (voltage converter)

The circuits described so far can read all Touch Memories and write NVRAM–based devices. For other technologies, however, voltage requirements other than 5V are necessary. One important group of Touch Memories, called Add–Only Memories, is based on EPROM technology and therefore needs a programming pulse of 12V to copy data from the scratchpad to the EPROM cells. Another device, the Touch Thermometer, will operate on 5V but requires a low impedance pull–up to 5V while measuring the temperature. To fulfill the requirements of these and future devices, the circuits described above need to be upgraded. These two new functions require two more signals and the 12V programming supply can be provided by a DC–to–DC voltage converter.

The complete circuit of such a universal interface in a TTL–version is shown in Figure 11. It is a compatible superset of Figure 9. The components Q1, R1, D1, D2 and their functions are the same as before. Additional requirements include the control input $\overline{\text{PGMEN}}$ with the diode D4 for ESD protection, the diode D5, the cascaded inverters R3, Q3, R4 and Q4 & R5, C1, the pull–up switch Q5 and the controlled voltage converter IC1 with its external components L1, D6 and C2.

TTL R/W ALL CIRCUIT Figure 11



$\overline{\text{PGMEN}}$ is the active low input to activate the pull–up switch. If not connected, $\overline{\text{PGMEN}}$ will be held high through R3 to avoid unwanted activation of the pull–up switch. The voltage converter can be controlled in three ways: a) hard–wired for continuous operation, b) activated by an external signal, or c) permanently shut down. Case a) is intended for applications which never require a strong 5V pull–up. If there is no control signal available from the master and strong 5V pull–up as well as EPROM programming is required, then a mechanical switch can be used to switch between case a) and c). Case b) offers the most flexibility. For EPROM programming $\overline{\text{SHDN}}$ needs to be high, for strong 5V pull–up it should be low. If the voltage converter is shut down, L1 and D6 together with a conducting Q5 provide the required low–impedance path to 5V.

If the signal $\overline{\text{PGMEN}}$ becomes active (i.e. is low) then the voltage at the gate of Q4 rises from 0V to approximately 5V, causing Q4 to conduct. This is equivalent to feeding a low level from $\overline{\text{PGMEN}}$ to the gate of Q5. The capacitor C1 between gate and drain of Q4 slows down the rise and fall of Q4's gate–source voltage and therefore determines the ramp rate of the programming pulse. As soon as the gate voltage of Q5 changes from the quiescent state of 5 or 12V (depending on mode of operation) to 0V, the P–channel transistor becomes conducting and pulls the 1–Wire bus either to 12V (if the voltage converter is on) or to 5V, bypassing R1.

From the strictly logical point of view, the double inversion (Q3, Q4) is unnecessary. The reasons for this circuit are to convert from a TTL–level system to a 12V system (5 volts on the gate of Q5 is not sufficient to turn the transistor off if the voltage converter is running), to avoid high voltage feedback from the voltage converter through R5 to the TTL–level control input and to extend the rise and fall time of the 12V programming pulse to the required minimum of 5 μs. High voltage feedback from the 1–Wire bus to the receive input of the microprocessor is avoided by the diode D5, which becomes conducting only when the voltage on the 1–Wire bus is lower than 5V.

The monolithic voltage converter IC1 requires L1, C2 and D6 for operation. It is activated by a low level at its TTL–compatible input $\overline{\text{SHDN}}$. The right choice of L1, D6 and C2 is essential for reliable operation. D6 is a Schottky diode, recommended part number 1N5818, C2 is a low ESR tantalum capacitor of 10 μF. L1 must be a low ESR device between 20 to 100 μH, capable of withstanding current peaks of approximately 0.5 A without magnetic saturation. To avoid EMI problems, L1 should be a pot–core or toroid type; a rod core type is not recommended. For further details on the voltage converter and its external components please refer to the appropriate data sheet and application notes. The LT1109 is just one example of available parts. Other manufacturer's components or modules can be used as well.

The duration of the programming pulse (pulse width of $\overline{\text{PGMEN}}$) or the strong pull–up is determined by software. Program examples are given later in this document.

D. 5V RS232 R/W all (voltage converter)

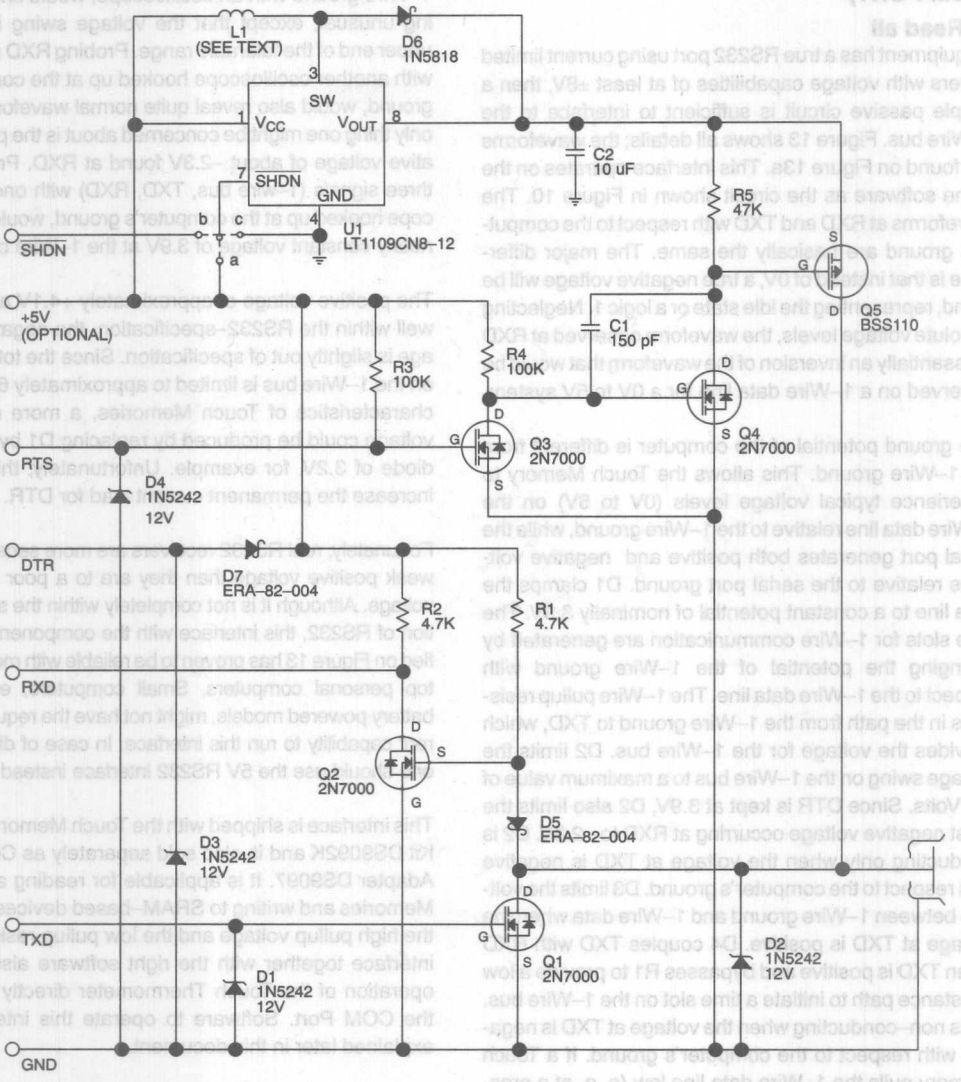
The universal upgrade of the interface of Figure 10 is shown in Figure 12. The components Q1, R1, D1, D2, Q2, R2, D3 and their functions are the same as before. Additional requirements include the control signal RTS with the diode D4 for ESD protection, the diodes D5, D7, the cascaded inverters R3, Q3, R4 and Q4 & R5, C2, the pull–up switch Q5 and the controlled voltage converter IC1 with its external components L1, D6 and C2.

RTS is used to activate the pull–up switch Q5. DTR may act as power supply, if it is able to source 5V at 25 mA. The strong pull–up is made possible by L1 and D6 if the voltage converter is shut down. If idle (i.e., the bit controlling RTS in the Modem Control Register of the UART is set to 1), RTS will be at 5V. To activate the pull–up switch, the RTS bit in the UART (see Figure 8) must be cleared to 0. This will cause a 0V level at the RTS pin of the RS232 connector. The DTR bit in the Modem Control Register of the UART must be set to 1. If power is supplied from the outside, the status of DTR becomes a don't care. In this case, D7 prevents driving the DTR line with the external power supply.

For reliable operation of this circuit, DTR must reach a high level of 5V minimum. If this is not possible, an external 5V supply must be connected as shown in Figure 12.

The function of the other components of this circuit has already been explained in the section IV.C. RTS is equivalent to $\overline{\text{PGMEN}}$ in Figure 11. D5 now prevents feedback from the 1–Wire bus to the internal power supply during the programming pulse. The duration of the programming pulse (pulse width of RTS) cannot be controlled by the UART alone. Software to provide the correct timing is found later in this document.

5V RS232 R/W ALL CIRCUIT Figure 12



V. CIRCUITS FOR 12V RS232 INTERFACES (COM PORT)

A. Read all

If equipment has a true RS232 port using current limited drivers with voltage capabilities of at least ±8V, then a simple passive circuit is sufficient to interface to the 1–Wire bus. Figure 13 shows all details; the waveforms are found on Figure 13a. This interface operates on the same software as the circuit shown in Figure 10. The waveforms at RXD and TXD with respect to the computer's ground are basically the same. The major difference is that instead of 0V, a true negative voltage will be found, representing the idle state or a logic 1. Neglecting absolute voltage levels, the waveform observed at RXD is essentially an inversion of the waveform that would be observed on a 1–Wire data line for a 0V to 5V system.

The ground potential of the computer is different from the 1–Wire ground. This allows the Touch Memory to experience typical voltage levels (0V to 6V) on the 1–Wire data line relative to the 1–Wire ground, while the serial port generates both positive and negative voltages relative to the serial port ground. D1 clamps the data line to a constant potential of nominally 3.9V. The time slots for 1–Wire communication are generated by changing the potential of the 1–Wire ground with respect to the 1–Wire data line. The 1–Wire pullup resistor is in the path from the 1–Wire ground to TXD, which provides the voltage for the 1–Wire bus. D2 limits the voltage swing on the 1–Wire bus to a maximum value of 6.2 Volts. Since DTR is kept at 3.9V, D2 also limits the most negative voltage occurring at RXD to –2.3V. D2 is conducting only when the voltage at TXD is negative with respect to the computer's ground. D3 limits the voltage between 1–Wire ground and 1–Wire data when the voltage at TXD is positive. D4 couples TXD with RXD when TXD is positive and bypasses R1 to provide a low resistance path to initiate a time slot on the 1–Wire bus. D4 is non–conducting when the voltage at TXD is negative with respect to the computer's ground. If a Touch Memory pulls the 1–Wire data line low (e. g. at a presence pulse or when sending out a zero data bit), it shorts DTR to RXD, resulting in a positive voltage at RXD. This positive voltage arrives as a zero in the UART's receive data register.

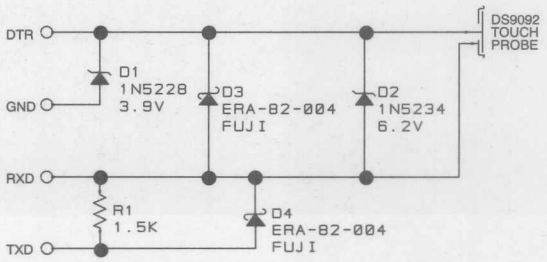
Probing the 1–Wire bus at the data contact and the 1–Wire ground with an oscilloscope, would show nothing unusual, except that the voltage swing is at the upper end of the tolerable range. Probing RXD and TXD with another oscilloscope hooked up at the computer's ground, would also reveal quite normal waveforms. The only thing one might be concerned about is the poor negative voltage of about –2.3V found at RXD. Probing all three signals (1–wire bus, TXD, RXD) with one oscillocope hooked up at the computer's ground, would show a nearly constant voltage of 3.9V at the 1–Wire bus.

The positive voltage of approximately +4.1V at RXD is well within the RS232–specification, the negative voltage is slightly out of specification. Since the total swing on the 1–Wire bus is limited to approximately 6V by the characteristics of Touch Memories, a more negative voltage could be produced by replacing D1 by a zener diode of 3.2V, for example. Unfortunately, this would increase the permanent current load for DTR.

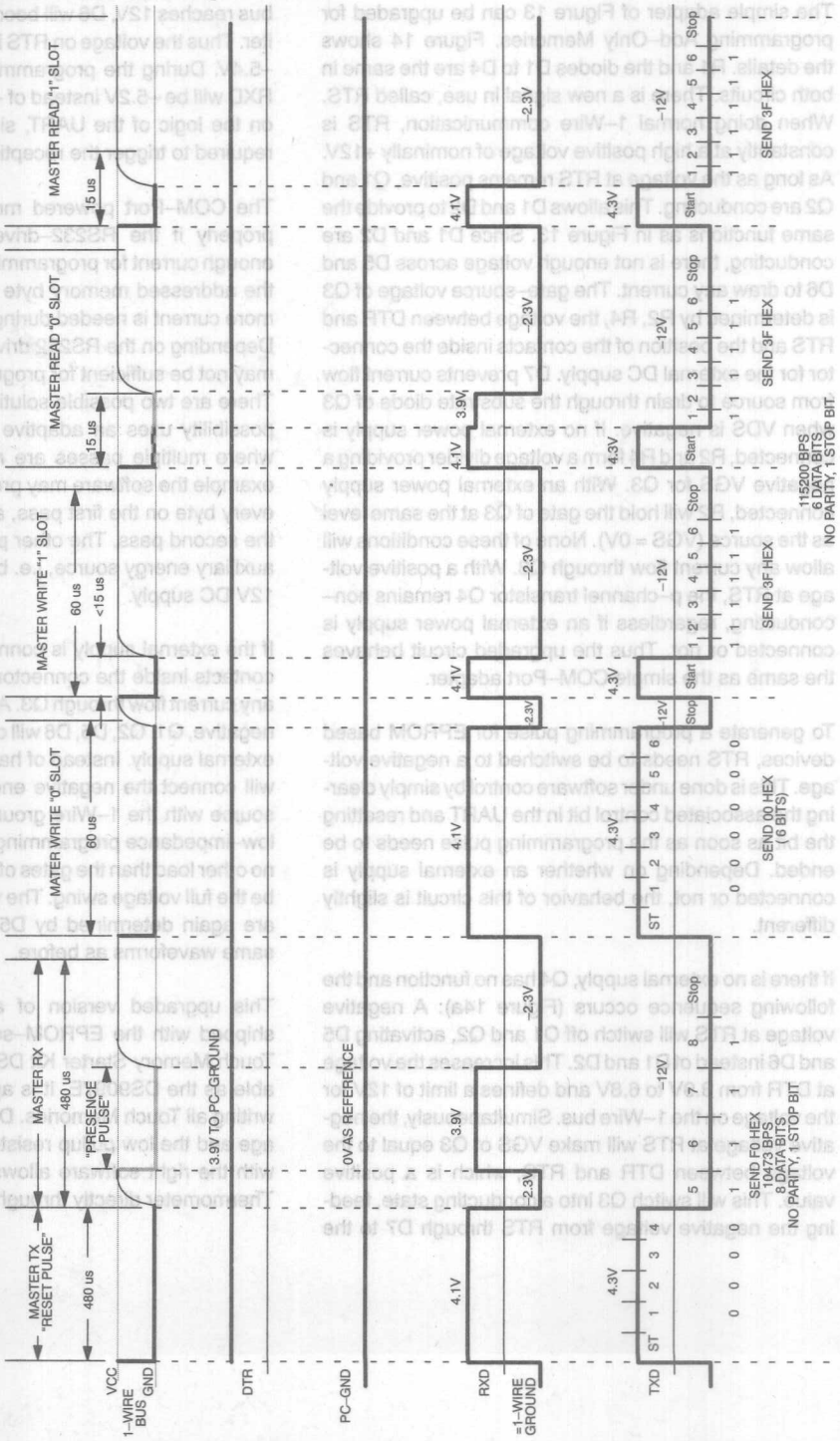
Fortunately, real RS232 receivers are more sensitive to a weak positive voltage than they are to a poor negative voltage. Although it is not completely within the specification of RS232, this interface with the components specified on Figure 13 has proven to be reliable with most desktop personal computers. Small computers, especially battery powered models, might not have the required current capability to run this interface. In case of difficulties, one should use the 5V RS232 interface instead.

This interface is shipped with the Touch Memory Starter Kit DS9092K and is also sold separately as COM Port Adapter DS9097. It is applicable for reading all Touch Memories and writing to SRAM–based devices. Due to the high pullup voltage and the low pullup resistor, this interface together with the right software also allows operation of the Touch Thermometer directly through the COM Port. Software to operate this interface is explained later in this document.

12V RS232 READ ALL CIRCUIT Figure 13



12V RS232 READ ALL WAVEFORMS Figure 13a



B. R/W all

The simple adapter of Figure 13 can be upgraded for programming Add–Only Memories. Figure 14 shows the details. R1 and the diodes D1 to D4 are the same in both circuits. There is a new signal in use, called RTS. When doing normal 1–Wire communication, RTS is constantly at a high positive voltage of nominally +12V. As long as the voltage at RTS remains positive, Q1 and Q2 are conducting. This allows D1 and D2 to provide the same functions as in Figure 13. Since D1 and D2 are conducting, there is not enough voltage across D5 and D6 to draw any current. The gate–source voltage of Q3 is determined by R2, R4, the voltage between DTR and RTS and the position of the contacts inside the connector for the external DC supply. D7 prevents current flow from source to drain through the substrate diode of Q3 when VDS is negative. If no external power supply is connected, R2 and R4 form a voltage divider providing a negative VGS for Q3. With an external power supply connected, R2 will hold the gate of Q3 at the same level as the source (VGS = 0V). None of these conditions will allow any current flow through Q3. With a positive voltage at RTS, the p–channel transistor Q4 remains non–conducting, regardless if an external power supply is connected or not. Thus the upgraded circuit behaves the same as the simple COM–Port adapter.

To generate a programming pulse for EPROM based devices, RTS needs to be switched to a negative voltage. This is done under software control by simply clearing the associated control bit in the UART and resetting the bit as soon as the programming pulse needs to be ended. Depending on whether an external supply is connected or not, the behavior of this circuit is slightly different.

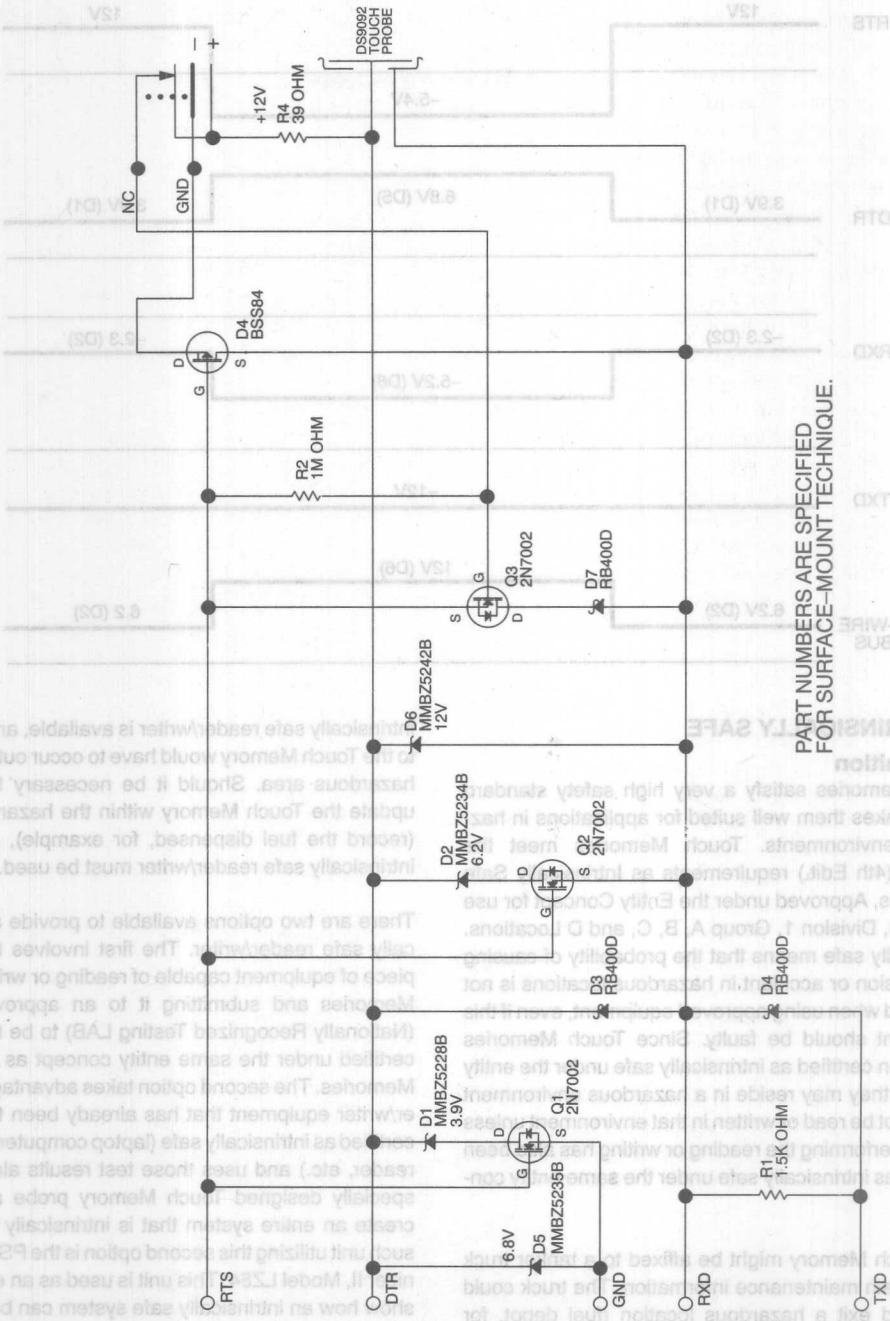
If there is no external supply, Q4 has no function and the following sequence occurs (Figure 14a): A negative voltage at RTS will switch off Q1 and Q2, activating D5 and D6 instead of D1 and D2. This increases the voltage at DTR from 3.9V to 6.8V and defines a limit of 12V for the voltage on the 1–Wire bus. Simultaneously, the negative voltage at RTS will make VGS of Q3 equal to the voltage between DTR and RTS, which is a positive value. This will switch Q3 into a conducting state, feeding the negative voltage from RTS through D7 to the 1–Wire ground. As soon as the voltage on the 1–Wire bus reaches 12V, D6 will become active as voltage limiter. Thus the voltage on RTS is limited to approximately –5.4V. During the programming pulse, the voltage at RXD will be –5.2V instead of –2.3V. This has no impact on the logic of the UART, since a positive voltage is required to trigger the reception of a character.

The COM–Port powered mode of this circuit works properly if the RS232–drivers are able to provide enough current for programming. If more than one bit of the addressed memory byte need to be altered, then more current is needed during the programming pulse. Depending on the RS232 drivers, the available energy may not be sufficient for programming all bits of a byte. There are two possible solutions to this problem. One possibility uses an adaptive programming algorithm, where multiple passes are made for each byte. For example the software may program the first four bits of every byte on the first pass, and the remaining bits on the second pass. The other possibility is to provide an auxiliary energy source, i.e. by connecting an external 12V DC supply.

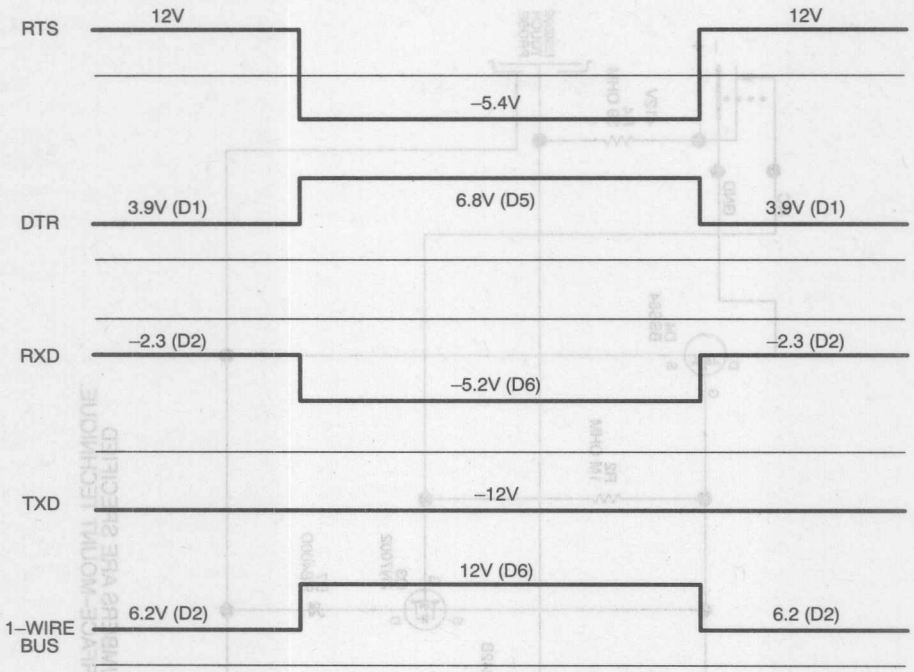
If the external supply is connected and operating, the contacts inside the connector will open. This prevents any current flow through Q3. As the voltage at RTS goes negative, Q1, Q2, D5, D6 will do the same as without the external supply. Instead of having no function, Q4 now will connect the negative end of the external voltage source with the 1–Wire ground, providing the desired low–impedance programming voltage. Since RTS has no other load than the gates of four transistors, there will be the full voltage swing. The voltages at RXD and TXD are again determined by D5 and D6 and exhibit the same waveforms as before.

This upgraded version of a COM–Port adapter is shipped with the EPROM–supporting revision of the Touch Memory Starter Kit DS9092K and is also available as the DS9097E. It is applicable for reading and writing all Touch Memories. Due to the high pullup voltage and the low pullup resistor, this interface together with the right software allows operation of the Touch Thermometer directly through the COM Port.

12V RS232 R/W ALL CIRCUIT Figure 14



12V RS232 R/W ALL PROGRAMMING WAVEFORMS Figure 14a



VI. INTRINSICALLY SAFE

A. Definition

Touch Memories satisfy a very high safety standard which makes them well suited for applications in hazardous environments. Touch Memories meet the UL#913 (4th Edit.) requirements as Intrinsically Safe Apparatus, Approved under the Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations. Intrinsically safe means that the probability of causing an explosion or accident in hazardous locations is not increased when using approved equipment, even if this equipment should be faulty. Since Touch Memories have been certified as intrinsically safe under the entity concept, they may reside in a hazardous environment but cannot be read or written in that environment unless the unit performing the reading or writing has also been certified as intrinsically safe under the same entity concept.

The Touch Memory might be affixed to a tanker truck and contain maintenance information. The truck could enter and exit a hazardous location (fuel depot, for example) without concern over an increased potential for an explosion due to the Touch Memory device. If no intrinsically safe reader/writer is available, any updates to the Touch Memory would have to occur outside of the hazardous area. Should it be necessary to read or update the Touch Memory within the hazardous area (record the fuel dispensed, for example), a certified intrinsically safe reader/writer must be used.

There are two options available to provide an intrinsically safe reader/writer. The first involves taking any piece of equipment capable of reading or writing Touch Memories and submitting it to an approved NRTL (Nationally Recognized Testing LAB) to be tested and certified under the same entity concept as the Touch Memories. The second option takes advantage of reader/writer equipment that has already been tested and certified as intrinsically safe (laptop computer, handheld reader, etc.) and uses those test results along with a specially designed Touch Memory probe adapter to create an entire system that is intrinsically safe. One such unit utilizing this second option is the PSION Organizer II, Model LZ64. This unit is used as an example to show how an intrinsically safe system can be realized.

B. Example of an Intrinsically Safe System

To use the LZ64 as an intrinsically safe Touch Memory Reader/Writer, an adapter is required. This adapter limits voltages and currents to safe values in the event a fault occurs. In the case of a fault, due to its internal construction, a maximum voltage of 17.22V at the 16–pin connector of the LZ64 may occur allowing a current of up to 1.55A. The adapter discussed here limits these values at the Touch Probe to a maximum voltage of 15V and a maximum current of 10mA (Values required by the Touch Memories in order to be certified as intrinsically safe.) These values together with the maximum inductance of 18 μH and maximum capacitance of 0.2nF of a Touch Memory fulfill the requirements for a complete system that is intrinsically safe according to UL specifications.

Figure 15 shows the complete circuit of the adapter. Essential components are the four current shunts Q1/R1 to Q4/R4, three Zener diodes D2 to D4 and one self–resetting fuse SS1. The Schottky diode D1 is optional. It protects Touch Memories by suppressing negative undershoots on the 1–Wire bus.

If by fault the LZ64 presents up to 17.22V at its connector and there is an open circuit at the Touch Probe, then the 12V Zener diodes D2 to D4 will limit the voltage at the Touch Probe to a value well below 15V. The intrinsically–safe regulations demand that this limitation will work correctly even if two of the protecting devices should fail. Therefore three Zener diodes are provided instead of one. If a Zener diode fails, it will either represent a short or it will be non–conducting. In either case, the voltage at the Touch Probe is limited to a safe value.

If by fault the LZ64 presents up to 17.22V at its connector and there is a short at the Touch Probe, then a current will flow through the resistors R1 to R4. The voltage drop across these resistors acts to turn on their respective transistors and causes base currents to flow. These base currents multiplied by the current gain of the transistors will direct most of the current to ground and limit the current at the Touch Probe to less than 10mA. Q1 will sink most of the current. Two of these Q/R stages are required to limit the current available at the Touch Probe under worst case conditions to less than 10mA. The other two current shunts are redundant since again the circuit must operate correctly with up to two faults. The self–resetting fuse with a trip point below 100mA will open in less than one second and thus prevent thermal damage to the transistors. It will also serve as an indicator to the operator that a fault or malfunction has occurred.

Although this adapter is designed for use with the LZ64, it can be used with similar intrinsically safe equipment with the same or lower faulted open–circuit voltage or short–circuit current to form a Touch Reader/Writer. This adapter does not impede writing to EPROM based Touch Memories.

VII. COMMENTED SOFTWARE

A. Software Architectural Model

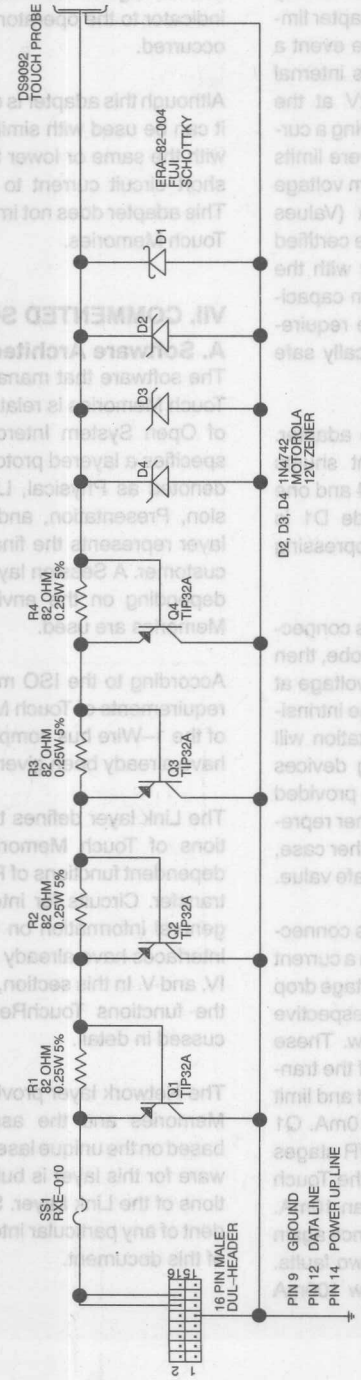
The software that manages data transfer to and from Touch Memories is related to the ISO reference model of Open System Interconnection (OSI). This model specifies a layered protocol having up to seven layers, denoted as Physical, Link, Network, Transport, Session, Presentation, and Application. The Application layer represents the final application designed by the customer. A Session layer may or may not be needed, depending on the environment in which the Touch Memories are used.

According to the ISO model, the electrical and timing requirements of Touch Memory and the characteristics of the 1–Wire bus comprise the Physical layer. Details have already been given in section II of this document.

The Link layer defines the basic communication functions of Touch Memories, which are the hardware dependent functions of Reset, Presence Detect and bit transfer. Circuits for interfacing Touch Memories and general information on the software to operate these interfaces have already been presented in sections III, IV, and V. In this section, the software itself, specifically the functions TouchReset and TouchByte, are discussed in detail.

The Network layer provides the identification of Touch Memories and the associated network capabilities based on the unique lasered identification number. Software for this layer is built up using the low–level functions of the Link Layer. Since this software is independent of any particular interface, it is not within the scope of this document.

INTRINSICALLy SAFE ADAPTER (EXAMPLE) Figure 15



The Transport layer is responsible for the data transfer between the non–ROM segments of Touch Memories and the master, and the data transfer from the scratchpad to the final storage areas and special registers of the Touch Memory. Due to their EPROM technology, Add–Only Memories require special attention for writing data. The Touch Thermometer may require special hardware together with appropriate software to do a temperature measurement. To comply these devices, the hardware specific function PulWidth has been provided on the Transport layer. Details are given in this chapter. All other software of the transport layer is independent of the type of interface, and therefore is not discussed here.

The layers Link, Network, and Transport are the foundations of the Presentation layer. This layer provides a DOS–like file system supporting functions like Format, Directory, Type, Copy, Delete, Optimize, and integrity check. Since the Presentation layer itself is based on software of the lower layers, its software is independent of any particular interface. Full details of the Presentation layer are given in the Touch Memory EXecutive DS0620. For software examples beyond the hardware dependent functions TouchReset, TouchByte and PulWidth, please refer to the "Book of DS19xx Touch Memory Standards" and the Touch Memory Starter Kit DS9092K.

A matrix that indicates which software of this section matches with which hardware is given in Table 3. For the 5V TTL type interface, assembly language code for the 8051 has been provided. For the group of interfaces based on the UART 8250, code examples in Pascal and C are included. This particular software has been adapted to and verified with IBM–compatible PCs employing a 8253 timer at 2.3863633 MHz and running under DOS. The timing is practically independent of the CPU clock rate. Under WINDOWS there is a lot more software being executed around an application program. This overhead introduces a significant influence from the CPU clock rate to the desired timing with the function PulWidth. The functions TouchReset and TouchByte are timed by the UART only and therefore are independent of the operating system.

SOFTWARE/HARDWARE MATRIX Table 3

LANGUAGE	8051 ASM	PASCAL AND C
TIMING	**CPU CRYSTAL**	**8250 UART (1.8 MHz) and 8253 TIMER (2.4 MHz)**
Electric Type	**5V TTL**	**5V RS232, 12V RS232**
SRAM R/W EPROM Read	TouchReset, TouchByte 1.8 or 11 MHz	TouchReset and TouchByte Pascal or C–Language
EPROM Write	0.5 ms pulsewidth: PULWIDTH(1) at 1.8 MHz PULWIDTH(6) at 11 MHz	0.5 ms pulsewidth: PULWIDTH(1193) under DOS

B. TTL–Interface R/W all

As a representative for all microprocessor timed 1–Wire interfaces the industry–standard 8051 microcontroller has been chosen. The following pages show two versions of assembly language code to provide the functions TouchReset and TouchByte. The first example is written for an 11.0592 MHz crystal, the second one for 1.8432 MHz. The higher frequency is very common since it supports all standard baud rates with the highest accuracy. The lower frequency is the lowest that can comply with the 1–Wire timing. The port to be used as 1–Wire bus is defined in the parameter DATA_BIT. Parameter passing from the subroutines TouchReset and TouchByte is very simple: If a Touch Memory is present on the 1–Wire bus, TouchReset will return a set carry flag; otherwise carry is cleared. To send one byte to the 1–Wire bus, the byte to be sent is loaded into the accumulator before calling TouchByte. If one intends to read, the accumulator is loaded with FFH. This generates correct Read Data Time Slots and returns data from the 1–Wire bus to the calling program through the accumulator. These conventions are valid for both versions of TouchReset and TouchByte.

The procedure to generate a programming pulse is the same for both clock frequencies. It generates a 0.5 ms

LOW pulse at the port named PROGRAM. If the clock frequency is 1.8 MHz, then the accumulator needs to be loaded with 1 before calling this procedure. For a clock frequency of 11 MHz the value of 6 loaded into the accumulator will generate a pulse of the same duration. Software considering the Touch Thermometer will be published as soon as the device is available. Generally, it is not a difficult task to adapt the procedure PulWidth to a pulsewidth of 2 seconds.

8051 ASSEMBLY LANGUAGE, 11.0592 MHZ

```
DATA_BIT  BIT       P0.0

; The following 8051 code uses a bi-directional port pin (specified by
; DATA_BIT) for 1-wire I/O. This code was written for an 11.0592 MHz
; crystal.
;
;         Procedure TouchReset
;
;         This procedure transmits the Reset signal to the Touch
;         Memory and watches for a presence pulse. On return,
;         the Carry bit is set if a presence pulse was detected,
;         otherwise the Carry is cleared. The code is timed for
;         an 11.0592 MHz crystal.
;
TOUCHRESET:
          PUSH      B                    ;       Save the B register.
          PUSH      ACC                  ;       Save the accumulator.
          MOV       A,        #4         ;       Load outer loop variable.
          CLR       DATA_BIT             ;       Start the reset pulse.
          MOV       B,        #221       ;   2.  Set time interval.
          DJNZ      B,        $          ; 442.  Wait with Data low.
          SETB      DATA_BIT             ;   1.  Release Data line.
          MOV       B,        #6         ;   2.  Set time interval.
          CLR       C                    ;   1.  Clear presence flag.
WAITLOW:
          JB        DATA_BIT, WH         ;       Exit loop if line high.
          DJNZ      B,        WAITLOW    ;       Hang around for 3360
          DJNZ      ACC,      WAITLOW    ;          us if line is low.
          SJMP      SHORT                ;       Line could not go high.
WH:
          MOV       B,        #111       ;       Delay for presence detect.
HL:
          ORL       C,        /DATA_BIT  ; 222.  Catch presence pulse.
          DJNZ      B,        HL         ; 222.  Wait with Data high.
SHORT:
          POP       ACC                  ;       Restore accumulator.
          POP       B                    ;       Restore B register.
          RET                            ;       Return.
;
;         Procedure TouchByte
;
;         The procedure TouchByte sends the byte in the accumulator
;         to the Touch Memory and simulatneously returns one
;         byte from the Touch Memory in the accumulator. Note that
```

```
;         the NOPs in the following code are intended to give the
;         optimum performance when using a 11.0592 MHz crystal.
;         Their purpose is to make the pulses as long as
;         possible consistent with the Touch Memory timing
;         constraints. When using other crystal frequencies,
;         the delays in this code should be adjusted to conform
;         to the timing requirements of the Touch Memory.
;
TOUCHBYTE:
          PUSH    B                 ;       Save the B register.
          MOV     B,#8              ;       Setup for 8 bits.
BIT_LOOP:
          RRC     A                 ;   1.  Get bit in carry.
          CALL    TOUCHBIT          ;   2.  Send bit.
          DJNZ    B, BIT_LOOP       ;   2.  Get next bit.
          RRC     A                 ;       Get final bit in ACC.
          POP     B                 ;       Restore B register.
          RET                       ;       Return to caller.
TOUCHBIT:
          CLR     DATA_BIT          ;   1.  Start the time slot.
          NOP                       ;   1.  Delay to make sure
          NOP                       ;   1.    that the Touch Memory
          NOP                       ;   1.      sees a low for at
          NOP                       ;   1.        least 1 microsecond.
          MOV     DATA_BIT, C       ;   2.  Send out the data bit.
          NOP                       ;   1.  Delay to give the
          NOP                       ;   1.    data returned from
          NOP                       ;   1.      the Touch Memory
          NOP                       ;   1.        time to settle
          NOP                       ;   1.          before reading
          NOP                       ;   1.            the bit.
          MOV     C,      DATA_BIT  ;   1.  Sample input data bit.
          PUSH    B                 ;   2.  Save B register.
          MOV     B,#12H            ;   2.  Delay until the end
          DJNZ    B,$               ;   36.   of the time slot.
          POP     B                 ;       Restore B register.
          SETB    DATA_BIT          ;       Terminate time slot.
          RET                       ;       Return to caller.
;
          END                       ; End of module.
```

8051 ASSEMBLY LANGUAGE, 1.8432 MHZ

```
;         Touch Memory I/O Procedures for use with a 1.8432 MHz crystal.

TOUCHRESET:
          CLR     DATA_BIT          ;   - Pull the data line low.
          MOV     B,      #35       ;   2 Hold the data line
          DJNZ    B,      $         ;  70   low for 481.77
          NOP                       ;   1     microseconds.
          SETB    DATA_BIT          ;   1 Release the data line.
```

```
          MOV       B,      #130      ;   2 Short circuit timeout.
          CLR       C                 ;   1 Presence pulse detector.
WAITLOW:
          JB        DATA_BIT, WAITHIGH ;  260 Go look for Presence pulse.
          DJNZ      B,      WAITLOW   ;  260 Abort on short circuit.
          SJMP      ABORT             ;    Short circuit (3.8877 ms).
WAITHIGH:
          MOV       B,      #18       ;   2 Prepare for high period.
HL:
          ORL       C,      /DATA_BIT ;   36 Trap the Presence pulse.
          DJNZ      B,      HL        ;   36 Wait out 481.77 microsec.
ABORT:
          RET                         ;      Return.
TOUCHBYTE:
          MOV       B,      #8        ;    Prepare to move 8 bits.
BIT_LOOP:
          RRC       A                 ;    Move LSB to Carry.
          JC        SENDONE           ;    If Carry then send 1.
          CLR       DATA_BIT          ;    Otherwise send 0.
          SJMP      DELAYSET          ;   2 Wait out rest of time slot.
SENDONE:
          CLR       DATA_BIT          ;    Start read/write 1 slot.
          SETB      DATA_BIT          ;   1 Set data line.
          MOV       C,      DATA_BIT  ;   1 Read data line.
DELAYSET:
          NOP                         ;   1 Delay 7 more cycles
          NOP                         ;   1    to produce enough
          NOP                         ;   1       delay to complete
          NOP                         ;   1          the time slot.
          NOP                         ;   1
          NOP                         ;   1
          NOP                         ;   1
          SETB      DATA_BIT          ;   1 Done (65.1 microseconds).
          DJNZ      B,      BIT_LOOP  ;    Repeat to send 8 bits.
          RRC       A                 ;    Align final result.
          RET                         ;    Return.
```

8051 ASSEMBLY LANGUAGE PULSEWIDTH (1.8432 AND 11.0592 MHZ)

```
PROGRAM   BIT       Pn.i
;
;         This procedure generates a 0.5 ms low pulse on port
;         Pn.i of an 8051 microprocessor, where 0 <= n <= 3
;         and 0 <= i <= 7.  The frequency of the crystal, in
;         multiples of the minimum frequency 1.8432 MHz, must
;         be passed in the accumulator.
;
PULWIDTH:
          MOV       B,      #38     ; Number of loops at 1.8432 MHz.
          MUL       AB                ; AB = # of loops given frequency.
          INC       B                 ; Adjust count value for
```

```
                                    ;     use with DJNZ instruction.
        PUSH    PSW                 ; Preserve state of interrupts.
        CLR     EA                  ; Inhibit all interrupts.
        CLR     PROGRAM             ; Bring the port pin low.
LOOP:
        DJNZ    ACC,    LOOP        ; Count while
        DJNZ    B,      LOOP        ;    pin is low.
        SETB    PROGRAM             ; Bring the port pin high.
        POP     PSW                 ; Restore state of interrupts.
        RET                         ; Return.
```

C. RS232 Interface R/W all

UARTs like the 8250 can be connected to any microprocessor to implement a RS232 type interface. The software to operate the UART mainly consists of reading and writing the UART's internal registers (Figure 8). This can easily be done in any high level language. Depending on the computer, the physical address of the UART will be different, but the crystal will usually be a 1.8432 MHz type. Not regarding the UART's physical address, the software examples for TouchReset and TouchByte given on the following pages are very general. The languages C and Pascal are very common and a variety of compilers is available.

Unfortunately, the UART does not control the timing of the signals DTR and RTS. It only allows activation or deactivation of these signals by setting or clearing bits inside its control registers. The timing itself is left to the microprocessor and its peripheral timing circuits. From the software developer's point of view this is a step backwards to assembly language, where every command and its execution time at a specified clock frequency need to be counted. For this reason it is not possible to provide machine–independent software to generate the programming pulse.

The most common computer using a 8250 type UART to implement a RS232 interface is the IBM–compatible PC. These machines employ a programmable interval timer 8253 running at 2.3863633 MHz for general timing purposes. This timer is involved in controlling the timing of the software examples of PulWidth. The pulsewidth is specified by a formal parameter passed to PulWidth. For 0.5 ms the value of this parameter is 1193 decimal. Under DOS, the software examples given below will perform accurately and almost independent of the CPU clock. Due to a very different environment and use of resources under WINDOWS, the pulses will be longer and also dependent on the CPU clock. This can be compensated for experimentally by reducing the value of the parameter passed to PulWidth. Software considering the Touch Thermometer will be published as soon as the device is available. For the 5V–type RS232 interface a pulsewidth of 2 seconds will be required for the strong pullup to 5V. The 12V RS232 interface has enough power available to run one Touch Thermometer without extra power switching.

C LANGUAGE FOR UART 8250 SYSTEMS

```
/*
   In the following C language code, 1–wire I/O is accomplished using the
   serial port of an IBM PC or compatible. The serial port must be capable
   of a 115,200 bps data rate. Setup must be called before any of the
   touch functions to verify the existence of the specified com port and
   initialize it.

   ---------------------------------------------------------------------

   The setup function makes sure that the com port number passed to it
   is from 1 to 4 and has a valid address associated with it.
*/
uchar Setup(uchar CmPt)
{
```

```
    uint far *ptr = (uint far *) 0x00400000;
    uint SPA;

    /* check to see if it is a valid com port number and address */
    SPA = *(ptr+CmPt-1); /* get the address */
    if (CmPt < 1 || CmPt > 4 || !SPA )
       return FL;

    /* serial port initialization */
    outportb(SPA+3,0x83);  /* set DLAB */
    outportb(SPA  ,0x01);  /* bit rate is 115200 */
    outportb(SPA+1,0x00);
    outportb(SPA+3,0x03);  /* 8 dta, 1 stp, no par */
    outportb(SPA+1,0x00);  /* no interrupts */
    outportb(SPA+4,0x03);  /* RTS and DTR on */

    return TR;
}
/*-----------------------------------------------------------------------
 * Do a reset on the 1 wire port and return  0 no presence detect
 *                                           1 presence pulse no alarm
 *                                           2 alarm followed by presence
 *                                           3 short circuit to ground
 *                                           4 no com port found
 *
 * The global variable 'com_port' must be set to the com port that the
 * DS9097 COM Port Adapter is attached to before calling this routine.
 *
 */
uchar TouchReset( void )
{
    uint SPA,F,X,Y,tmp,trst=0;
    uint far *ptr = (uint far *) 0x00400000;
    ulong far *sysclk = (ulong far *) 0x0040006c;
    ulong M;

    /* get the serial port address */
    SPA = *(ptr+com_port-1);

    /* return if there is no address */
    if (!SPA) return 4;

    /* serial port initialization */
    outportb(SPA+3,0x83);  /* set DLAB */
    outportb(SPA  ,0x01);  /* bit rate is 115200 */
    outportb(SPA+1,0x00);
    outportb(SPA+3,0x03);  /* 8 dta, 1 stp, no par */
    outportb(SPA+1,0x00);  /* no interrupts */
    outportb(SPA+4,0x03);  /* RTS and DTR on */
```

```
/* Initialize the time limit */
M = *sysclk +1;

/* loop to clear the buffers */
do { tmp = inportb(SPA+5) & 0x60;  } while (tmp != 0x60);

/* flush input */
while (inportb(SPA+5) & 0x1) X = inportb(SPA);

outportb(SPA+3,0x83);  /* set DLAB */
outportb(SPA+1,0x00);  /* baud rate is 10473 */
outportb(SPA  ,0x0B);
outportb(SPA+3,0x03);  /* 8 dta, 1 stp, no par */
outportb(SPA  ,0xF0);  /* send the reset pulse */

/* wait until character back or timeout */
do
{
     Y = inportb(SPA+5);
     F = Y & 0x1;
} while ( !F && (*sysclk <= M) );

if (F) X = inportb(SPA);
else   return 3;

if (X != 0xF0)           /* if more bits back than sent then there */
{                        /* is a device  if framing error or break */
     trst = TR;
     if ( (Y & 0x18) != 0 )
     {
          trst = 2;

          /* loop to clear the buffers */
          do { tmp = inportb(SPA+5) & 0x60;  } while (tmp != 0x60);

          /* wait until character back or timeout */
          do
          {
               Y = inportb(SPA+5);
               F = Y & 0x1;
          } while ( !F && (*sysclk <= M) );

          if (F) X = inportb(SPA);
          else return 3;
     }
}

outportb(SPA+3,0x83);  /* set DLAB */
outportb(SPA  ,0x01);  /* bit rate is 115200 */
outportb(SPA+3,0x03);  /* 8 dta, 1 stp, no par */
```

```
    return trst;
}

/*-------------------------------------------------------------------
 * This is the 1-Wire routine 'TouchByte', sometimes called 'DataByte'.
 * It transmits 8 bits onto the 1-Wire data line and receives 8 bits
 * concurrently. The global variable 'com_port' must be set to the
 * com port that the serial brick is attached to before calling this
 * routine. This com port must also be set to 115200 baud, 8 dta, 1 stp,
 * and no parity. This routine returns the uchar 8 bit value received.
 * If it times out waiting for a character then 0xFF is returned.
 */
uchar TouchByte(uchar outch)
{
    uchar inch=0,sendbit,Mask=1;
    uint SPA;
    uint far *ptr = (uint far *) 0x00400000;
    ulong far *sysclk = (ulong far *) 0x0040006c;
    ulong M;

    /* get the serial port address */
    SPA = *(ptr+com_port-1);

    /* Initialize the time limit */
    M = *sysclk +2;

    /* wait to TBE and TSRE */
    do {} while ( (inportb(SPA+5) & 0x60) != 0x60 );

    /* flush input */
    while ( (inportb(SPA+5) & 0x1) )
        inportb(SPA);

    /* get first bit ready to go out */
    sendbit = (outch & 0x1) ? 0xFF : 0x00;

    /* loop to send and receive 8 bits */
    do
    {
        outportb(SPA,sendbit);  /* send out the bit */

        /* get next bit ready to go out */
        Mask <<= 1;
        sendbit = (outch & Mask) ? 0xFF : 0x00;

        /* shift input char over ready for next bit */
        inch >>= 1;

        /* loop to look for the incoming bit */
        for (;;)
        {
            /* return if out of time */
```

```
            if ( *sysclk > M )
               return 0xFF;
            if ( inportb(SPA+5) & 0x01 )
            {
               inch |= ((inportb(SPA) & 0x01) ? 0x80 : 0x00);
               break;
            }
         }

   } while (Mask);

   return inch;   /* return the input char */
}
```

C LANGUAGE PULSEWIDTH FOR SYSTEMS USING 8253 AND 8250

```
// standard include header file
#include <dos.h>

// function prototype
void PulWidth(unsigned int);

// global variable
int SPA;

//-------------------------------------------------------------------------
//  This procedure creates a fixed pulse width for programming that is
//  approximately independent of system clock speed.  X is in units of
//  0.419 microseconds for values greater than about 1000.
//
void PulWidth(unsigned int X)
{
   unsigned int N,M;

   disable();                                  // turn off interrupts
   outportb(SPA+4,(inportb(SPA+4) & 0xFD));    // apply program pulse to rts
   outportb(0x43,0);                           // freeze value in timer
   M = inportb(0x40);                          // read value in timer
   M |= (inportb(0x40) << 8);
   do
   {
      outport(0x43,0);                         // freese value in timer
      N = inportb(0x40);                       // read value in timer
      N |= (inportb(0x40) << 8);
   }
   while (X > (M - N));

   outportb(SPA+4,(inportb(SPA+4) | 0x02));    // remove program Voltage
   enable();                                   // turn interrupts on
}
```

PASCAL LANGUAGE FOR UART 8250 SYSTEMS

```
{
   In the following pascal code 1-wire I/O is accomplished using the
   serial port of an IBM PC or compatible. The serial port must be capable
   of a 115,200 bps data rate.
}
Const
   SPA : Word = 0;            { Currently active serial port address }

Function TouchReset(N: Byte): Boolean;
{
   This function transmits the one-wire protocol reset sequence to
   the device connected to COM port number N. This sequence consists
   of a low pulse lasting a mimimum of 480 us followed by a high dead
   time lasting a mimimum of 480 us. The function returns True if a
   presence detect pulse occurs during the dead time, otherwise
   it returns False.
}
Const
   Init : Array[1..4] of Boolean = (True, True, True, True);

Var
   S : Array[1..4] of Word Absolute $40:0;
   T : LongInt Absolute $40:$6C;
   M : LongInt;
   F : Boolean;
   X, Y : Byte;

Begin
   SPA := 0; TouchReset := False;                    { Assume failure }
   If (N > 0) and (N < 5) and (S[N] > 0) then Begin  { Legal port # }
      SPA := S[N];                  { Save active serial port address }
      If Init[N] then Begin   { Serial port requires initialization }
         Port[SPA +3] := $83;                          { Set the DLAB }
         Port[SPA]     :=   1;                         { Bit rate is   }
         Port[SPA +1] :=   0;                          {    115200 bps }
         Port[SPA +3] :=   3;                  { 8 dta, 1 stp, no par }
         Port[SPA +1] :=   0;                          { No interrupts }
         Port[SPA +4] :=   3;                         { RTS and DTR on }
         Init[N] := False;                { Initialization completed }
      End;
      M := T +1;                           { Initialize the time limit }
      Repeat until Port[SPA +5] and $60 = $60;  { Await TBE & TSRE }
      While Odd(Port[SPA +5]) do X := Port[SPA];     { Flush input }
      Port[SPA +3] := $83;                                { Set DLAB }
      port[SPA+1] := 0;                           { Baud rate is 10473 }
      Port[SPA] := 11;
      Port[SPA +3] := 3;                  { 8 data, 1 stop, no parity }
      Port[SPA] := $F0;                          { Send the reset pulse }
      Repeat                { Wait until character back or timeout }
         Y := Port[SPA +5];
         F := Odd(Y);
```

```
      until F or (T > M);
      If F then X := Port[SPA] else X := $F0;
      If (X <> $F0) Then Begin          { If more bits back than sent }
         TouchReset := True;                { then there is a device }
         If ((Y and $18) <> 0) Then Begin { Framing error or break }
            Repeat until Port[SPA +5] and $60 = $60; { TBE & TSRE }
            Repeat F := Odd(Port[SPA +5]) until F or (T > M);
            If F then X := Port[SPA];
         End;
      End;
      Port[SPA +3] := $83;                        { Set the DLAB }
      Port[SPA]     :=   1;                 { Bit rate is 115200 bps }
      Port[SPA +3] :=   3;                   { 8 dta, 1 stp, no par }
   End;
End;

Function TouchByte(X: Byte): Byte;
{
   This function transmits the byte X to the device attached to the
   currently active serial port SPA, and returns a byte from the
   device as its value.
}
Var
   T    : LongInt Absolute $40:$6C;
   M    : LongInt;
   I, J : Byte;
Begin
   If SPA = 0 then TouchByte := X else Begin
      M := T +1;                        { Initialize the time limit }
      Repeat until Port[SPA +5] and $60 = $60; { Await TBE & TSRE }
      While Odd(Port[SPA +5]) do I := Port[SPA];     { Flush input }
      I := 0; J := 0;          { Initialize output & input bit counters }
      Repeat
         If Odd(Port[SPA +5]) then Begin
            Inc(J); If Odd(Port[SPA]) then X := X or $80;
         End else If (I<=J) and (Port[SPA+5] and $20 = $20) then Begin
            If Odd(X) then Port[SPA] := $FF else Port[SPA] := 0;
            X := X shr 1; Inc(I);
         End;
      Until (J = 8) or (T > M);
      While (J < 8) do Begin
         X := X shr 1 or $80;
         Inc(J)
      End;
      TouchByte := X;
   End;
End;
```

PASCAL LANGUAGE PULSEWIDTH FOR SYSTEMS USING 8253 AND 8250

```
Procedure PulWidth(X : Word);
{
   This procedure creates a fixed pulse width for programming
   that is approximately independent of system clock speed.  When
   used in an IBM PC or compatible computer operating under MS-
   DOS, X is in units of 0.419 microseconds for values of X
   greater than about 1000.  The procedure can be used with any
   processor having an 8250 UART I/O mapped to base port address
   SPA and an 8253 timer mapped to base port address $40,
   operating with an input clock of 2.386363 MHz and with its
   count limit set to the maximum value.
}
Var
   M, N : Word;
Begin
   Inline($FA);                                  {Turn off interrupts}
   Port[SPA +4] := Port[SPA +4] and $FD;      {Apply Program Pulse on RTS}
   Port[$43] := 0;                               {Freeze value in timer}
   M := Port[$40] shl 8 or Port[$40];            {Read value in timer}
   Repeat                                        {Loop to consume real time}
      Port[$43] := 0;                            {Freeze value in timer again}
      N := Port[$40] shl 8 or Port[$40];         {Read new value in timer}
   Until M - N >= X;                             {See if "X" usec have elapsed}
   Port[SPA +4] := Port[SPA +4] or 2;         {Remove Program Voltage}
   Inline($FB);                                  {Turn interrupts on}
End;
```

VIII. SUMMARY

This application note explains the hardware of different types of 1–Wire interfaces and software examples adapted to this hardware. Depending on the types of Touch Memories required for a project and the type of computer to be used, the most economic interface is easily found. The hardware examples shown are basically two different types: 5V general interface and 12V RS232 interface. Within the 5V group a common printed circuit board could be used for all four circuits. The variations can be achieved by different population of components (Table 4). The same principle is used for the 12V RS232 interface. The population determines if it is a Read all or a Read/Write all type of interface (Table 5).

There are other possible circuit implementations to create a 1–Wire interface. The circuits described in this application note cover many different configurations. For a custom application, one of the described options can be adapted to meet individual needs. The circuits can be used for reading and writing SRAM based Touch Memories, for individually programming EPROM based Touch Memories and for temperature measurement with the DS1920 Touch Thermometer. For programming large quantities of EPROM based Touch Memories with the same data (gang programming) commercial programmers are available from several independent companies. A list of vendors is available from Dallas Semiconductor on request.

PARTS LIST FOR 5V SERIAL TO 1–WIRE PORT ADAPTERS (FOUR OPTIONS) Table 4

POSITION	TTL READ ALL	5V RS232 RD ALL	TTL RW ALL	5V RS232 RW ALL
C1	empty	empty	10µ tantalum	10µ tantalum
C2	empty	empty	150p, ceramic	150p, ceramic
D1	1N5242 (12V)	1N5242 (12V)	1N5242 (12V)	1N5242 (12V)
D2	1N5232 (5.6V)	1N5232 (5.6V)	1N5242 (12V)	1N5242 (12V)
D3	empty	1N5232 (5.6V)	empty	1N5242 (12V) optional
D4	empty	empty	1N5242 (12V)	1N5242 (12V)
D5	empty	empty	ERA–82–004	ERA–82–004
D6	empty	empty	1N5818	1N5818
D7	short	short	empty	ERA–82–004 optional
IC1	empty	empty	LT1109CN8–12	LT1109CN8–12
Q1	2N7000	2N7000	2N7000	2N7000
Q2	short GD	2N7000	short GD	2N7000
Q3	empty	empty	2N7000	2N7000
Q4	empty	empty	2N7000	2N7000
Q5	empty	empty	BSS110	BSS110
R1	4.7 kΩ	4.7 kΩ	4.7 kΩ	4.7 kΩ
R2	empty	4.7 kΩ	empty	4.7 kΩ
R3	empty	empty	100 kΩ	100 kΩ
R4	empty	empty	100 kΩ	100 kΩ
R5	empty	empty	47 kΩ	47 kΩ
L1	empty	empty	see text	see text

PARTS LIST FOR 12V COM PORT TO 1–WIRE ADAPTERS (TWO OPTIONS) Table 5

POSITION	READ ALL	RW ALL
D1	empty	1N5228 (3.9V)
D2	empty	1N5234 (6.2V)
D3	ERA–82–004	ERA–82–004
D4	ERA–82–004	ERA–82–004
D5	1N5228 (3.9V)	1N5235 (6.8V)
D6	1N5234 (6.2V)	1N5242 (12V)
D7	empty	ERA–82–004
Q1	empty	2N7000
Q2	empty	2N7000
Q3	empty	2N7000
Q4	empty	BSS110
R1	1.5 kΩ	1.5 kΩ
R2	empty	1000 kΩ
R3	empty	empty
R4	empty	39 Ω

SOFTWARE PROTECTION: THREE–WIRE PRODUCTS

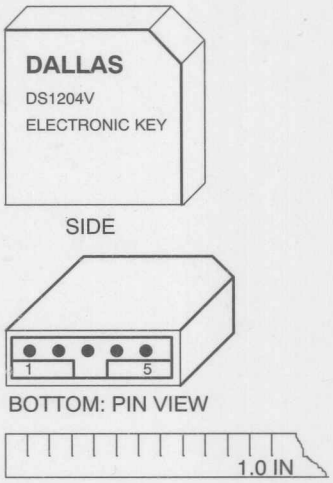
DALLAS SEMICONDUCTOR

DS1204V
Electronic Key

FEATURES

- Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit security match code virtually prevents deciphering by exhaustive search with over 10^{19} possibilities
- 128 bits of secure read/write memory create additional barriers by permitting data changes as often as needed
- Rapid erasure of identification security match code and secure read/write memory can occur if tampering is detected
- Low-power CMOS circuitry
- Four million bps data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN ASSIGNMENT



See Mech. Drawing – Pg. 350

PIN DESCRIPTION

Pin 1 - V_{CC}	+5 Volts
Pin 2 - $\overline{RST}$	Reset
Pin 3 - DQ	Data Input/Output
Pin 4 - CLK	Clock
Pin 5 - GND	Ground

DESCRIPTION

The DS1204V Electronic Key is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a procedure with a serial format to retrieve or update data. Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), Reset ($\overline{RST}$), and Data Input/Output (DQ).

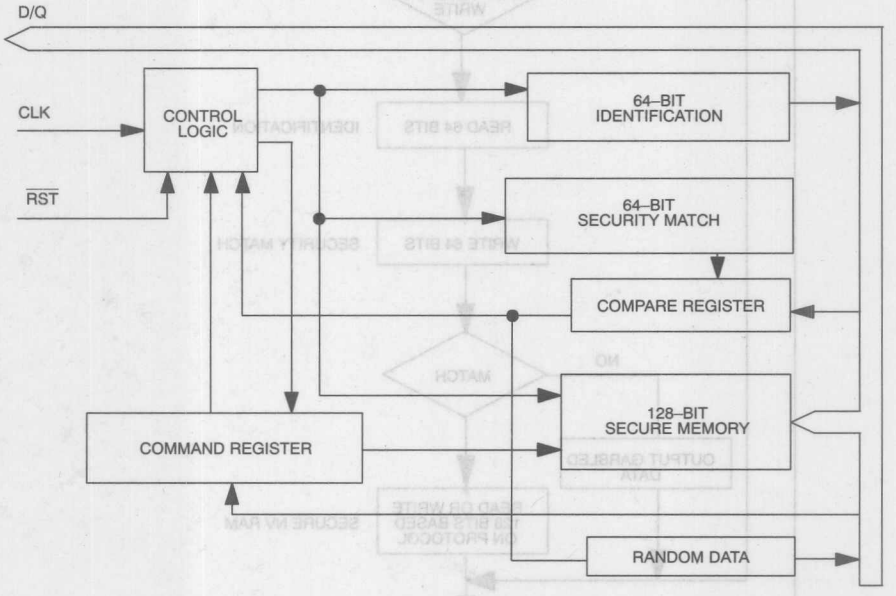
Low pin count and a guided entry for mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

OPERATION - NORMAL MODE

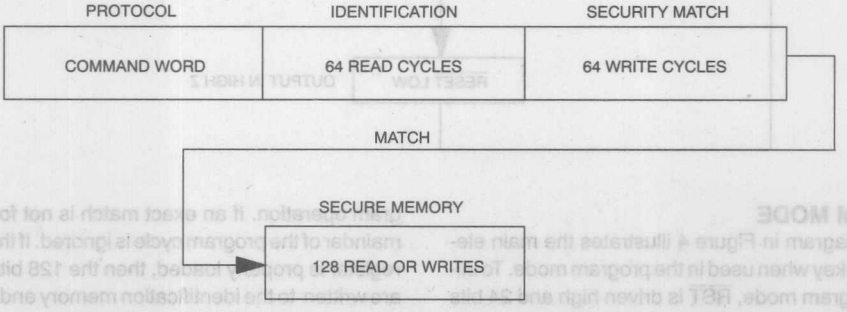
The Electronic Key has two modes of operation: normal and program. The block diagram (see Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, $\overline{RST}$ is taken high and 24 bits are loaded into the command

register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines normal operation for read or write, or communications are ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are reads. Data is clocked out of the key on the high-to-low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

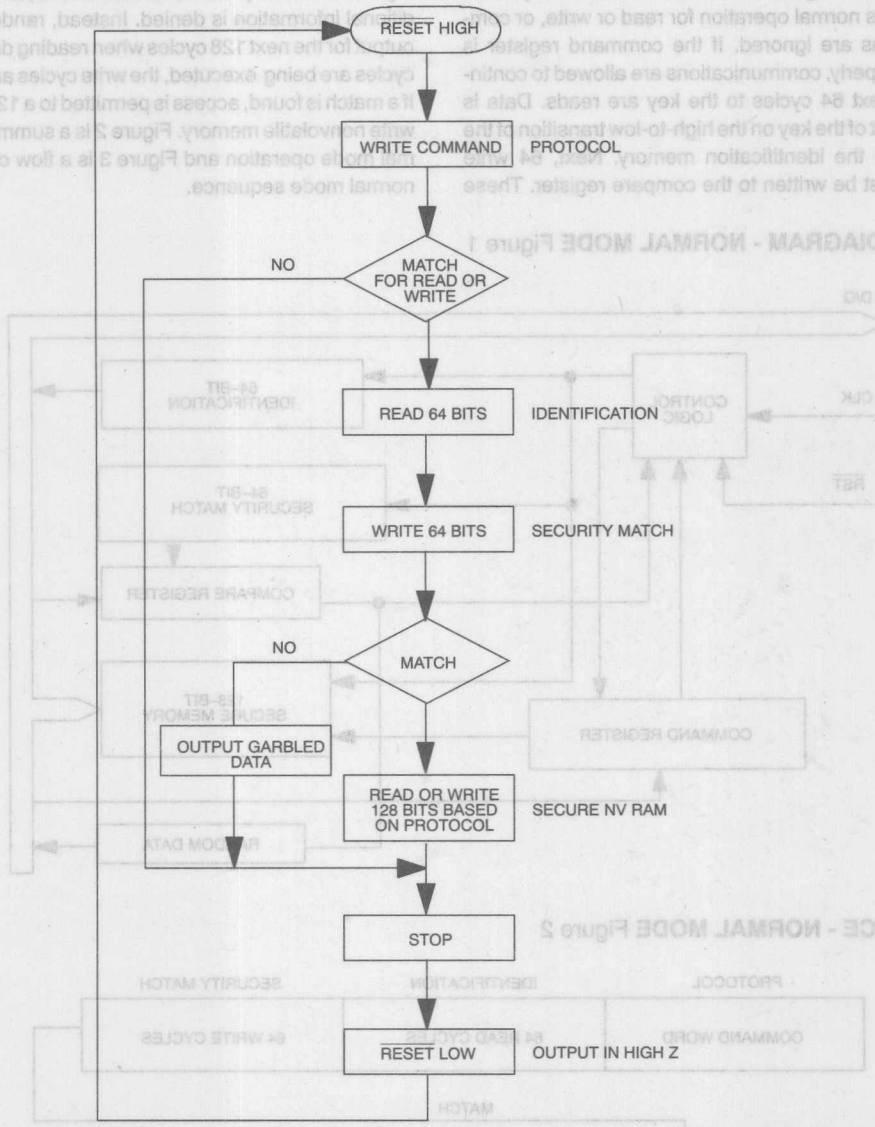
BLOCK DIAGRAM - NORMAL MODE Figure 1



SEQUENCE - NORMAL MODE Figure 2



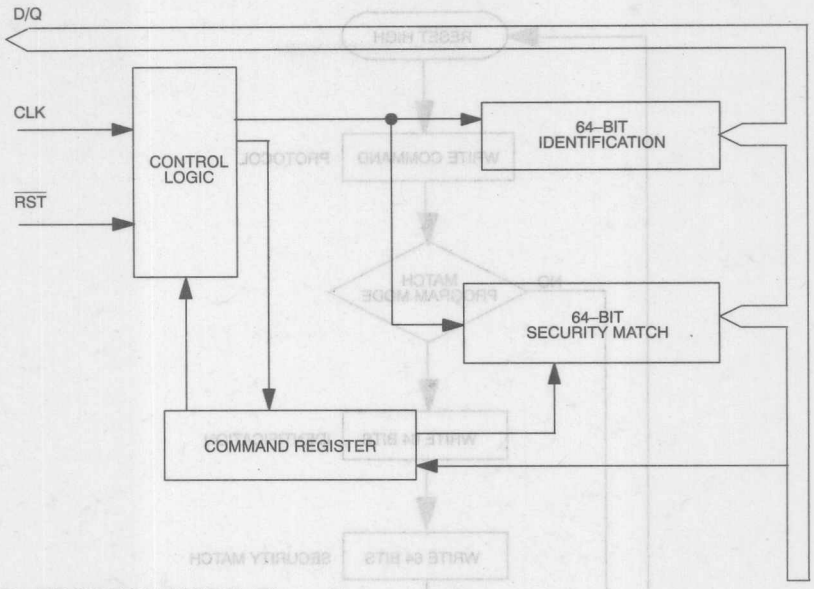
FLOW CHART - NORMAL MODE Figure 3



PROGRAM MODE

The block diagram in Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact pattern that defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the 128 bits that follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

BLOCK DIAGRAM - PROGRAM MODE Figure 4



SEQUENCE - PROGRAM MODE Figure 5

PROTOCOL	IDENTIFICATION	SECURITY MATCH
COMMAND WORD	64 WRITE CYCLES	64 WRITE CYCLES

COMMAND WORD

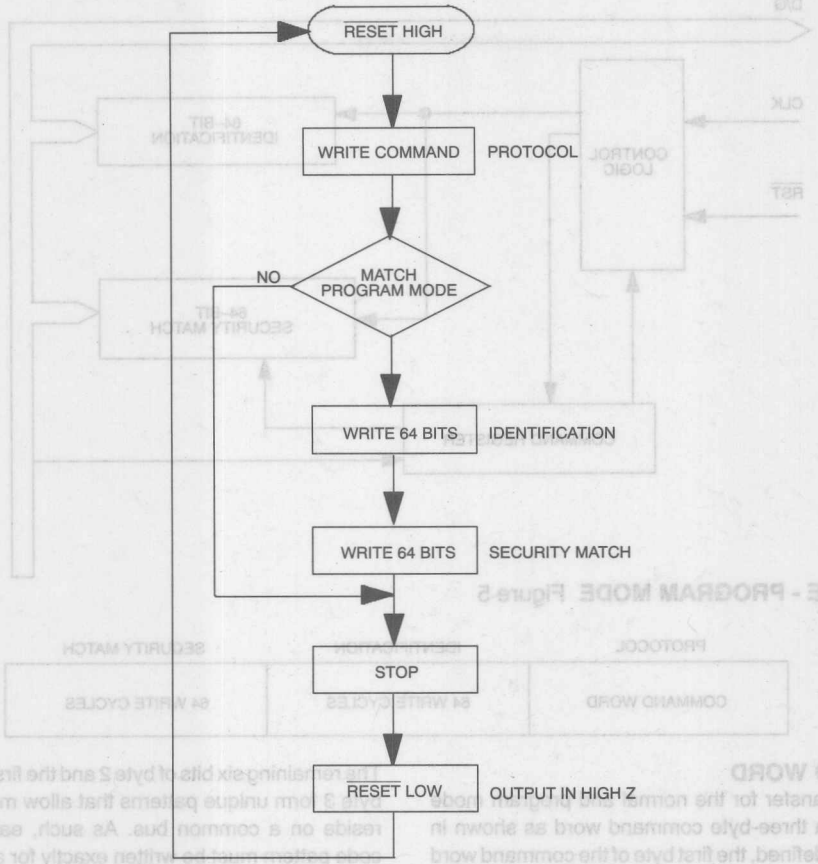
Each data transfer for the normal and program mode begins with a three-byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128-bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern that selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining six bits of byte 2 and the first seven bits of byte 3 form unique patterns that allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has five patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor, the user can specify any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

NOTE:
Contact the Dallas Semiconductor sales office for a special command word code assignment that makes possible an exclusive blank key.

FLOW CHART - PROGRAM MODE Figure 6

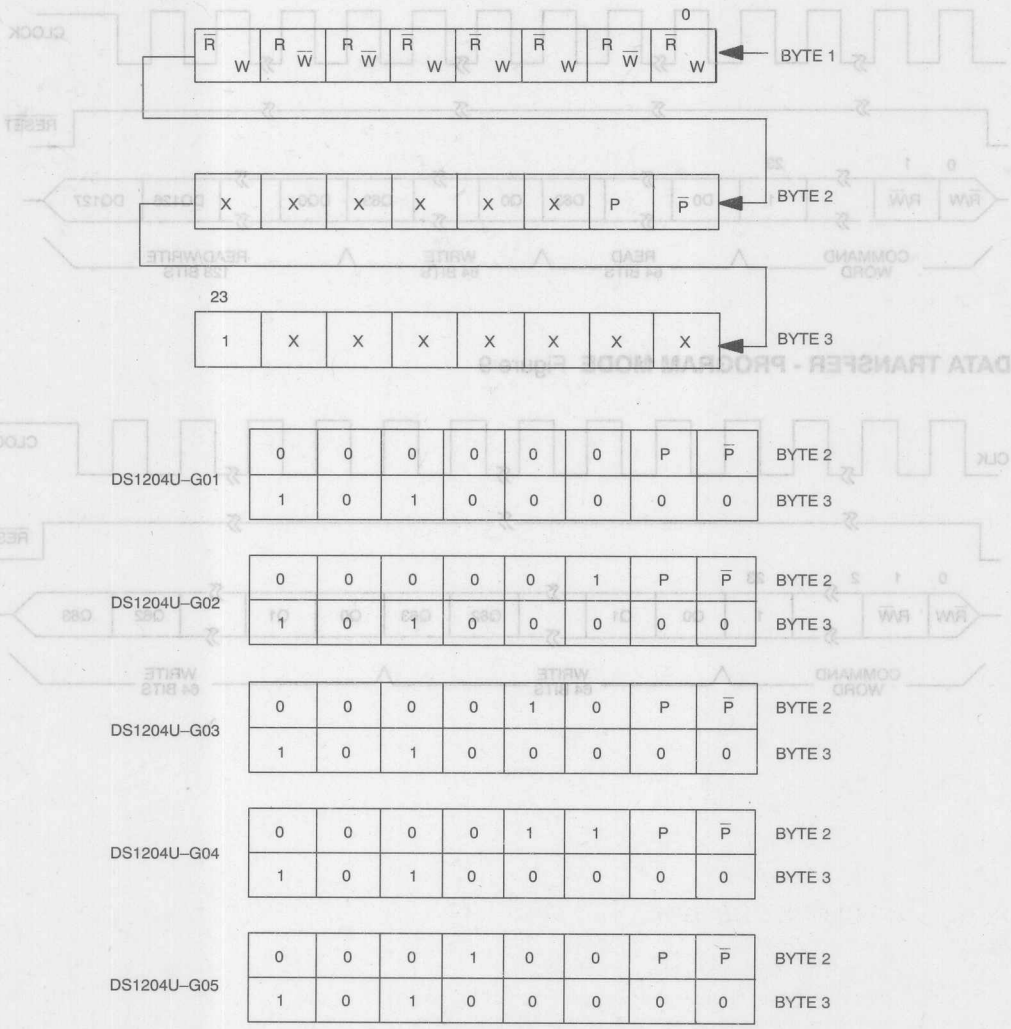


RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves three functions. First, it turns on control logic, which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA @ 3.5 volts is required. However, if the V_{CC} pin is connected to a 5-volt source within nominal limits, the $\overline{RST}$ is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 µA. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at a high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

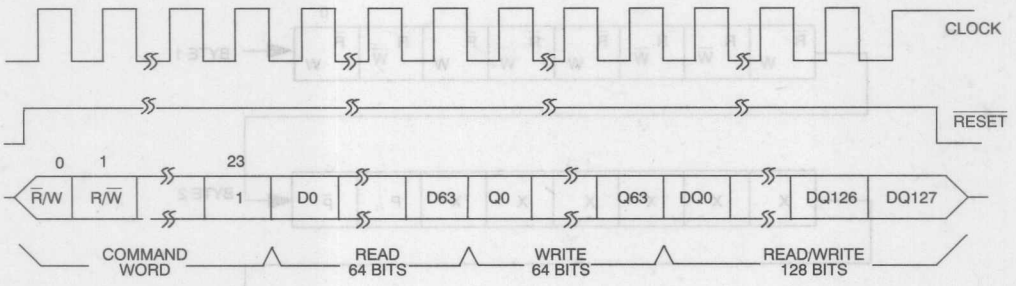
COMMAND WORD Figure 7



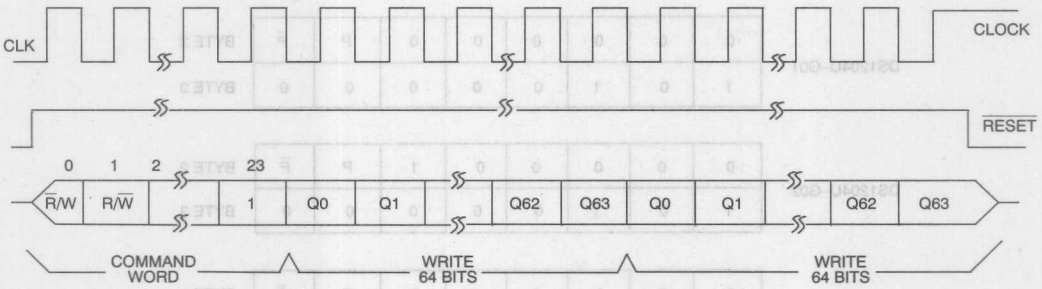
KEY CONNECTIONS

The key is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle (SAMTEC SS–105 or equivalent). A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the key pins can be determined to ensure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DQ all have internal 20K ohm pulldown resistors to ground that can be sensed by a reading device.

DATA TRANSFER - NORMAL MODE Figure 8



DATA TRANSFER - PROGRAM MODE Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1, 8, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.5			V	1, 9, 11
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	µA	4
Output Leakage	I_{LO}			+500	µA	
Output Current @2.4V	I_{OH}	-1			mA	
Output Current @0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		60	K ohms	
D/Q Input Resistance	Z_{DQ}	10		60	K ohms	
CLK Input Resistance	Z_{CLK}	10		60	K ohms	
$\overline{\text{RST}}$ Current @3.0V	I_{RST}			2	mA	6, 9, 13
Active Current	I_{CC1}			6	mA	6
Standby Current	I_{CC2}			2.5	mA	6

CAPACITANCE

(t_A = 25°C)

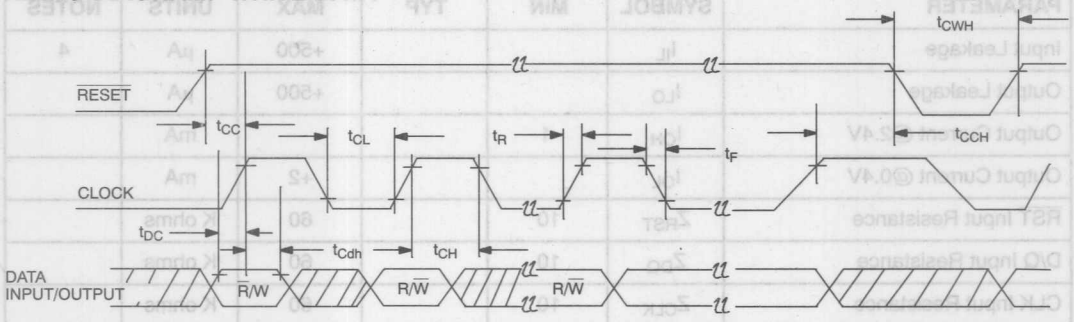
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

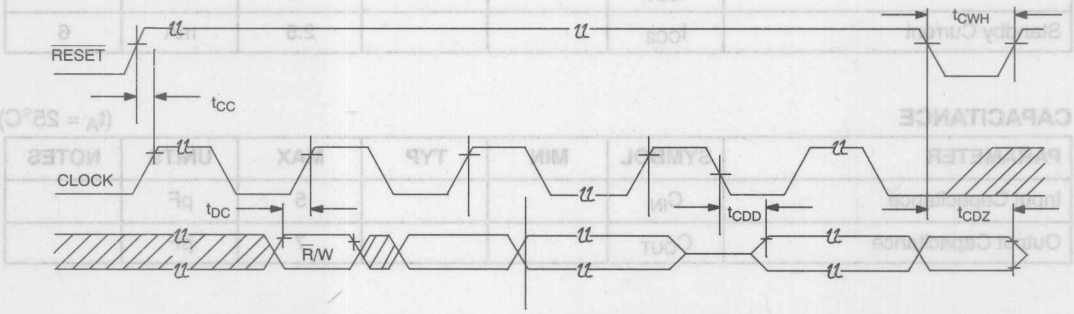
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2, 7
CLK to Data Hold	t_{CDH}	40			ns	2, 7
CLK to Data Delay	t_{CDD}			100	ns	2, 3, 5, 7
CLK Low Time	t_{CL}	125			ns	2, 7
CLK High Time	t_{CH}	125			ns	2, 7
CLK Frequency	f_{CLK}	DC		4.0	MHz	2, 7
CLK Rise & Fall	t_R, t_F	500			ns	2, 7
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2, 7
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2, 7
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	2, 7, 14
$\overline{RST}$ to I/O High Z	t_{CDZ}			50	ns	2, 7

TIMING DIAGRAM: WRITE DATA



TIMING DIAGRAM: READ DATA



NOTES:

1. All voltages are referenced to GND.
2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10ns maximum rise and fall time.
3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
4. For CLK, D/Q, and $\overline{RST}$.
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST} \geq 3.5V$ when $\overline{RST}$ supplies power.
8. Logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and $\overline{RST}$ + 0.3 volts if the $\overline{RST}$ pin supplies power.
9. Applies to $\overline{RST}$ when $V_{CC} < 3.5V$.
10. Input levels apply to CLK, DQ, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the key, then $\overline{RST}$ input reverts to V_{IHE}.
11. $\overline{RST}$ logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1204V is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture.
13. Average AC $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3})\ (CL + 140)^f$
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHz.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I_{TOTAL} of 5 mA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to100 ms average.

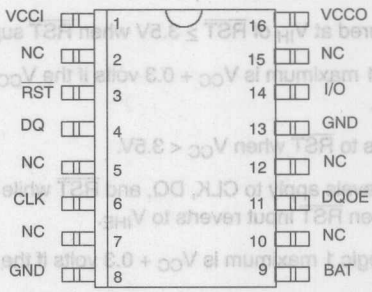
DALLAS SEMICONDUCTOR

DS1205S MultiKey Chip

FEATURES

- Three secure read/write data partitions of 384 bits each
- One non-secure read/write data partition of 512 bits
- Secure data cannot be deciphered by reverse engineering
- Guaranteed unique, 48-bit, laser etched serial number
- 64-bit password and I.D. fields provide positive identification and security for each secure data partition
- Maximum data transfer rate of 2 million bits/second
- Low-power CMOS circuitry
- Access via 3-wire or 1-wire interface
- Applications include proprietary data, financial transactions, secure personnel areas, and systems access control

PIN ASSIGNMENT



DS1205S 16-Pin SOIC (300 mil)
See Mech. Drawing Pg. 338

PIN DESCRIPTION

V_{CCI}	–	+5V Supply (Battery Backup Mode)
$\overline{RST}$	–	Reset (3-Wire)
DQ	–	Data (3-Wire)
CLK	–	Clock (3-Wire)
GND	–	Ground
BAT	–	Battery (+) (Battery Backup Mode)
DQOE	–	Data Available (3-Wire)
I/O	–	Data I/O (1-Wire)
V_{CCO}	–	Battery (+) (Battery Powered Mode)

DESCRIPTION

The DS1205S MultiKey Chip is an enhanced version of the DS1204U Electronic Key which has both a standard 3-wire interface (data, clock, and reset) and a 1-wire interface. The DS1205S MultiKey has three secure read/write subkeys which are each 384 bits in length. In addition, there is a 512-bit read/write scratchpad which can be used as a non-secure data area or as a holding register for data transfer to one of the three subkeys. Each subkey within the part is uniquely addressable on byte boundaries.

OPERATING MODES

There are two modes of operation for powering the DS1205S MultiKey Chip. In the Normal Mode (Battery Backup), V_{CC} power is supplied to the part on the V_{CCI} pin, while the battery backup source is applied to the BAT pin. In this mode of operation, the chip supply is switched internally between V_{CCI} and BAT (depending on which is higher) and this level is presented internally to the V_{CCO} pin. In the Battery Operate Mode, the battery supply is connected directly to the V_{CCO} pin while the V_{CCI} and BAT pins are grounded.

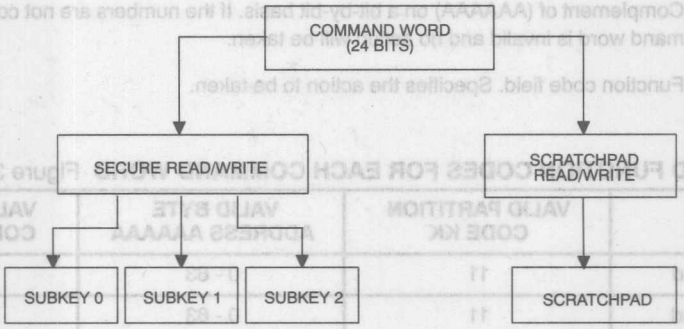
INTERFACES

Two interfaces to the DS1205S are provided. The 1-wire interface requires a 1-wire I/O command for addressing the device. An additional function command word is then passed through the 1-wire interface to access the various DS1205S functions. The 3-wire interface (data (DQ), reset ($\overline{RST}$), and clock (CLK)) requires only the function command word. The four 1-wire I/O commands that deal with the unique lasered ROM are available only through the 1-wire interface. All other functions are available through either interface.

FUNCTIONS

A command word written written to the DS1205S MultiKey specifies the operation to be performed and the partition to be operated on. There are two classes of functions available. One class includes operations on the read/write secure partitions. The other class includes operations on the read/write scratchpad (Figure 1).

COMMAND OPERATIONS Figure 1



The 24 bit function command word is organized into three fields of eight bits each. These one byte fields include the function to be performed, the memory partition to be accessed and the starting byte address for the data transfer operation. The starting byte address and the partition codes are required to be given in both real and complement form. If these values do not match, access to the part will be denied (Figure 2).

The function command word is presented to the DS1205S LSB first. The first byte contains the 8-bit function code that defines which of the six valid function codes is to be executed. Each function code is valid for only certain partition and starting address combinations. Figure 3 illustrates the valid partition code, starting address and function code combinations. The second byte consists of the 2-bit partition code, identifying which partition is being accessed, and the 6-bit starting byte address, which specifies where to start the access of the given partition. The third byte consists of the complement of the 2-bit partition code and the complement of the 6-bit starting byte address.

COMMAND WORD STRUCTURE Figure 2

MSB		LSB
$(KK)_C(AAAAAA)_C$	(KK) (AAAAAA)	FFFFFFFF

(KK) = Two-bit number specifying which partition is to be accessed. 00 specifies subkey 0. 01 specifies subkey 1. 10 specifies subkey 2. 11 specifies the scratchpad.

$(KK)_C$ = Complement of (KK) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

(AAAAAA) = Address field containing address bits that define the starting byte address of the partition to be accessed.

$(AAAAAA)_C$ = Complement of (AAAAAA) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

FFFFFFFF = Function code field. Specifies the action to be taken.

LOCATIONS, AND FUNCTION CODES FOR EACH COMMAND WORD Figure 3

COMMAND	VALID PARTITION CODE KK	VALID BYTE ADDRESS AAAAAA	VALID FUNCTION CODE FFFF FFFF
Set Scratchpad	11	0 - 63	1001 0110
Get Scratchpad	11	0 - 63	0110 1001
Set Secure Data	00, 01, 10	16 - 63	1001 1001
Get Secure Data	00, 01, 10	16 - 63	0110 0110
Set Security Match	00, 01, 10	000000	0101 1010
Move Block	00, 01, 10	000000	0011 1100

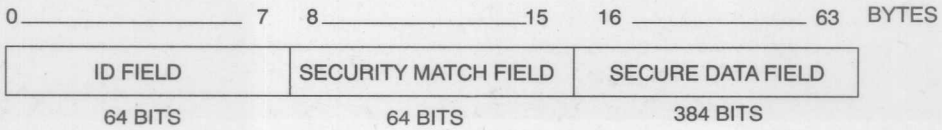
SECURE PARTITION COMMANDS

Each of the three secure partitions within the DS1205S MultiKey is comprised of a 64-bit I.D. field, a 64-bit security match code and a 384-bit secure data field (Figure 4). The three commands that operate on the secure partitions are:

1) Set Security Match
2) Set Secure Data
3) Get Secure Data

As a guard against attackers, the security match code can never be read. Similarly, tampering through reprogramming will immediately clear the entire secure partition.

SECURE PARTITION ORGANIZATION Figure 4



SET SECURITY MATCH

The Set Security Match command is used to enter data into the I.D. and security match fields of the selected secure partition. The DS1205S will respond to the command by outputting the 64-bit I.D. field of the selected secure partition. The next 64 clock cycles are used to echo the I.D. field back to the DS1205S. Upon receipt of the correct I.D., the DS1205S MultiKey will erase the contents of the selected secure partition. The part is then ready to receive the the new 64-bit I.D. and the 64-bit security match code. The flow sequence is shown in Figure 5.

SET SECURE DATA

The Set Secure Data command is used to write data into the selected secure partition. After the command is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is output. The next 64 bits of input comprise a password that must match the security match code of the selected secure partition. If the password and the security match are identical, data is written to the secure data field starting at the address specified in the command word. If the password and the security match code are not identical, the DS1205S will terminate the transaction immediately. The flow sequence is shown in Figure 6.

GET SECURE DATA

The Get Secure Data command is used to retrieve data from the selected secure partition. After the command word is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is returned. The next 64 bits are the password being written to the DS1205S. If the presented password and the security match code of the selected secure partition are identical, the DS1205S will output the contents of the secure data field starting from the byte specified in the command word. If the presented password is not identical to the security match code, the DS1205S MultiKey will use the password as a "seed" for its internal random number generator. This results in a repeatable, seemingly valid yet false response to the invalid password. The flow sequence is shown in Figure 7.

SCRATCHPAD READ/WRITE COMMANDS

The 512-bit read/write scratchpad of the DS1205S MultiKey is not protected by a security match code. This partition is byte addressable. The scratchpad can be used to store unsecured data or it can act as a staging area to build and verify data structures to be transferred to a secure partition. The three commands that operate on the read/write scratchpad are:

1. Set Scratchpad Data
2. Get Scratchpad Data
3. Move Block

SET SCRATCHPAD DATA

The Set Scratchpad Data command is used to enter data into the DS1205S MultiKey scratchpad. The command word must specify the starting byte address for the data transfer. Valid byte addresses are 0 through 63. The DS1205S MultiKey will write data to the scratchpad until byte 63 has been written or until the $\overline{RST}$ line goes to a logic low level. The flow sequence is shown in Figure 8.

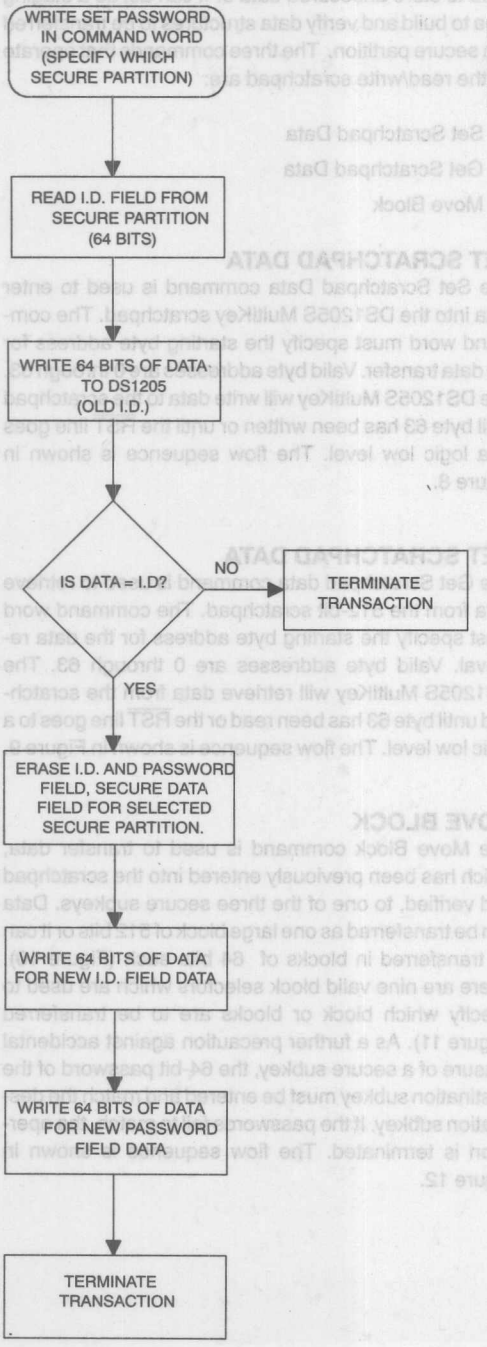
GET SCRATCHPAD DATA

The Get Scratchpad data command is used to retrieve data from the 512-bit scratchpad. The command word must specify the starting byte address for the data retrieval. Valid byte addresses are 0 through 63. The DS1205S MultiKey will retrieve data from the scratchpad until byte 63 has been read or the $\overline{RST}$ line goes to a logic low level. The flow sequence is shown in Figure 9.

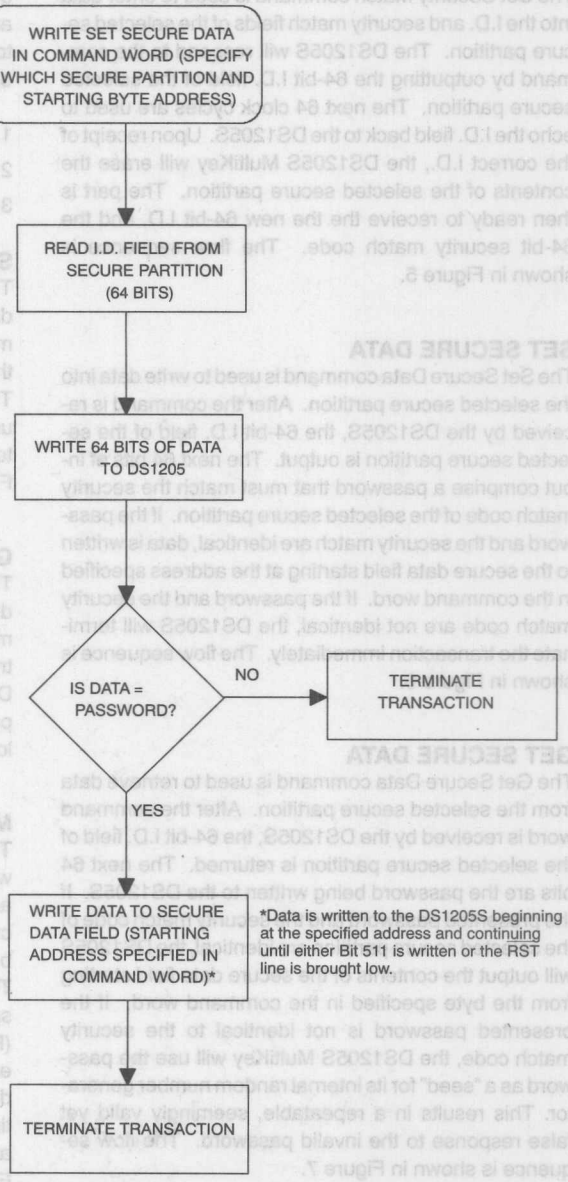
MOVE BLOCK

The Move Block command is used to transfer data, which has been previously entered into the scratchpad and verified, to one of the three secure subkeys. Data can be transferred as one large block of 512 bits or it can be transferred in blocks of 64 bits each (Figure 10). There are nine valid block selectors which are used to specify which block or blocks are to be transferred (Figure 11). As a further precaution against accidental erasure of a secure subkey, the 64-bit password of the destination subkey must be entered and match the destination subkey. If the passwords fail to match, the operation is terminated. The flow sequence is shown in Figure 12.

SET SECURITY MATCH Figure 5

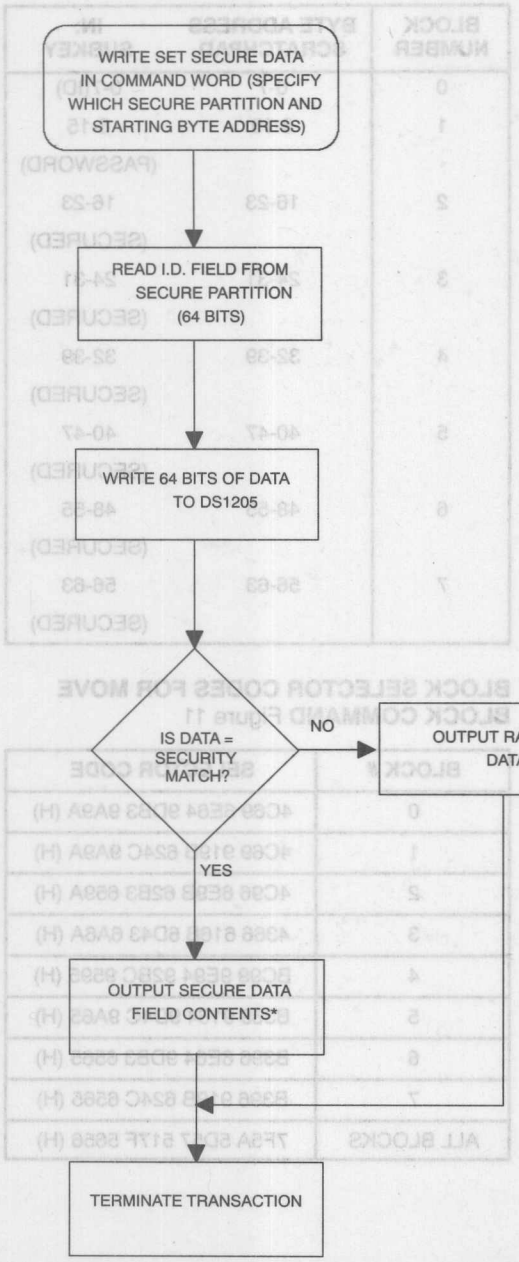


SET SECURE DATA Figure 6



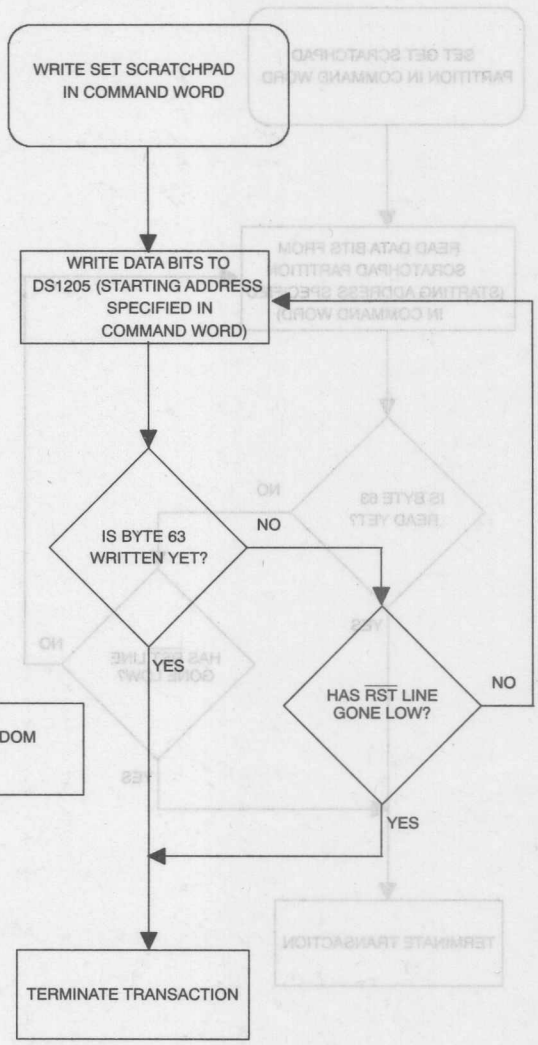
*Data is written to the DS1205S beginning at the specified address and continuing until either Bit 511 is written or the RST line is brought low.

GET SECURE DATA Figure 7

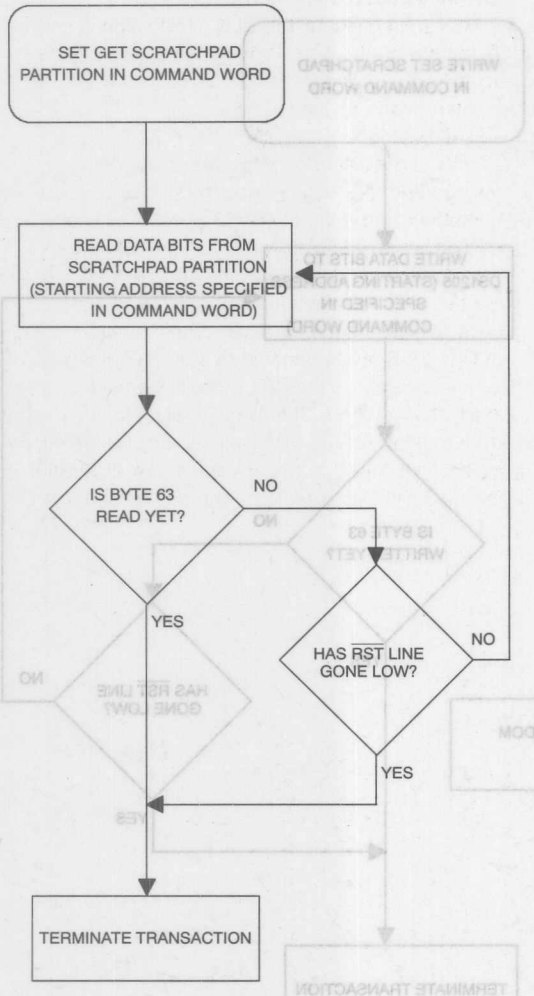


*Data is read from the DS1205S beginning at the specified address and continuing until either Bit 511 is read or the $\overline{RST}$ line is brought low.

SET SCRATCHPAD Figure 8



SET SCRATCHPAD Figure 9



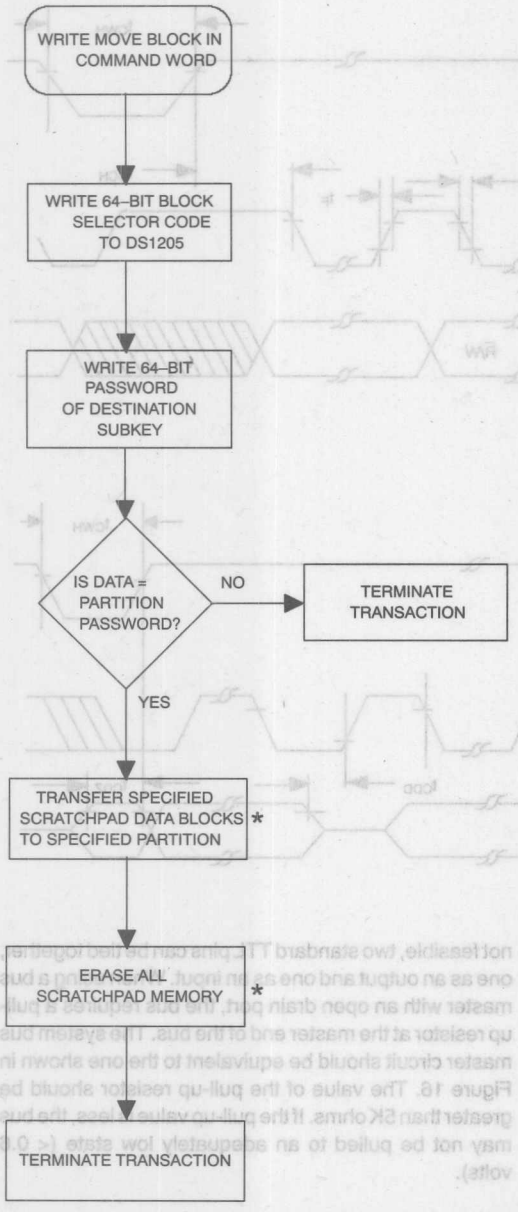
BLOCK SELECTIONS Figure 10

BLOCK NUMBER	BYTE ADDRESS SCRATCHPAD	IN: SUBKEY
0	0-7	0-7(ID)
1	8-15	8-15 (PASSWORD)
2	16-23	16-23 (SECURED)
3	24-31	24-31 (SECURED)
4	32-39	32-39 (SECURED)
5	40-47	40-47 (SECURED)
6	48-55	48-55 (SECURED)
7	56-63	56-63 (SECURED)

BLOCK SELECTOR CODES FOR MOVE BLOCK COMMAND Figure 11

BLOCK #	SELECTOR CODE
0	4C69 6E64 9DB3 9A9A (H)
1	4C69 919B 624C 9A9A (H)
2	4C96 6E9B 62B3 659A (H)
3	4366 616B 6D43 6A6A (H)
4	BC99 9E94 92BC 9595 (H)
5	B369 9164 9D4C 9A65 (H)
6	B396 6E64 9DB3 6565 (H)
7	B396 919B 624C 6565 (H)
ALL BLOCKS	7F5A 5D57 517F 5656 (H)

MOVE BLOCK Figure 12

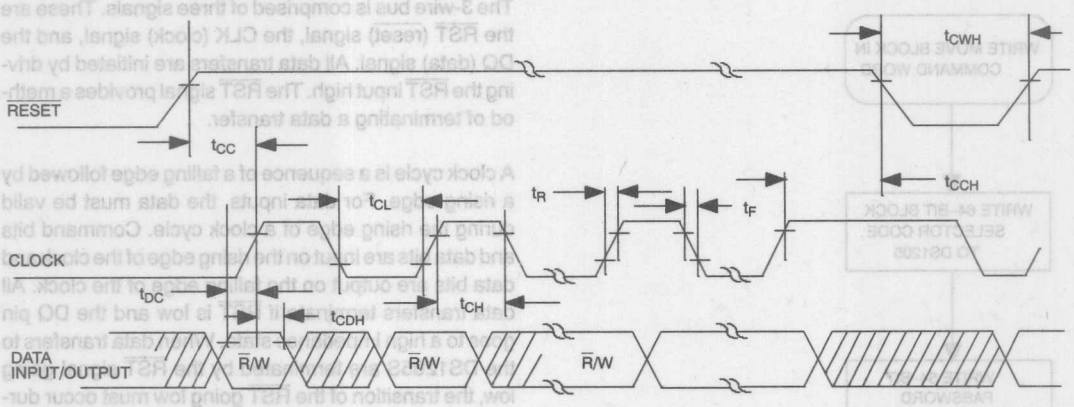


3-WIRE BUS

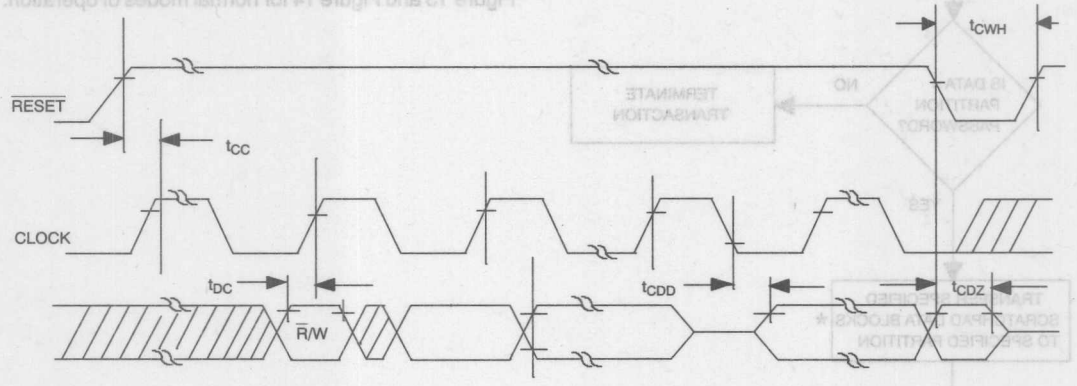
The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ ($\overline{reset}$) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if $\overline{RST}$ is low and the DQ pin goes to a high impedance state. When data transfers to the DS1205S are terminated by the $\overline{RST}$ signal going low, the transition of the $\overline{RST}$ going low must occur during a high level of the CLK signal. Failure to ensure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figure 13 and Figure 14 for normal modes of operation.

WRITE DATA TIMING DIAGRAM Figure 13



READ DATA TIMING DIAGRAM Figure 14



1-WIRE PROTOCOL

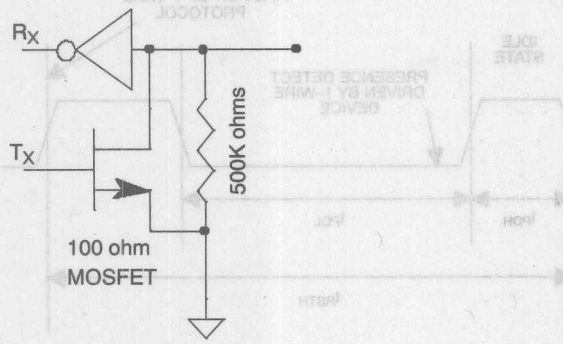
The 1-wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1205S is a slave. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence.

Hardware Configuration

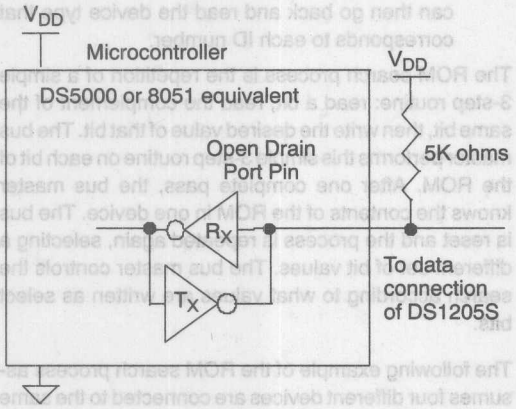
The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain connections. The DS1205S is an open drain part with an internal circuit equivalent to that shown in Figure 15. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 16. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

The idle state for the 1-wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left for more than 560 μS, all components on the bus will be reset.

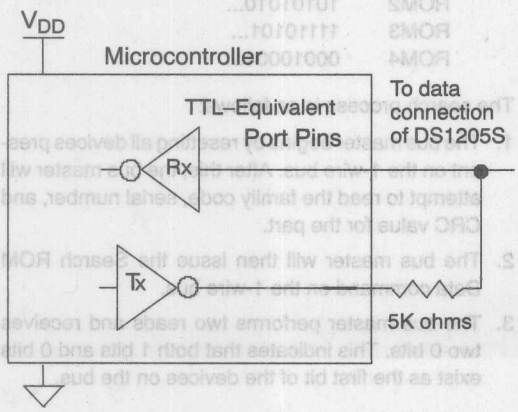
EQUIVALENT CIRCUIT Figure 15



BUS MASTER OPEN DRAIN CIRCUIT Figure 16A



BUS MASTER STANDARD TTL CIRCUIT Figure 16B



Transaction Sequence

The protocol for accessing the DS1205S is as follows:

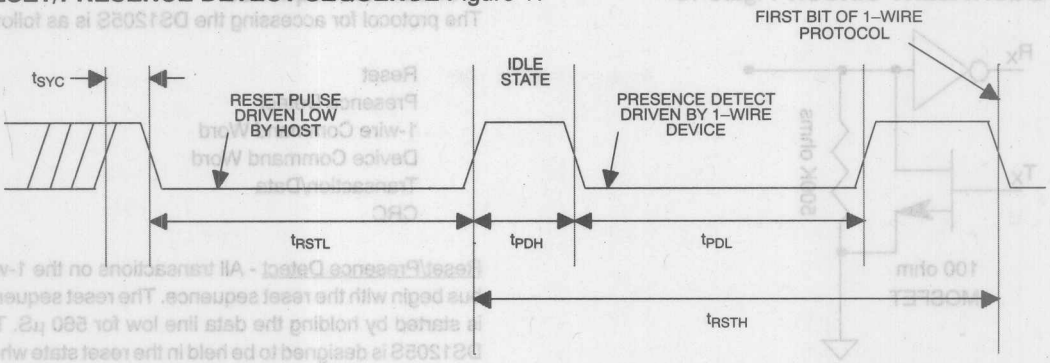
Reset
Presence Detect
1-wire Command Word
Device Command Word
Transaction/Data
CRC

Reset/Presence Detect - All transactions on the 1-wire bus begin with the reset sequence. The reset sequence is started by holding the data line low for 560 μS. The DS1205S is designed to be held in the reset state whenever it is not connected to the bus. When it is connected to the bus, the data line is pulled high, the part is taken out of reset, and the part is ready to issue the presence detect.

After detecting a high state on the data line, the DS1205S waits 15 μS minimum and issues its presence detect. This presence detect is a low-going pulse that last 70 μS. This response to the reset pulse lets the bus master know that the DS1205S is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from noise as the DS1205S is taken on and off the bus. Refer to the timing diagram in Figure 17.

After the DS1205S has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of 1 μS. The 1 μS interval is like a frame sync. After each bit is transmitted on the bus, there is a frame strobe to sync up for the next transmission. Refer to Figure 17.

RESET/PRESENCE DETECT SEQUENCE Figure 17



1-Wire I/O Commands - Once the bus master has detected a presence, it can issue one of the four different 1-wire I/O commands. These commands deal with the laser-etched ROM code which has the following format.

Type ID	Unique Serial Number	CRC
8 bits	48 bits	8 bits

All 1-wire commands are eight bits long. A list of these commands are as follows:

CCh Pass Thru Mode

This command saves time by allowing direct access to the DS1205S without identifying it by ROM ID number. This command can only be used when there is a single slave on the bus. If more than one device is present, there will be bus contention.

33h Read ROM Data

This command allows the bus master to read the DS1205S's unique 48-bit ID number and CRC. This command can only be used if there is a single DS1205S on the bus. If more than one is present, there will be bus contention.

55H Match ROM Data

This mode allows the bus master to single out a specific DS1205S on a multidrop bus. The bus master selects the specific slave by the ROM ID number for the transaction. This command can be used with a single or multiple device on the bus.

F0h Search ROM Data

When a system is initially brought up, the bus master might not know the number or types of devices on the bus. By invoking the Search ROM Data command the bus master can, by process of elimination, find the ID numbers of all the devices on the bus. Once this is known, the bus master can then go back and read the device type that corresponds to each ID number.

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the same bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The bus is reset and the process is repeated again, selecting a different set of bit values. The bus master controls the search according to what values are written as select bits.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1 00110101...
ROM2 10101010...
ROM3 11110101...
ROM4 00010001...

The search process is as follows:

1. The bus master begins by resetting all devices present on the 1-wire bus. After this, the bus master will attempt to read the family code, serial number, and CRC value for the part.
2. The bus master will then issue the Search ROM Data command on the 1-wire bus.
3. The bus master performs two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the first bit of the devices on the bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

At this point, the bus master repeats the process described above to determine the address of the remaining devices on the 1-wire bus by repeating steps 1 though 7.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ID is:

$$960\ \mu S + 3(8+64)\ X\ 0.06mS = 13.92mS$$

The bus master is therefore capable of identifying 60 different 1-wire devices per second.

Additionally, the data obtained from the two reads of each set of three have the following interpretations:

00 - There are still devices attached which have conflicting bits in this position.

01 - All devices still coupled have a zero bit in this bit position.

10 - All devices still coupled have a one bit in this bit position.

11 - There are no devices attached to the 1-wire bus.

Transmitting/Receiving Data - All communications on the 1-wire bus begin with the reset and presence detect sequence. This sequence ensures the DS1205S is in the listening mode. The bus master must then transmit the 1-wire command to the DS1205S. To transmit the first bit of the 1-wire I/O command, the master pulls the bus low for 1 μS. This low-going edge informs the DS1205S that the first bit is being sent. After 1 μS, the master does one of two things:

1. holds the line low for an additional 70 μS to output a 0 (write a 0) or,
2. lets the bus go high for an additional 70 μS (write a 1).

The state of the bus during this 70 μS time phase determines the value of the bit. The DS1205S will sense any rising edge during this 70 μS time phase as a one. After the 70 μS has lapsed, the bus master must then drive the bus high for 1 μS. This is the frame sync mentioned earlier. This process is repeated until all the eight bits are transmitted. Refer to the timing diagram in Figure 18.

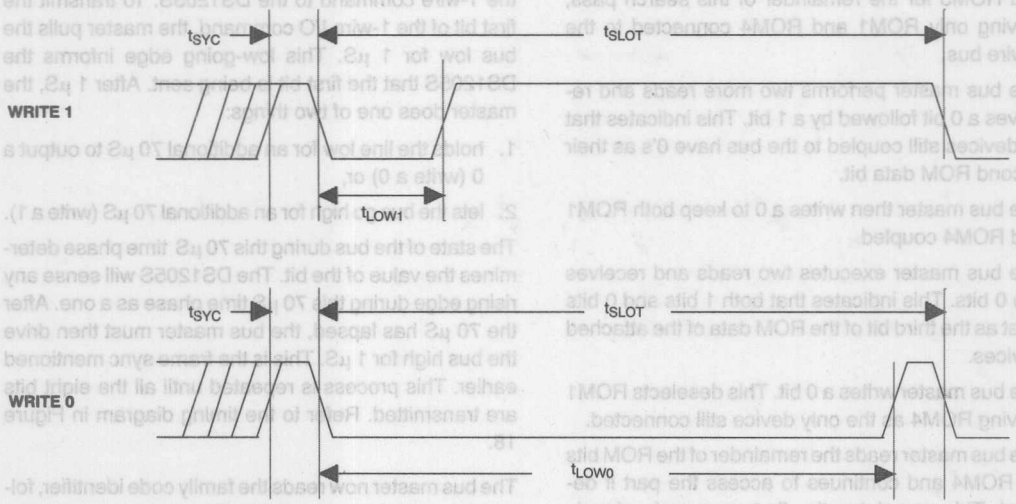
The bus master now reads the family code identifier, followed by the data and a CRC. The read cycle is similar to the write cycle. It is started with the bus master pulling the bus low for 1 μS. This informs the DS1205S that it should have data on the bus no later than the 1 μS from the falling edge. After the 1 μS, the bus master lets go of the bus and the DS1205S drives the bus. The slave must hold the data on the bus for an additional 14 μS minimum (59 μS maximum). During the DS1205S holding time, the bus master reads the state of the bus. Ideally, the bus master should read data from the bus 15 μs after the falling edge. The entire cycle time for one bit lasts a minimum of 70 μS (140 μS maximum) from the falling edge. At the end of the cycle, the bus master drives the bus high for 1 μS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 19 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1205S must be reset.

CRC Generation - To validate the transmitted data from the DS1205S, the bus master must generate a CRC value for the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1205S. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but NOT over the stored CRC value itself. The CRC is calculated using the following polynomial.

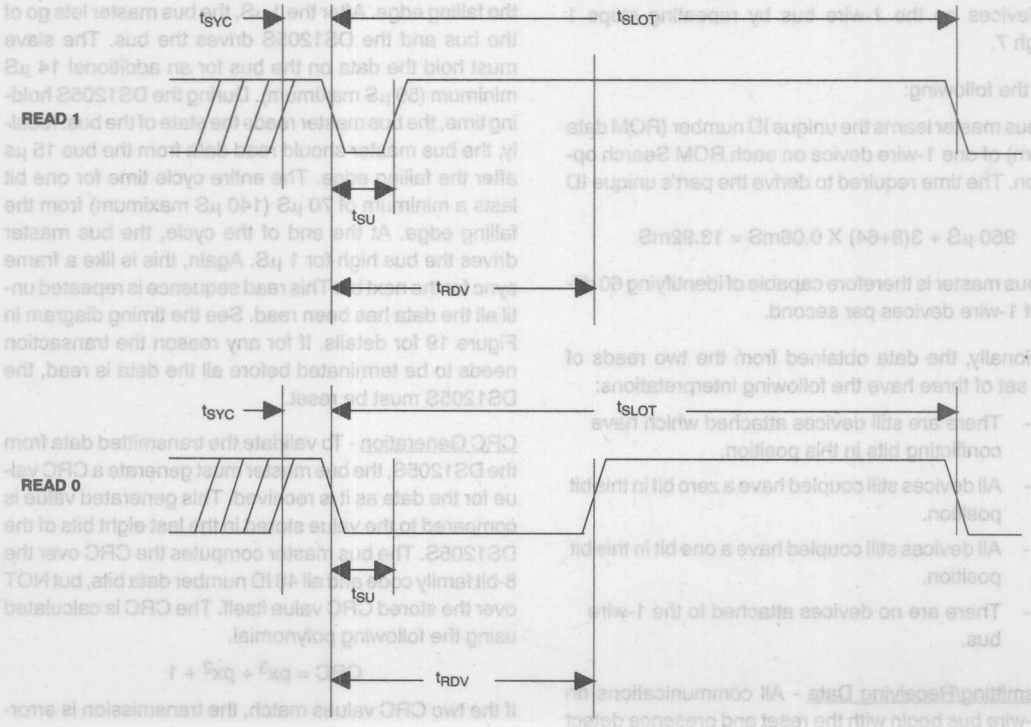
$$CRC = px^3 + px^2 + 1$$

If the two CRC values match, the transmission is error-free.

1-WIRE WRITE TIMING Figure 18



1-WIRE READ TIMING Figure 19



PASS-THRU MODE

A host connected to the 1-wire bus may send function commands directly to the DS1205S without preceding them with 1-wire I/O commands by using the pass-thru command (CCh). This command bypasses the serial number and consequently it can only be used when there is one DS1205S on the 1-wire bus.

1-WIRE/3-WIRE ARBITRATION

The DS1205S can utilize both the 1-wire and the 3-wire busses simultaneously. Neither input bus has priority over the other. Instead, if both inputs are being used, the signal arriving first will take precedence. More simply, if the 1-wire interface becomes active before the 3-wire interface, all communications will take place on the 1-wire bus. The 3-wire bus will be ignored in this case. The same condition occurs for the 1-wire interface if the 3-wire interface becomes active first.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	µA	
Output Leakage	I_{OL}			+500	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+1	mA	
$\overline{RST}$ Input Resistance	Z_{RST}	100		1000	Kohm	
D/Q Input Resistance	Z_{DQ}	100		1000	Kohm	
CLK Input Resistance	Z_{CLK}	100		1000	Kohm	
Active Current	I_{CC1}		3	6	mA	5,6
Standby Current	I_{CC2}			100	µA	5,6
Batt. Operate Consumption	I_{BAT}		200	500	nC	7,8
Batt. Operate Standby Current	I_{BATS}		30	200	nA	7
Batt. Voltage	V_{BAT}	2.0		3.6	V	1
Output Supply Current	I_{CCO}			10	mA	11

CAPACITANCE

(t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			200	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(0°C to 70°C, V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot Period	t_{SLOT}	70		140	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	70		140	µs	
Read Data Valid	t_{RDV}	15			µs	
Read Data Setup	t_{SU}	1			µs	10
Frame Sync	t_{SYC}	1			µs	
Reset Low Time	t_{RSTL}	560			µs	
Reset High Time	t_{RSTH}	560			µs	9
Presence Detect High	t_{PDH}	15		70	µs	
Presence Detect Low	t_{PDL}	70		280	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. (Normal battery backup operation) V_{CC1} = 5.0 Volts ± 10%; V_{BAT} = 3.0 Volts.
7. (Battery operate mode) V_{CCO} = 3.0 Volts.
8. Per transaction (512 bits + protocol).
9. An additional reset or communication sequence cannot begin until the reset high time has expired.
10. Read data setup time refers to the time the host must pull the 1-wire pin low to read a bit. Data is guaranteed to be valid within 1 µS of this falling edge and will remain valid for 14 µS minimum (15 µS total falling edge on 1-wire).
11. $V_{CCO} = V_{CCI} - 0.3V$

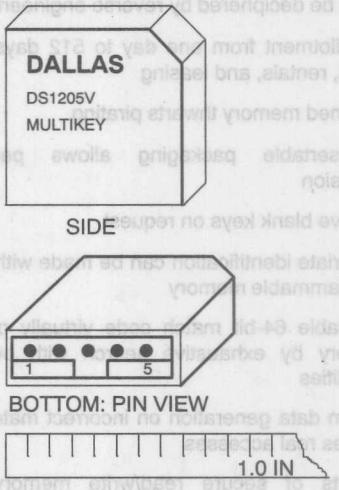
DALLAS SEMICONDUCTOR

DS1205V MultiKey

FEATURES

- Three secure read/write data partitions of 384 bits each
- 64-bit security match and I.D. fields provide positive identification and security for each secure data partition
- One non-secure read/write partition of 512 bits
- Electrical tampering is met with seemingly valid, yet false, responses
- Secure data cannot be deciphered by reverse engineering
- Access via Dallas 3-Wire Interface
- Applications include software authorization, configuration management, and systems access control

PIN ASSIGNMENT



See Mech. Drawing – Pg. 350

DESCRIPTION

The DS1205V MultiKey has three, 384-bit read/write data partitions, each protected by its own 64-bit I.D. and security match fields. The security match field, programmed by the customer, can never be read from the DS1205V. An additional security feature, the Intelligent Response generator, uses invalid security match codes as the "seed" to trigger seemingly valid, yet false responses to electronic attack.

Communication with the DS1205V is via the Dallas 3-Wire Interface (Data, Clock, $\overline{\text{Reset}}$). These signals are under host software control.

The DS1205V MultiKey is designed to be plugged into a standard 5-pin, 0.1 inch-center SIP receptacle. A guide is provided to insure proper alignment with the receptacle.

System designers can use the DS1205V to insure that their valuable firmware can only by run when a valid key is present. The MultiKey can also contain data on system configurations and upgrade options. Designers may choose to allow maintenance or diagnostic routines to be run only by an authorized key holder.

See the DS1205S MultiKey Chip data sheet for implementation details.

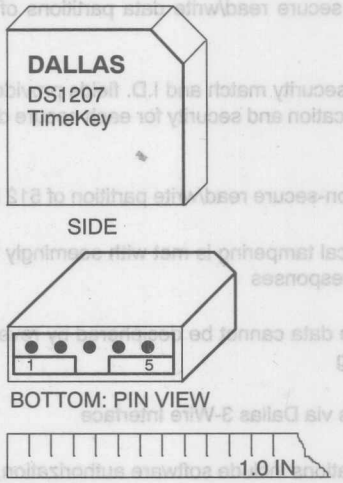
DALLAS SEMICONDUCTOR

DS1207 TimeKey

FEATURES

- Cannot be deciphered by reverse engineering
- Time allotment from one day to 512 days for trial periods, rentals, and leasing
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit match code virtually prevents discovery by exhaustive search with over 10^{19} possibilities
- Random data generation on incorrect match codes obscures real accesses
- 384 bits of secure read/write memory create additional barriers by permitting data changes as often as needed
- Rapid erasure of identification, security match code and secure read/write memory can occur if tampering is detected
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN ASSIGNMENT



See Mech. Drawing – Pg. 350

PIN DESCRIPTION

Pin 1	NC	No connection
Pin 2	$\overline{RST}$	Reset
Pin 3	DQ	Data input/output
Pin 4	CLK	Clock
Pin 5	GND	Ground

DESCRIPTION

The DS1207 TimeKey is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 384 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the TimeKey via a special program mode operation. After programming, the TimeKey follows a procedure with a serial format to retrieve or update data. The TimeKey is set to expire from one day to 512 days or infinity, as specified by the customer. The TimeKey starts its countdown from the first access by the end user.

Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), Reset ($\overline{RST}$) and Data Input/Output (DQ). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

OPERATION – NORMAL MODE

The TimeKey has two modes of operation: normal and program. The normal mode of operation provides the functions of reading and writing the 384-bit secure memory. The block diagram (Figure 1) illustrates the main elements of the TimeKey when used in the normal mode. To initiate data transfer with the TimeKey, $\overline{RST}$ is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines normal operations with a function code of read or write. If one of these patterns is not matched, communications are ignored. If the command register is loaded properly, communications are allowed to continue. Data is clocked out of the TimeKey on the high-to-low transition of the clock. If the pattern matched in the command register calls for a normal read or write, the next 64 cycles following the command word are read and data is clocked out of the identification memory. The next 64 write cycles are written to the compare register (Figure 2). These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, if a normal read mode is selected, random garbled data is output for the next 384 cycles. If a normal write cycle is selected and a match is not achieved, the TimeKey will ignore any additional information. However, when a security match is achieved, access is permitted to write the 384-bit secure memory.

OPERATION - PROGRAM MODE

The program mode of operation provides the functions of programming the identification and security match memory, and setting and reading the amount of time the TimeKey can be used. The block diagram in Figure 3 illustrates the main elements of the TimeKey when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines the program mode for the identification and security match bits or the program mode for setting and reading the amount of time for which the TimeKey can be used. If an exact match for one of the seven function codes of the program mode is not found, the remainder of the program mode is ignored. When the command register is properly loaded for programming the identification and security match bits, the next 128 bits are written to the identification and security match memory (Figure 4). When this mode of operation is invoked, all memory contents are erased.

SETTING AND READING TIME REMAINING

There are six functions of the program mode which are used to set or read the amount of time for which the TimeKey will allow full operation. To initiate any of the six functions of the program mode used for setting and reading time remaining, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. If the command register is properly loaded with the function code for reading the 20-bit day clock counter, the next 20 bits will be output (LSB first) as a binary count of the amount of time elapsed in the current day (see Figure 5). The time can be calculated by dividing this count reading by 2^{20} (20 bits is equal to 1,048,576 counts). One minus this result is the fraction of a day remaining. The 20-bit day clock counter is driven by an internal oscillator that has a period of 82.4 ms. If the command register is properly loaded with the function code for reading the 9-bit number of days counter, the next 9 bits will be output (LSB first) as a binary count of the days remaining (see Figure 6). This count is decremented each time the day clock counter rolls over to zero. When the number of days remaining counter rolls through zero, normal and program mode write cycles are inhibited. If the program mode read cycle to the number of days counter is attempted, the nine bits will be returned as all ones.

If the command register is properly loaded with the function code for writing the 9-bit number of days counter, the next nine bits will be input (LSB first) as a binary count of the desired number of days in which the TimeKey will be fully functional (see Figure 7). The number of days counter can be changed by writing over an entered value as often as required until the lock command is entered. The lock command is given when the command register is properly loaded with the function code for locking up the number of days counter. The lock command consists of the 24-bit command word only (see Figure 8). Once the lock command is given, all future write cycles to the number of days register are ignored. After the correct value has been written and locked into the number of days counter, the DS1207 will start counting the time from the entered value to zero after the first access to the TimeKey is executed, provided the arm oscillator bit is set. The arm oscillator bit is set when the command register has been properly loaded with the function code for arming the oscillator. The arm oscillator command consists of the 24-bit command word only (see Figure 9). One other command is also available for use in setting and reading time remaining. A stop oscillator command is given when the command register is

properly loaded with the function code for stopping the oscillator. The stop oscillator command consists of the 24-bit command word only (see Figure 10). This command will only execute prior to issuing a lock command. After the lock command is issued, stop oscillator commands are ignored.

A sequence for properly setting the expiration time of the DS1207 is as follows (see Figure 11). First, program the identification and security match bits to the desired value. Use normal mode operation to write the appropriate secure data. Second, write the number days remaining register to the desired value. This number can be immediately verified by reading the number of days remaining. Next, arm the oscillator by writing the appropriate command. Then do a normal mode read. This action will start the internal oscillator. Now read the 20-bit day clock counter several times to verify that the oscillator is running. After oscillator activity has been verified, issue the stop oscillator command. The lock command should be issued, followed by the arm oscillator command. The TimeKey will start the countdown to expiration on the next access. To guarantee security, a locked TimeKey cannot be unlocked. The key cannot be reprogrammed after expiration. The oscillator verification portion of this sequence is not required and can be deleted when speed in setting time remaining is important.

COMMAND WORD

Each data transfer for normal and program mode begins with a 3-byte command word as shown in Figure 12. As defined, the first byte of the command word specifies the function code. Eight function codes are acceptable (Figure 13). If any one of the bits of the first byte of the command word fails to meet one of the exact patterns for function codes, the data transfer will be aborted.

The first two bits of the second byte of the command word specify whether the data transfer to follow is program or normal mode. The bit pattern for program mode is 0 in bit 0 and 1 in bit 1. The bit pattern for normal mode is a 1 in bit 0 and a 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause the transfer to abort. The program mode can be invoked with one of seven function codes: program identification and security match, read the 20-bit day clock counter, read the number of days count, write the number of days count, lock number of days count, arm oscillator, and stop oscillator.

The remaining six bits of byte 2 and the first four bits of byte 3 must be written to match one of the five patterns as indicated in Figure 12 or data transfer will abort. Under special contract with Dallas Semiconductor, these bits can be defined by the user as any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last four bits of byte 3 of the command word must be written 1011 or data transfer will abort. Table 1 provides a summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The reset input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA at 3.5 volts is required. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the clock cycle. Command bits and data bits are input on the rising edge of the clock. Data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. Data transfer is illustrated in Figure 14 for normal mode and Figure 15 for program mode.

TIMEKEY CONNECTIONS

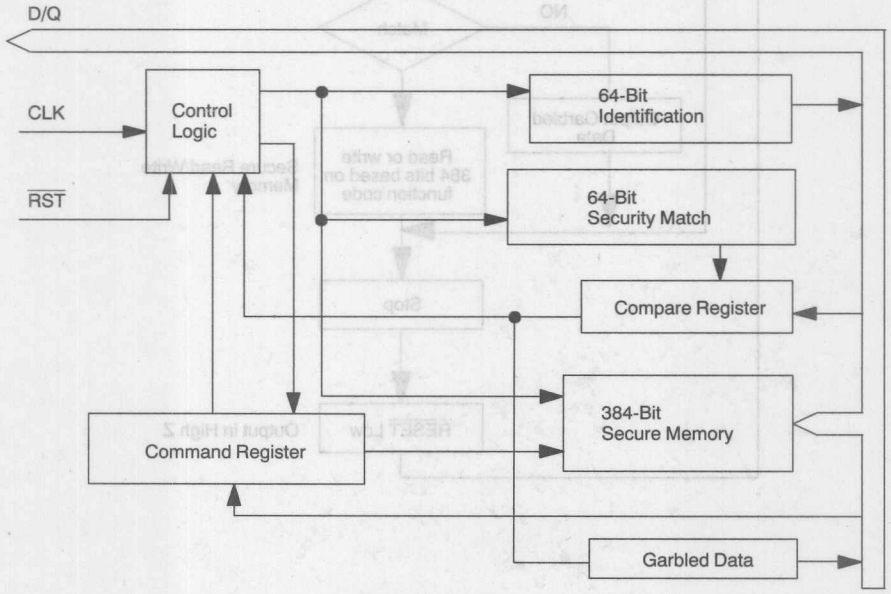
The TimeKey is designed to be plugged into a standard 5-pin 0.1 inch center SIP receptacle. A guide is provided to prevent the TimeKey from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the TimeKey pins can be determined to ensure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DQ all have 20K ohm pulldown resistors to ground that can be sensed by a reading device.

COMMAND WORDS Table 1

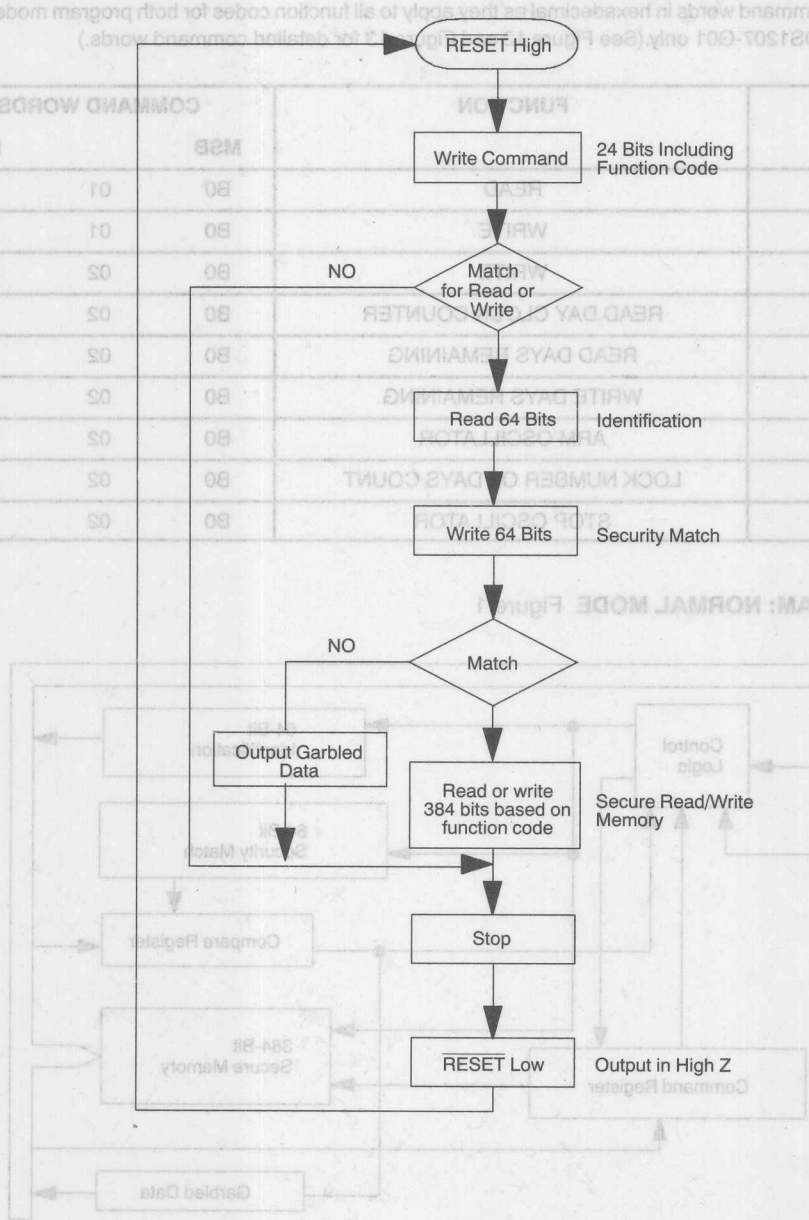
Summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode for the DS1207-G01 only.(See Figure 12 and Figure 13 for detailed command words.)

MODE	FUNCTION	COMMAND WORDS		
		MSB		LSB
NORMAL	READ	B0	01	62
NORMAL	WRITE	B0	01	9D
PROGRAM	WRITE	B0	02	9D
PROGRAM	READ DAY CLOCK COUNTER	B0	02	F1
PROGRAM	READ DAYS REMAINING	B0	02	F3
PROGRAM	WRITE DAYS REMAINING	B0	02	F2
PROGRAM	ARM OSCILLATOR	B0	02	F5
PROGRAM	LOCK NUMBER OF DAYS COUNT	B0	02	F6
PROGRAM	STOP OSCILLATOR	B0	02	F4

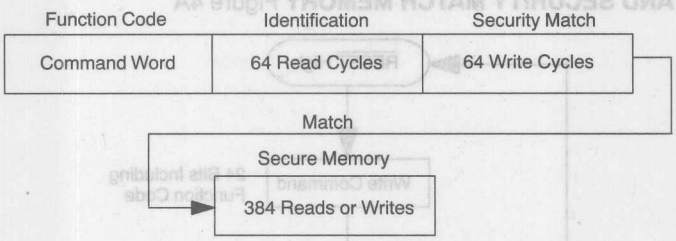
BLOCK DIAGRAM: NORMAL MODE Figure 1



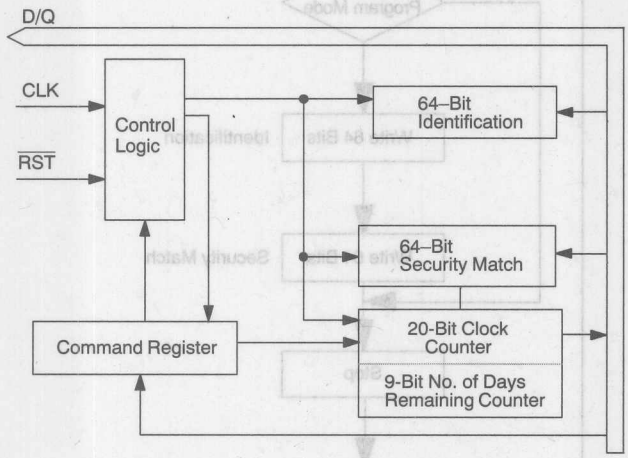
NORMAL MODE: READ OR WRITE SECURE READ/WRITE MEMORY Figure 2A



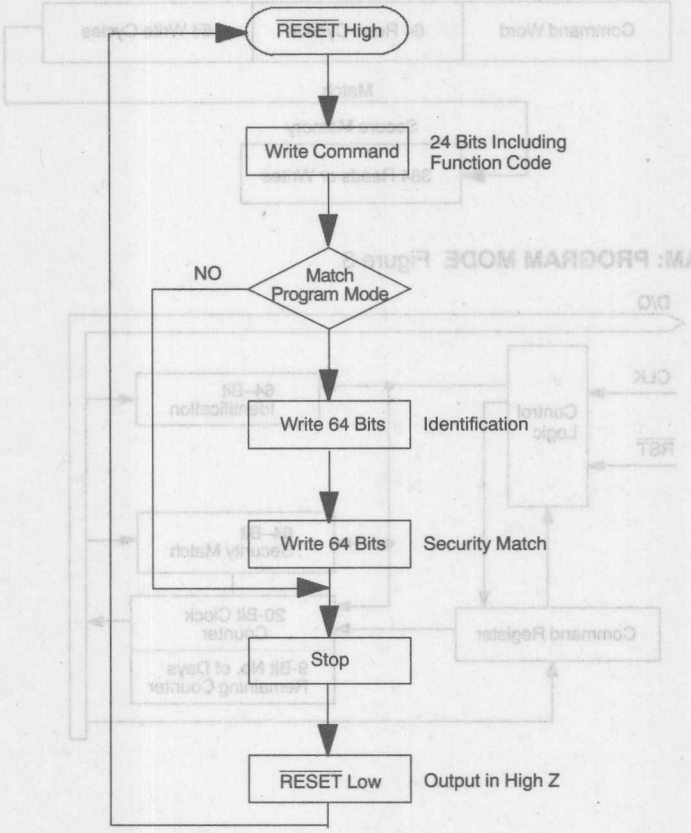
SEQUENCE: NORMAL MODE, READ OR WRITE SECURE MEMORY Figure 2B



BLOCK DIAGRAM: PROGRAM MODE Figure 3



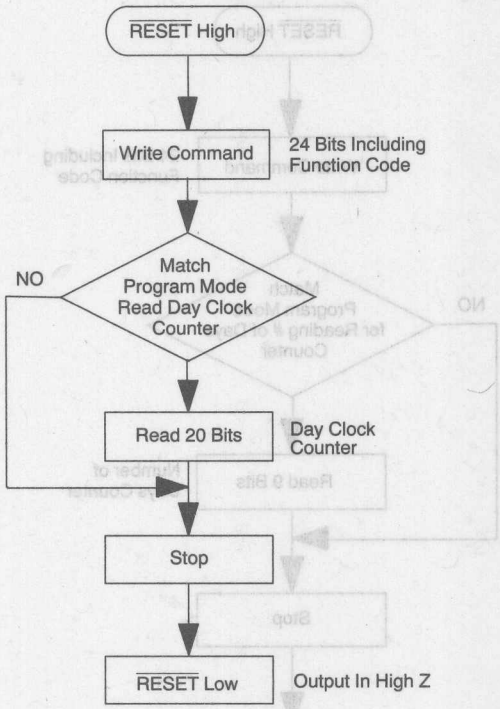
PROGRAM MODE: PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 4A



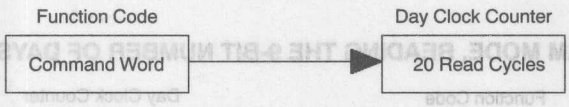
SEQUENCE: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH BITS Figure 4B

Function Code	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

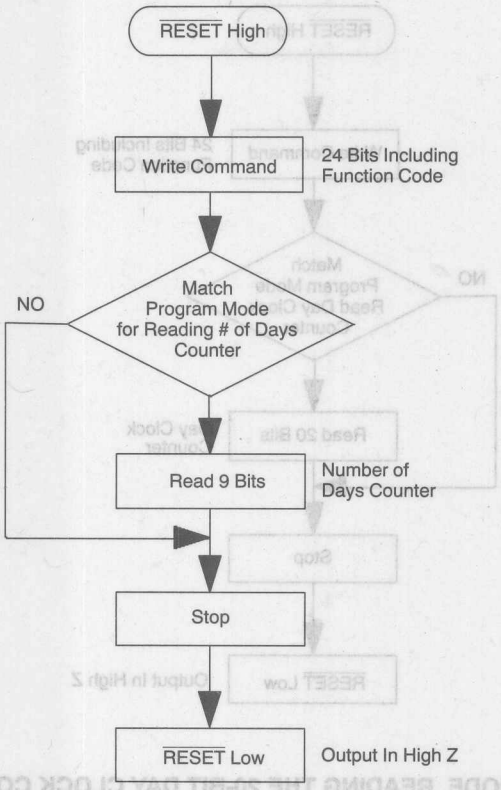
FLOW CHART: PROGRAM MODE, READING THE 20-BIT DAY CLOCK CALENDAR Figure 5A



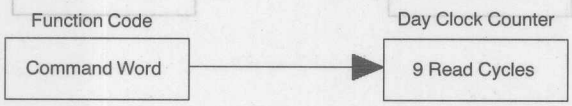
SEQUENCE: PROGRAM MODE, READING THE 20-BIT DAY CLOCK COUNTER Figure 5B



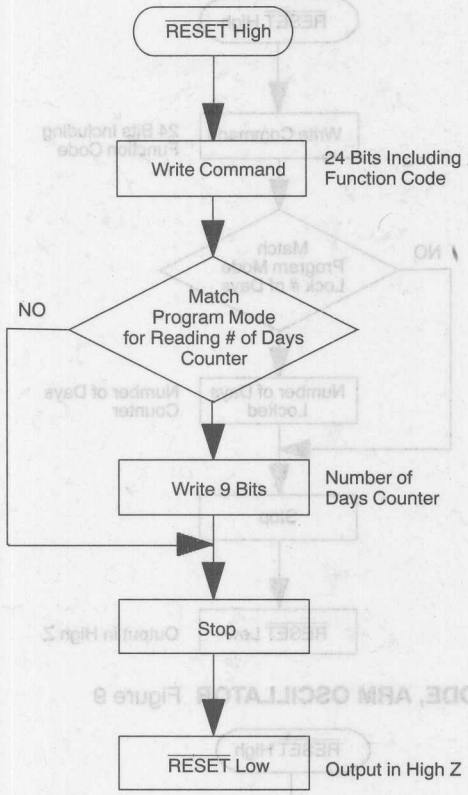
FLOW CHART: PROGRAM, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6A



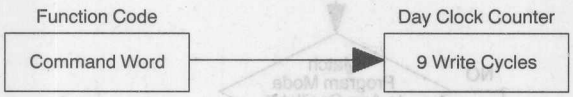
SEQUENCE: PROGRAM MODE, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6B



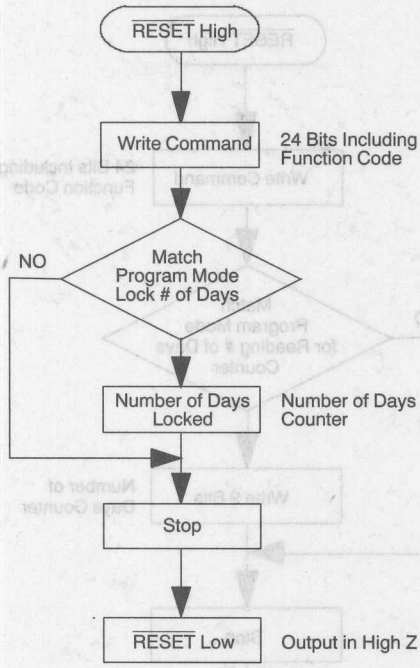
FLOW CHART: PROGRAM MODE, WRITING TO NUMBER OF DAYS COUNTER Figure 7A



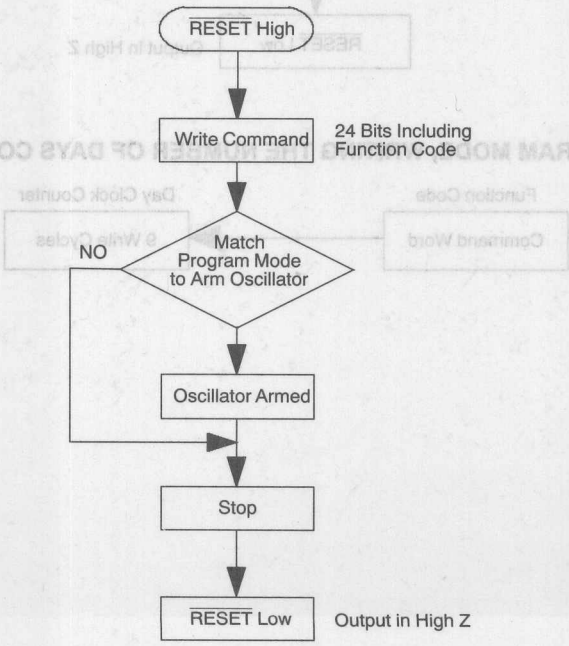
SEQUENCE: PROGRAM MODE, WRITING THE NUMBER OF DAYS COUNTER Figure 7B



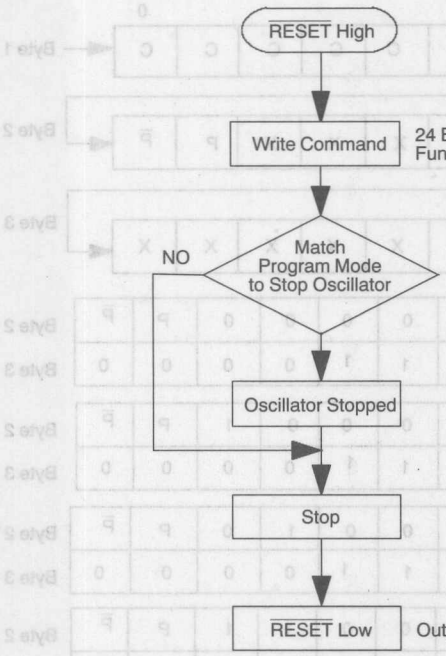
FLOW CHART: PROGRAM MODE, LOCK NUMBER OF DAYS REGISTER Figure 8



FLOW CHART: PROGRAM MODE, ARM OSCILLATOR Figure 9



FLOW CHART: PROGRAM MODE, STOP OSCILLATOR Figure 10

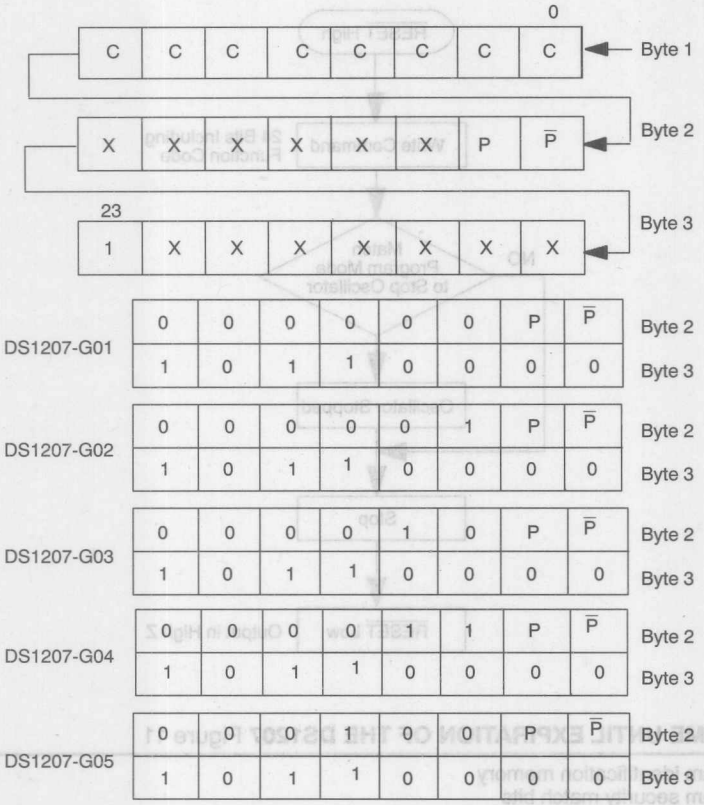


SETTING THE TIME UNTIL EXPIRATION OF THE DS1207 Figure 11

Step 1	Program identification memory Program security match bits Write normal mode secure data
Step 2	Program write the number of days remaining Program read the number of days remaining for verification
Step 3*	Issue arm oscillator command
Step 4*	Do a read of any kind
Step 5*	Program read the day clock counter several times (verify that the oscillator is running)
Step 6*	Issue the stop oscillator command
Step 7	Issue the lock command
Step 8	Issue the arm oscillator command (time of expiration will start on first access)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

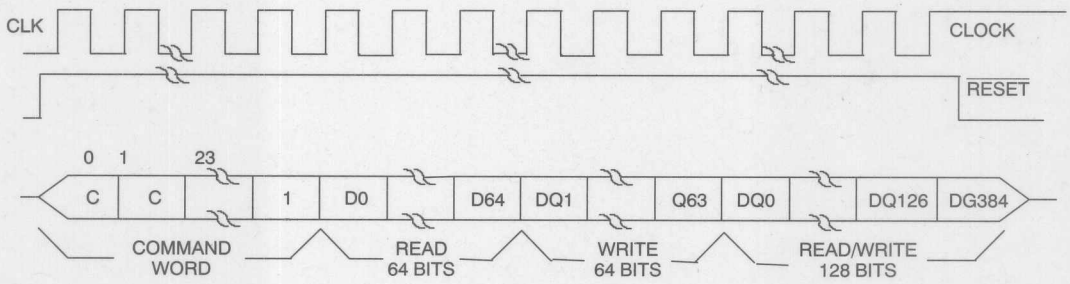
COMMAND WORD Figure 12



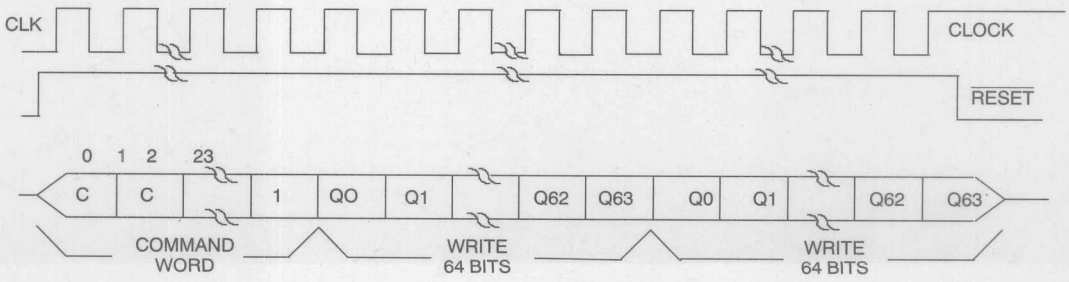
FUNCTION CODES: FIRST BYTE OF COMMAND WORD Figure 13

MSB							LSB	
0	1	1	0	0	0	1	0	READ
1	0	0	1	1	1	0	1	WRITE
1	1	1	1	0	0	0	1	READ DAY CLOCK COUNTER
1	1	1	1	0	0	1	0	WRITE NUMBER OF DAYS REMAINING
1	1	1	1	0	0	1	1	READ NUMBER OF DAYS REMAINING
1	1	1	1	0	1	0	0	STOP OSCILLATOR
1	1	1	1	0	1	0	1	ARM OSCILLATOR
1	1	1	1	0	1	1	0	LOCK NUMBER OF DAYS COUNT

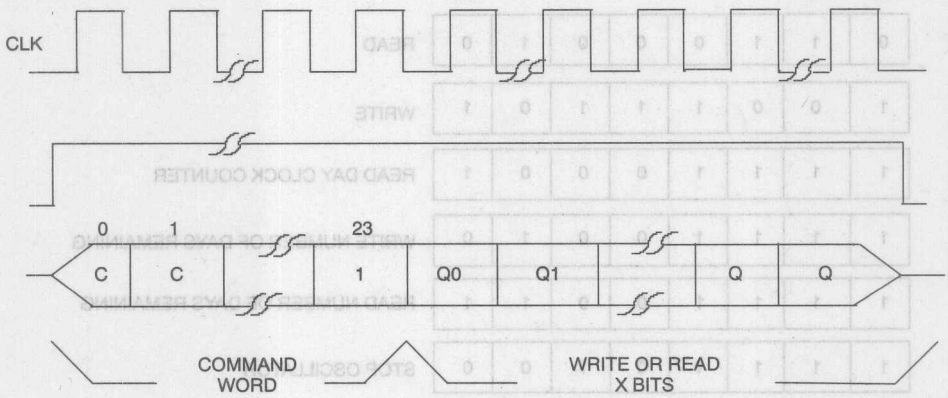
DATA TRANSFER: NORMAL MODE, READ OR WRITE SECURE READ/WRITE MEMORY Figure 14



DATA TRANSFER: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 15A



DATA TRANSFER: PROGRAM MODE, DAY CLOCK, DAYS REMAINING AND OSCILLATOR CONTROL Figure 15B



NOTE: The number of bits which follow the command word will be either 0, 9, or 20 bits based on the function code.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{\text{Reset}}$ Logic 1	V_{IHE}	3.5			V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $\overline{RST}$ = 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	µA	4
Output Leakage	I_{LO}			+500	µA	
Output Current @2.4V	I_{OH}	-1			mA	
Output Current @0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		60	K ohms	
D/Q Input Resistance	Z_{DQ}	10		60	K ohms	
CLK Input Resistance	Z_{CLK}	10		60	K ohms	
$\overline{\text{RST}}$ Current @3.5V	I_{RST}			2	mA	6, 9

CAPACITANCE

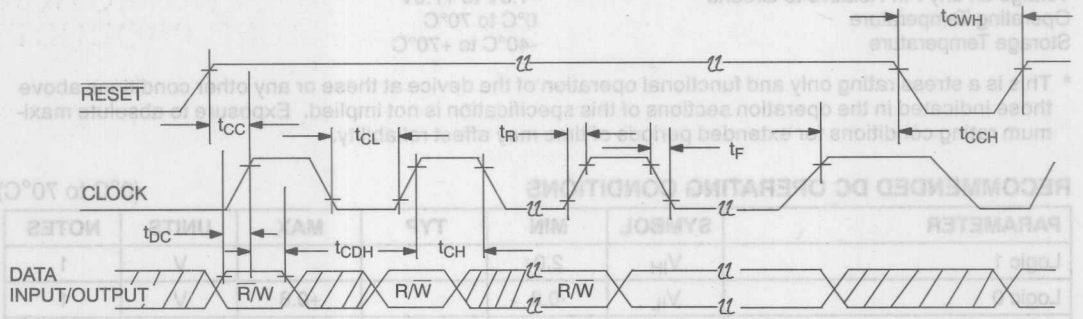
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

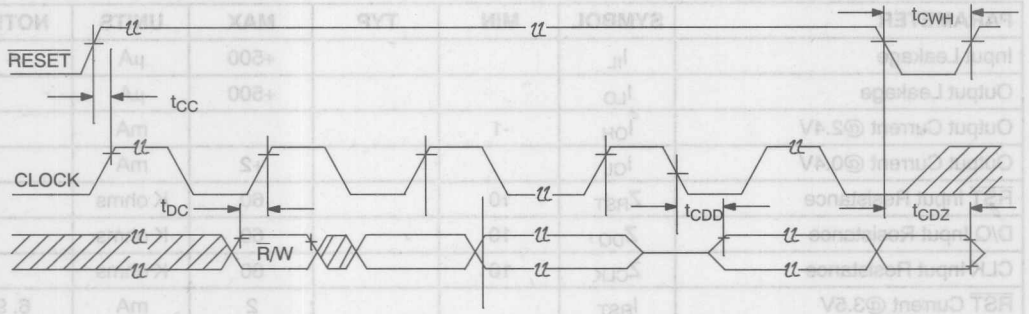
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	50			ns	2, 7
CLK to Data Hold	t_{CDH}	70			ns	2, 7
CLK to Data	t_{CDD}			200	ns	2, 3, 5, 7
CLK Low Time Delay	t_{CL}	250			ns	2, 7
CLK High Time	t_{CH}	250			ns	2, 7
CLK Frequency	f_{CLK}	DC		2.0	MHz	2, 7
CLK Rise & Fall	t_R, t_F			500	ns	2, 7
$\overline{\text{RST}}$ to CLK Setup	t_{CC}	1			µs	2, 7
CLK to $\overline{\text{RST}}$ Hold	t_{CCH}	60			ns	2, 7
$\overline{\text{RST}}$ Inactive Time	t_{CWH}	10			ms	2, 7,
$\overline{\text{RST}}$ To I/O High Z	t_{CDZ}			70	ns	2, 7



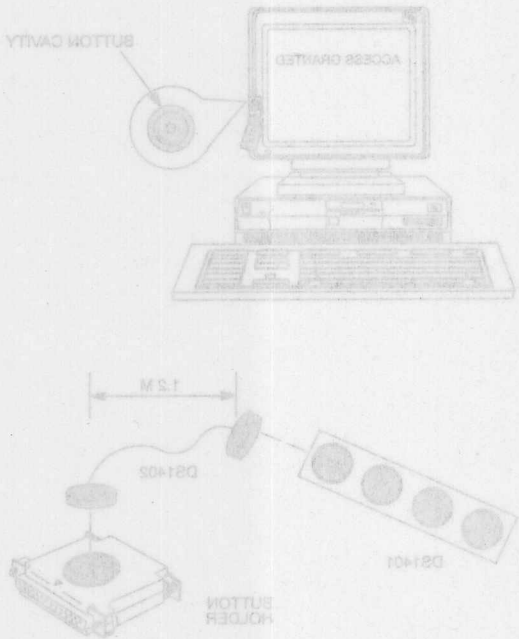
TIMING DIAGRAM: READ DATA



NOTES:

1. All voltages are referenced to GND.
2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
4. For CLK, D/Q, and $\overline{RST}$.
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST}$ greater than or equal to 3.5 volts.
8. Each DS1207 is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
9. Average AC $\overline{RST}$ current can be determined using the following formula:
   $I_{TOTAL} = 2 + I_{LOAD}$ DC + (4 x 10-3)(CL + 280)^{f}
   I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHz.
   Applying the above formula, a load capacitance of 50 pF running at a frequency of 2.0 MHz gives an I_{TOTAL} of 1.6 mA.

SOFTWARE PROTECTION: BUTTON BASED PRODUCTS

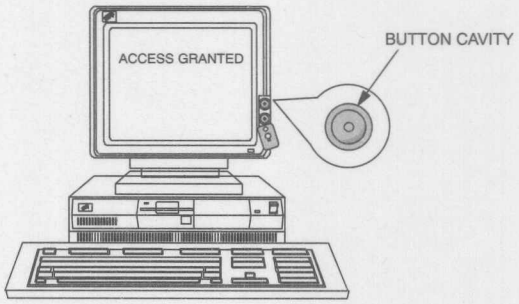


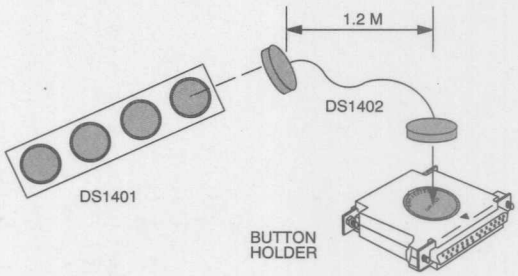
DALLAS SEMICONDUCTOR

DS1401
Front Panel Button Holder
DS1402
Button Cable

FEATURES

- A convenient interface for Buttons
- Can be used with any Dallas Semiconductor Button holder
- Provides from 4 to 24 Button ports (1 port used for Button Cable connection)
- Buttons can be inserted in any combination
- Momentary touch or dwelled contact
- Fastens to any convenient location





DESCRIPTION

Dallas Buttons can now be conveniently accessed using the DS1401 and DS1402.

The DS1401 is connected to the computer using the DS1402 and any Dallas Button Holder (which connects to an I/O port). The DS1401 mounts to any surface (top of tower computer, CRT, keyboard).

The DS1401 supports Dallas' MicroLan architecture, allowing Buttons to be inserted into Button ports in any combination. Each Button's unique 64–bit ID makes location detection automatic.

The DS1401 also supports momentary touch contact with Button ports for applications which do not require a dwelled contact.

Multiple versions of the DS1401 are available to provide 4 to 24 Button ports.

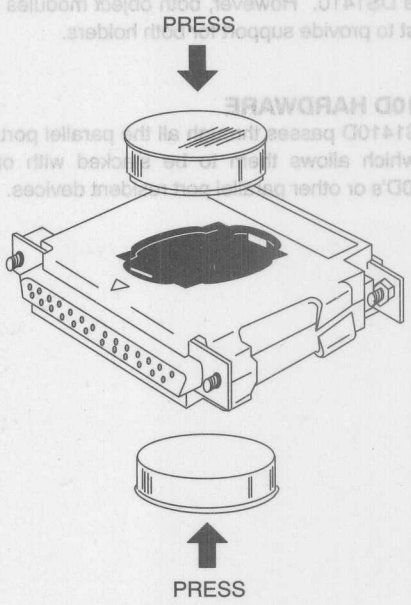
DALLAS SEMICONDUCTOR

DS1410D
Parallel Port Button Holder

FEATURES

- Provides a parallel port interface for Dallas Buttons
- No external power required
- Coexists with other parallel port resident products
- Operates with DOS, OS/2, Windows, PC Based–UNIX, Windows NT, QNX
- Used to protect applications installed on a system

DS1410D BUTTON HOLDER



DESCRIPTION

The DS1410D Parallel Port Button Holder interfaces Dallas Semiconductor Authorization Buttons to host computers via a PC parallel port. In conjunction with the Buttons, the DS1410D provides a high security storage vault for critical execution control information. Only users that possess a Button can utilize the software, preventing execution of unauthorized copies.

The modularity of the DS1410D allows for easy feature customization. The device supports the insertion of two Buttons, which can be removed and replaced to vary functionality.

For example, a DS1427 Time Button can be programmed for a 30 day expiration, issued with a DS1410D, and a software copy. The evaluator can be converted into a registered user by issuing a DS1425 Button and inserting it into the second receptacle.

The DS1410D supports the same Buttons as other Dallas Button Holders. This allows standardization of any protection scheme across virtually all hardware platforms, regardless of the operating system. The Buttons remain constant, and the Button holders change according to the specific platform interface.

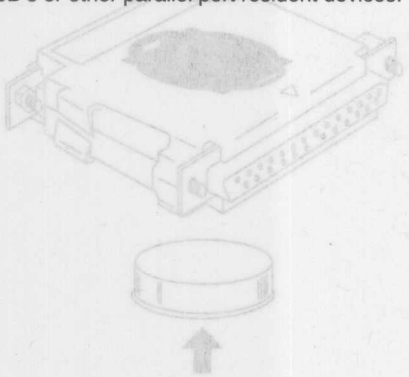
DS1410D SOFTWARE

The DS1410D Development Kit contains access system software which must be linked with the application software in order to complete integration. The support for the application development environments and operating systems lies in the interface software of the access system. The access system contains the low level interface for communicating with the Buttons.

NOTE: The DS1410D is not object code compatible with the DS1410. However, both object modules can co–exist to provide support for both holders.

DS1410D HARDWARE

The DS1410D passes through all the parallel port I/O lines, which allows them to be stacked with other DS1410D's or other parallel port resident devices.



The DS1410D attaches directly to the PC parallel port. If use of a printer is desired, the DS1410D should reside between the parallel port and the printer cable. With system and printer both off, simply plug the 25–pin male D connector side of the DS1410D into the PC parallel port and then plug the printer cable into the 25–pin female D connector side of the DS1410D. The top and bottom screws that reside on the DS1410D and the printer cable should then be tightened accordingly.

Attaching another parallel port device is not required to operate the DS1410D.

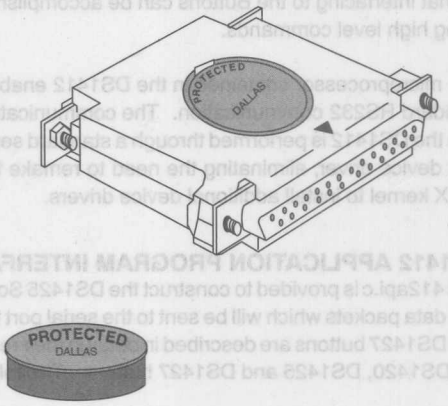
To cascade DS1410D's, simply follow the same directions as above, inserting DS1410D 25–pin D male and female connectors accordingly.

DALLAS SEMICONDUCTOR

DS1412
Serial Port Button Holder

FEATURES

- RS232 interface for Dallas Buttons
- No external power required
- API included
- No gender changers needed
- Multiplatform Support



DESCRIPTION

The DS1412 Serial Port Button Holder interfaces Dallas Semiconductor Authorization Buttons to host computers via an RS232 serial port. In conjunction with the Buttons, the DS1412 provides a high security storage vault for critical license management and execution control information. Only users that possess a Button can utilize the software, preventing execution of unauthorized copies.

The modularity of the DS1412 allows for easy feature customization. The device supports the insertion of one Button, which can be removed and replaced with another Button of different functionality.

For example, a DS1427 Time Button can be programmed for 30 day expiration, issued with a DS1412, and an evaluation software copy. Upon expiration, the evaluator can be converted into a registered user simply by issuing a DS1425 Button.

The DS1412 supports the same Buttons as other Dallas Button holders. This allows standardization of any protection scheme across virtually all hardware platforms, regardless of the operating system. The Buttons remain constant, and the Button holders change according to the specific platform interface.

DS1412 SOFTWARE

The DS1412 Development Kit contains an object file which must be linked with the application software in order to complete integration. This object file contains the low level interface for communicating with the DS1412.

An Application Programming Interface (API) has been provided as part of the DS1412 development software so that interfacing to the Buttons can be accomplished using high level commands.

The microprocessor contained in the DS1412 enables standard RS232 communication. The communication with the DS1412 is performed through a standard serial port device driver, eliminating the need to remake the UNIX kernel to install additional device drivers.

DS1412 HARDWARE

The DS1412 will integrate without modification onto different host computers, especially where their is no gender uniformity. One end of the DS1412 is a male connector and the other a female. Choose the proper end accordingly, connect to the serial port of the host, and the DS1412 will operate properly.

NOTE: The DS1412 requires a dedicated serial port regardless of which end is connected to the host.

A red label has been provided which should be affixed to the end the DS1412 not in use. This will ensure that no one attempts to connect another serial port device (a modem for example) in line with the DS1412.

DS1412 APPLICATION PROGRAM INTERFACE

DS1412api.c is provided to construct the DS1425 Software Key and DS1427 Time Key specific command structures and data packets which will be sent to the serial port transfer layer called sportio (serial port I/O). Note: The DS1425 and DS1427 buttons are described in detail in their respective data sheets. The *take_census function is available for the DS1420, DS1425 and DS1427 buttons. The following function is provided in DS1412api.c.

uchar *take_census (uchar *num_pres)

This function reads the ROM Data from all of the DOW (Dallas 1–wire) parts present on the 1–wire bus of the DS1412. take_census returns a pointer to the beginning of the buffer containing the ROM Data. num_pres indicates the number of DOW parts found during the census. If num_pres == 0 the structure DS1412_comm (described below) should be examined to determine the cause of the failure.

Please note that for many of the functions described below, a true result only implies that the data you specified was sent the proper button. For example, if read_subkey is called with an incorrect password in the key_dta array, the multikey button will send back incorrect secure data. However, read_subkey will return true (providing a DS1412 and button are present) as nobody but the caller has any way of knowing if the password and secure data are correct. To verify any data write or transfer the user can simply call the appropriate read function.

Please consult the button data sheets for details on their use.

DS1425 SPECIFIC FUNCTIONS

The following functions are available for communication with a DS1425 button. For more information on the features of the button itself please refer to the DS1425 data sheet. Example programs and details of functions are provided in the documentation and example program provided with the API software.

uchar read_subkey (uchar key_num, uchar *key_dta, uchar *rom_ptr)

This function reads the secure subkey specified by key_num of the DS1425 with ROM Data pointed to by rom_ptr. key_dta points to a 64 byte field constructed as follows:

bytes 0–7 : ID field
bytes 8–15 : password field bytes
bytes 16–63 : secure data field

Upon successful completion, read_subkey returns true, and the ID and secure data fields are overwritten with data from the key (the password field is left untouched as it is write only memory in the DS1425). If the function fails for any reason, read_subkey returns false. A structure defined below will specify the reason for the failure condition.

uchar write_subkey (uchar key_num, uchar *key_dta, uchar *rom_ptr)

This function writes to the secure subkey, specified by key_num, of the DS1425 with ROM Data pointed to by rom_ptr. The data sent to the part is taken from the field pointed to by key_dta. Upon successful completion, write_subkey returns true. If the function fails for any reason write_subkey returns false.

uchar read_1425_sp (uchar *scr_dta, uchar *rom_ptr)

This function reads the scratchpad of the DS1425 with ROM Data pointed to by rom_ptr. Upon successful completion read_1425_sp returns true with the 64 byte field pointed to byte scr_dta (this is simply a homogenous field of Read/ Write memory) overwritten with the scratchpad data from the selected DS1425. Any failure will result in read_1425_sp returning false.

uchar write_1425_sp (byte *scr_dta, byte *rom_ptr)

This function writes the scratchpad of the DS1425 with ROM Data pointed to by rom_ptr. The data sent to the part is taken from the field pointed to by scr_dta. Upon successful completion write_1425_sp returns true. Any failure will result in write_1425_sp returning false.

uchar reprogram_subkey (uchar key_num, uchar *key_dta, uchar *rom_ptr)

This function reprograms the subkey (specified by key_num) of the DS1425 with ROM Data pointed to by rom_ptr. The first 8 bytes of the key_dta array should contain the old ID field of the subkey to be reprogrammed. The second 8 bytes should contain the new ID, and the next eight bytes should hold your new password for the subkey. Upon successful completion reprogram_subkey returns true. Please note that a true result only implies the data was sent to the correct DS1425. To reprogram the subkey, the old ID field you pass this function must match that of the specified subkey in the DS1425. Any failure will result in reprogram_subkey returning false.

uchar move_block (uchar key_num, uchar *key_dta, uchar *rom_ptr, uchar blocknum)

This function performs the move block command of the DS1425 with ROM Data pointed to by rom_ptr. blocknum is a value from 0 to 8 which specifies the block to be transferred from the scratchpad, to the secure subkey number specified by key_num. The second 8 byte field of key_dta must contain the 8 byte password field which is required by the DS1425 for any block transfer. Upon successful completion move_block returns true. Please note that this does not imply that the move block occurred within the DS1425. If the password was incorrect the move block will be terminated by the DS1425. All successful completion guarantees is that the DS1425 received the specified data. Any failure will result in move_block returning false.

DS1427 SPECIFIC FUNCTIONS

The following functions are available for communication with a DS1427 button. For more information on the features of the button itself please refer to the DS1427 data sheet. Example programs and details of functions are provided in the documentation and example program provided with the API software.

uchar read_1427_smem (uchar *smem_dta, uchar *rom_ptr, uchar page_num)

This function reads the secure memory page (specified by page_num), of the DS1427 with ROM data pointed to by rom_ptr. smem_dta is a pointer to a 32 byte block of memory which will receive the secure memory data read from the DS1427. Upon successful completion read_1427_smem returns true, otherwise it returns false.

uchar read_1427_sp (uchar *scr_dta, uchar *rom_ptr)

This function reads the scratchpad of the DS1427 with ROM data pointed to by rom_ptr. The data read is stored beginning at the location pointed to by scr_dta. The first three bytes will receive the authorization code required for a copy scratchpad (described below). The next 32 bytes will be the scratchpad data just read. Upon successful completion read_1427_sp returns true, otherwise it returns false.

uchar write_1427_sp (uchar *scr_dta, uchar *rom_ptr, uchar page_num)

This function writes the scratchpad of the DS1427 with ROM data pointed to by rom_ptr. The data written to the scratchpad is taken starting with the byte pointed to by rom_ptr. page_num specifies which page you want this data copied to via a copy scratchpad command. Upon successful completion write_1427_sp returns true, otherwise it returns false.

uchar copy_1427_sp (uchar *auth_code, uchar *rom_ptr)

This function copies the contents of the scratchpad, with ROM Data pointed to by rom_ptr, to the secure memory starting at an address specified by the authorization code (first three bytes received from a read scratchpad). Remember that to set any of the write protect bits in the clock page (page #16), the copy scratchpad must be performed three times. After the first copy the AA bit is set. This means that the authorization code changes. The scratchpad can be read again, or you can set that bit in the authorization code to save time. Upon successful completion copy_1427_sp returns true, otherwise it returns false.

```
typedef struct
{
    char tty_name[20]
    uchar setup_error;
    uchar driver_open_error
    uchar ioctl_error
    uchar no_DS1412;
    uchar no_button;
    uchar mem_err;
}
DS1412_struct;

DS1412_struct DS1412_comm;
```

DS1412_comm: Contains fields used to examine error conditions and specify which tty driver is to be used to communicate with the DS1412.

tty_name: Copy the name of the tty driver for sportio to use for communication with the DS1412 in this field (i.e. /dev/ttya to use the serial port A on a SUN).

setup_error: This field is currently unused.

driver_open_error: If this field is true (1) tty_name is most likely invalid.

ioctl_error: If this field is true (1) an error occurred getting/setting the tty drivers parameters. This is not likely if tty_name is correct.

no_DS1412: This field is true (1) if no DS1412 was found on the serial port.

no_button: This field is true (1) if either no DS1412 was found, or if a DS1412 is present but contains no buttons. If no_DS1412 is false (0), and no_button is true (1) prompt the user to insert a button.

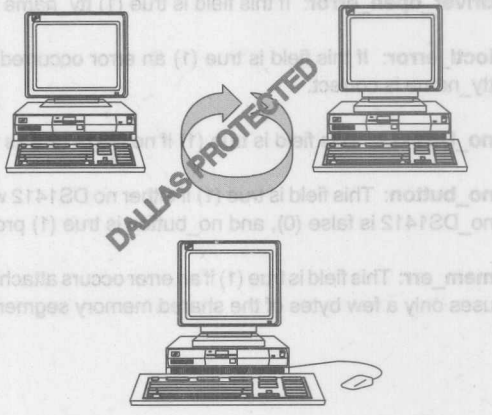
mem_err: This field is true (1) if an error occurs attaching a shared memory segment. This is unlikely because sportio uses only a few bytes of the shared memory segment, and detaches the segment quickly.

DALLAS SEMICONDUCTOR

DS1414
Network Button Holder

FEATURES

- Parallel port interface for Buttons
- No external power required
- One device required per network
- Operates with third party license management software
- Protects multiple applications
- Updates license transparently



DESCRIPTION

The DS1414 Network Button Holder interfaces Dallas Semiconductor Authorization Buttons to host computers via a parallel port. The combination provides a high security storage vault for critical license management and execution control information.

The DS1414 can be placed on a server or any client on the network. If placed on the server, no additional communication software is necessary on the clients. The server software and API (both provided in the development kit) work together to allow individual client sessions to be authenticated from the central server.

One major advantage of the DS1414 is the ability to update Buttons. The update procedure can be performed transparent to the end user, as a natural extension of the software update process. This simplifies the task of adding users, software options or new applications, while maintaining a complete audit trail.

The DS1414 supports the same Buttons as other Dallas Button holders. Standardize your single user and network software protection scheme across virtually all hardware platforms, regardless of the operating system. The Buttons remain constant, and the Button holders change according to the specific platform interface.

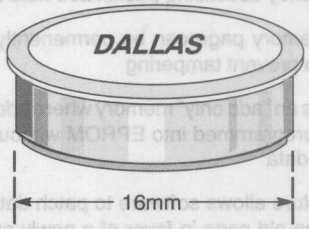
DALLAS SEMICONDUCTOR

DS1420
Serial ID Button

FEATURES

- Provides a unique 64–bit serial number
- No external power required
- Uses inexpensive 1–wire protocol
- Universally portable across platforms

PACKAGE OUTLINE



DESCRIPTION

Authorization Buttons are sophisticated microelectronics, sealed into miniature stainless steel cans, creating a low cost, portable medium for storing and controlling access to sensitive information.

Buttons are used with Button Holders as a hardware based protection system for software. Buttons help protect the right to copy software by actually protecting the right to execute it. Software can now be locked to a user, a machine, or an application with a complete audit trail and guaranteed uniqueness.

The DS1420 is a Button that provides a 64–bit unique ID number, and is typically used to uniquely identify a person or a machine.

Hardware communication with Buttons is conducted via a 1–wire interface. The conversion from a PC I/O port to the 1–wire interface is the responsibility of the Button Holder.

Software applications communicate with the Button using Dallas' Access System, which is contained in any of the Button Holder Developer's kits. The Access System provides software developers with easy to use commands which are embedded into the application in order to utilize the Button resources during run time.

For more information on the Access System, please reference any of the Button Holder data sheets.

Each Dallas Button is uniquely serialized with a 64–bit code that is laser–etched in the silicon. This unique ID provides a basic level of security, is traceable in the field, and makes it possible to identify the specific Button in a field of many.

The serial number is divided into three parts (see Figure 1). The 8–bit family code tells the Access System (and consequently the developer) what type of Button is being used. The next 48 bits are lasered sequentially with no two numbers the same. The last 8 bits contain a Cyclic Redundancy Check (CRC) value that has been calculated across the family code and the 48–bit serial number. The CRC ensures that Button communication is error free.

SERIAL NUMBER ORGANIZATION Figure 1

		FAMILY CODE 82H
8-BIT CRC CODE	48-BIT SERIAL NUMBER NUMBER	10000001

MSB

PRODUCT PREVIEW

DALLAS SEMICONDUCTOR

DS1422
1Kbit Add–Only UniqueWare Button

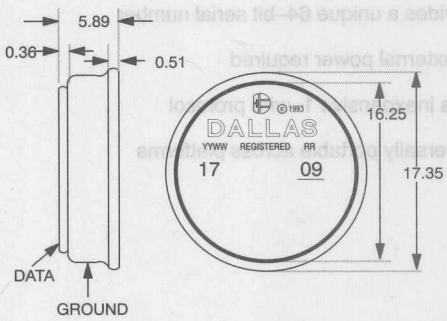
SPECIAL FEATURES

- 1024–bits Electrically Programmable Read Only Memory (EPROM) partitioned into four 256–bit pages for randomly accessing packetized data records
- Each memory page can be permanently write–protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reads over a wide voltage range of 2.8V to 6.0V from –40°C to +85°C; programs at 11.5V ± 0.5V from –40°C to +85°C

COMMON BUTTON FEATURES

- Unique, factory–lasered 64–bit identification number
- Communicates at 16.3Kbits per second
- Standard 16 mm diameter and 1–Wire protocol ensure compatibility with Button family
- Steel case withstands harsh environments
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations

F5 MICROCAN™

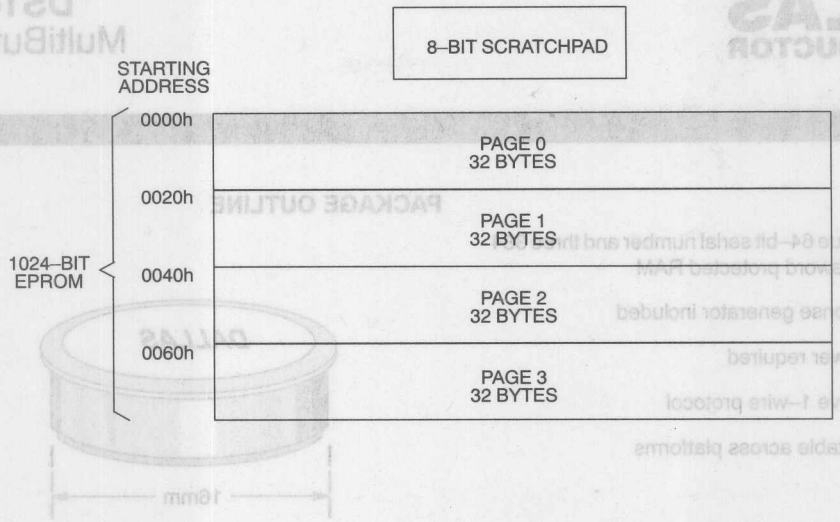


DESCRIPTION

The DS1422 UniqueWare Button is an add only alternative to the static RAM based DS1425 and DS1427 Buttons. The DS1422 consists of a factory–lasered 64 bit identification number plus 1Kbit of EPROM, which is user–programmable. The power to program and read the DS1422 is derived entirely from the 1–Wire communication line. Data is transferred serially via the 1–Wire protocol. The entire device can be programmed and then write–protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a standalone database.

The DS1422 can be programmed with unchangeable information (perhaps a division, location or family code of the applications origin) and used to maintain update and version control information, tied to a unique identification number. Audibility becomes a snap by reading the history of the software's distribution, customized for each installation of your software.

DS1422 MEMORY MAP Figure 1



EPROM STATUS BYTES

ADDRESS:	0007h (MSB)	0006h	0005h	0004h	0003h	0002h	0001h	0000h (LSB)
	7	6	5	4	3	2	1	0
	FACTORY–PROGRAMMED 00h	RESERVED FOR FUTURE EXPANSION		PAGE ADDRESS REDIRECTION BYTE FOR PAGE 3	PAGE ADDRESS REDIRECTION BYTE FOR PAGE 2	PAGE ADDRESS REDIRECTION BYTE FOR PAGE 1	PAGE ADDRESS REDIRECTION BYTE FOR PAGE 0	BIT 0 = WRITE PROTECT PAGE 0 BIT 1 = WRITE PROTECT PAGE 1 BIT 2 = WRITE PROTECT PAGE 2 BIT 3 = WRITE PROTECT PAGE 3 BIT 4–7 = RESERVED

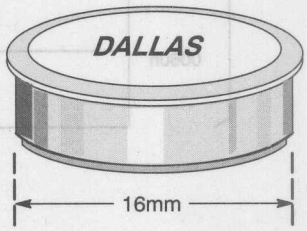
DALLAS SEMICONDUCTOR

DS1425
MultiButton

FEATURES

- Provides a unique 64–bit serial number and three 384 bit fields of password protected RAM
- Intelligent response generator included
- No external power required
- Uses inexpensive 1–wire protocol
- Universally portable across platforms

PACKAGE OUTLINE



DESCRIPTION

Authorization Buttons are sophisticated microelectronics, sealed into miniature stainless steel cans, creating a low cost, portable medium for storing and controlling access to sensitive information.

Buttons are used with Button Holders as a hardware based protection system for software. Buttons help protect the right to copy software by actually protecting the right to execute it. Software can now be locked to a user, a machine, or an application with a complete audit trail and guaranteed uniqueness.

The DS1425 provides a 64–bit unique ID number, and three 384 bit fields of password protected RAM. The DS1425 is used to provide nested levels of protection, or to protect multiple applications.

Hardware communication with the Buttons is conducted via a 1–wire interface. The conversion from a PC I/O port to the 1–wire interface is the responsibility of the Button Holder.

Software applications communicate with the Button using Dallas' Access System, which is contained in any of the Button Holder Developer's kits. The Access System provides easy to use commands which are embedded into the application in order to utilize the Button resources during run time.

Each Dallas Button is uniquely serialized with a 64–bit code that is laser–etched in the silicon. This unique ID provides a basic level of security, is traceable in the field, and makes it possible to identify the specific Button in a field of many.

The serial number is divided into three parts (see Figure 1). The 8–bit family code tells the Access System (and consequently the developer) what type of Button is being used. The next 48 bits are lasered sequentially with no two numbers the same. The last 8 bits contain a Cyclic Redundancy Check (CRC) value that has been calculated across the family code and the 48–bit serial number. The CRC ensures that Button communication is error free.

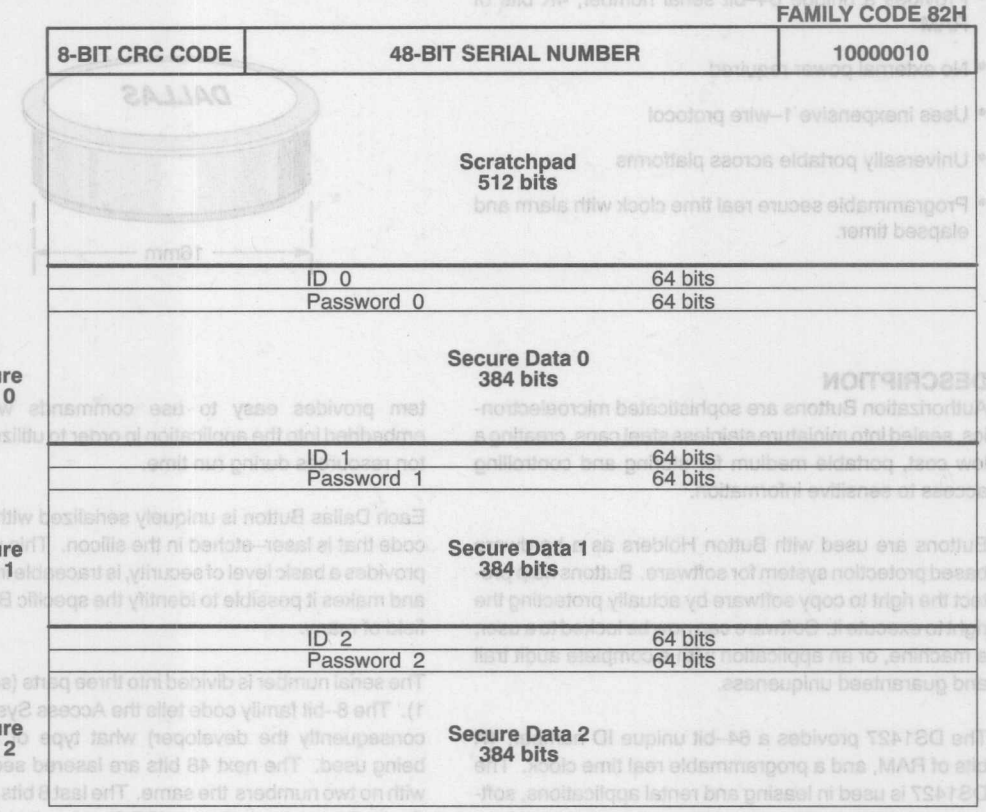
High levels of security are achieved by storing application code and/or data necessary for execution in the Button memory.

Each 384–bit secure data area is prefaced by a 64–bit identification field and an unreadable 64–bit password. Note that this password is user selected and programmed. This means no one, including Dallas Semiconductor, can access that data.

If the DS1425 is presented with a valid password from the host application, the contents of the secure data will be returned. However, if the DS1425 is presented with an invalid password, the on–board intelligent response generator will return what seems to be a normal response, but is not. The false response will be unique to the false access.

By using seemingly random data in both the password and secure data fields, and by generating many false accesses for each valid access, even sophisticated attackers are defeated.

DS1425 MULTIBUTTON ORGANIZATION Figure 1



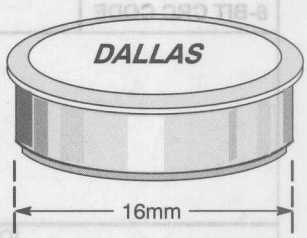
DALLAS SEMICONDUCTOR

DS1427
Time Button

FEATURES

- Provides a unique 64–bit serial number, 4K bits of RAM
- No external power required
- Uses inexpensive 1–wire protocol
- Universally portable across platforms
- Programmable secure real time clock with alarm and elapsed timer.

PACKAGE OUTLINE



DESCRIPTION

Authorization Buttons are sophisticated microelectronics, sealed into miniature stainless steel cans, creating a low cost, portable medium for storing and controlling access to sensitive information.

Buttons are used with Button Holders as a hardware based protection system for software. Buttons help protect the right to copy software by actually protecting the right to execute it. Software can now be locked to a user, a machine, or an application with a complete audit trail and guaranteed uniqueness.

The DS1427 provides a 64–bit unique ID number, 4K bits of RAM, and a programmable real time clock. The DS1427 is used in leasing and rental applications, software metering, and to vary valid protection keys by time. Ability to distribute demonstration software that expire on a date controlled by the deliverer.

Hardware communication with the Buttons is conducted via a 1–wire interface. The conversion from a PC I/O port to the 1–wire interface is the responsibility of the Button Holder.

Software applications communicate with the Button using Dallas' Access System, which is contained in any of the Button Holder Developer's kits. The Access System provides easy to use commands which are embedded into the application in order to utilize the Button resources during run time.

Each Dallas Button is uniquely serialized with a 64–bit code that is laser–etched in the silicon. This unique ID provides a basic level of security, is traceable in the field, and makes it possible to identify the specific Button in a field of many.

The serial number is divided into three parts (see Figure 1). The 8–bit family code tells the Access System (and consequently the developer) what type of Button is being used. The next 48 bits are lasered sequentially with no two numbers the same. The last 8 bits contain a Cyclic Redundancy Check (CRC) value that has been calculated across the family code and the 48–bit serial number. The CRC ensures that Button communication is error free.

The DS1427 tracks elapsed time from either initial programming or from first access by the application software. All timers and alarms can be locked from reprogramming, so that the time base is not compromised in any way.

Memory is organized into 16 pages of 256 bits each. An additional scratch page is provided to validate data before it is written into storage areas.

There are four function commands to address the memory. Three commands are used to read, write, or copy data to or from the scratch page and the storage areas accordingly. All data is written to the scratch page first, verified, and then copied to the appropriate storage locations. The fourth command is used to read the contents of the storage locations, the clock, elapsed timer, alarm registers, or the configuration/status registers.

The real time clock keeps time in 1/256 second increments. This can be translated into seconds, minutes, days, months or years. A read of the clock will return the number of seconds after the reference date. The elapsed timer can be stopped or started based on the contents of the configuration registers.

The configuration and status registers control the operating mode of the DS1427. Setting alarms and controlling interrupts for the clock and elapsed timer are user selectable. Additional registers are used to control the clock oscillator, elapsed timer triggers, and to provide write protection for various memory locations.

DS1427 TIME BUTTON ORGANIZATION Figure 1

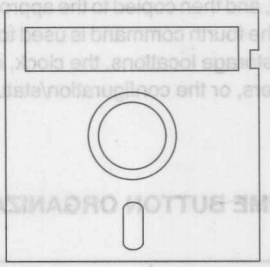
8-BIT CRC CODE	48-BIT SERIAL NUMBER	FAMILY CODE 10000100
MSB 0000h 01FFh	512 Bytes NV SRAM 16 Pages 32 Bytes per Page	
0200h 0201h	Configuration and Status Registers	
0202h 0206h	Real Time Clock	
0207h 020Bh	Elapsed Timer	
020Ch 020Fh	Reserved	
0210h 0214h	RTC Alarm	
0215h 0219h	Elapsed Time Alarm	
021Ah 021Dh	Reserved	

DALLAS SEMICONDUCTOR

DS1410K
Parallel Holder Developer's Kit

INCLUDES:

- DS1410 Button holder
- DS1420 ID Button
- DS1425 MultiButton
- DS1427 Time Button
- Software diskette
- Product data sheets
- Customer registration form



DESCRIPTION

The DS1410K Developer's Kit contains all the software and hardware necessary to complete integration of the DS1410 Button Holder and corresponding Buttons into an application.

The software diskette provided contains an object file (called the Access System), which must be linked with the application code to provide the communication path between the host and the DS1410.

Documentation and examples in a variety of programming languages are also provided on the diskette for reference. The DS1410 supports DOS, OS/2, Windows, and PC–UNIX operating systems.

The kit also provides three different Buttons and a DS1410 Button holder. No other software or hardware is necessary to move into production. Simply choose the Button(s) according to your scheme, link the object file with the application code, and purchase additional Buttons and holders on an as needed basis.

NOTE: This kit can also be used to develop applications for the DS1405 Authorization Module and DS1407 Timed Authorization Module. The DS1405 is a sealed unit version of the DS1410 and DS1425 combination, and the DS1407 is a sealed unit version of the DS1410 and DS1427.

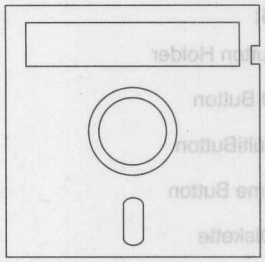
A Customer Registration Form is provided for easy access to free upgrades and discounts on the purchase of other Dallas Authorization Developer's kits.

DALLAS SEMICONDUCTOR

DS1412K
Serial Holder Developer's Kit

INCLUDES:

- DS1412 Button holder
- DS1420 ID Button
- DS1425 MultiButton
- DS1427 Time Button
- Software diskette
- Product data sheets
- Getting started tutorial
- Customer registration form



DESCRIPTION

The DS1412K Developer's Kit contains all the software and hardware necessary to complete integration of the DS1412 Serial Button Holder and corresponding Buttons into an application.

The software diskette provided contains an object file (the control layer), which must be linked with the application code to provide the communication path between the host and the DS1412.

Calls used to check authentication during operation are made to the control layer from the application code via an Application Programming Interface.

The DS1412 supports SUN O/S (for SPARC Stations), HP–UX, AIX (for RS6000), UnixWare, and PC–UNIX operating systems.

The kit also provides three different Buttons and a DS1412. No other software or hardware is necessary to move into production. Simply choose Button(s) according to your scheme, link the object file with the application code, and purchase additional Buttons and holders on an as needed basis.

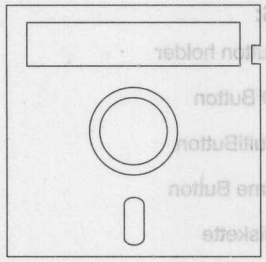
A Customer Registration Form is provided for easy access to free upgrades and discounts on the purchase of other Dallas Authorization Developer's kits.

DALLAS SEMICONDUCTOR

DS1414K
Network Holder Developer's Kit

INCLUDES:

- DS1414 Button Holder
- DS1420 ID Button
- DS1425 MultiButton
- DS1427 Time Button
- Software Diskette
- Product Data Sheets
- Getting Started Tutorial
- Customer Registration Form



DESCRIPTION

The DS1414K Developer's Kit contains all the hardware and software necessary to complete integration of the DS1414 Network Button holder and corresponding Buttons into LAN server based applications.

The software diskette contains an Application Programming Interface which provides high–level communication between applications and Buttons.

The kit also offers run time software which provides rudimentary routines for implementing a simple server based license manager. More sophisticated license management needs can be met by using third party software compatible with Buttons. Call Dallas Semiconductor for a current list of supported license server vendors.

The DS1414 is connected to the parallel port of the LAN server. Only one DS1414 is required to protect all applications serviced by the LAN server hosting the device.

The kit also contains a customer registration form for easy access to free upgrades and discounts on other Dallas Semiconductor Developer's kits.

I. LASER ROM

A. General Information

A major feature of Dallas Semiconductor 1–Wire products is the laser engraved registration number. This unique unalterable number is fundamental to the product line, providing a level of authenticity and security to every product which contains it. Each chip becomes a globally unique credential because

1. Every registration number is different and there are no duplicates.
2. Laser engraved silicon cannot be altered.
3. Controlling/owning an entire range of registration numbers guarantees authenticity of the product.

Ownership over a registration number range enables easy detection of unauthorized use. The test for authenticity would be: Is the device in question within my range of ownership?. This allows a Dallas Semiconductor customer to use these parts as identifiers to authenticate their products.

The unique registration number is contained in a 64–bit ROM. The number within the ROM is made up of three parts: the Family Code, the Serial Number and the Cyclic Redundancy Check (CRC). This unique registration number is lasered into each part at the time of manufacture.

8–bit Family Code

There are various product types within the 1–Wire product group. Each product type has an identifying Family Code which is constant and will not change for the life of the product. The first product type was the DS2401 / DS1990A, Family Code 01H. As products are added to the 1–Wire product group a new Family Code is assigned. It should be noted that bit 7 (the MSB of the Family Code) is reserved as a flag for Special Registration Number parts.

48–bit Serial Number

Each part in a family, (i.e., having the same Family Code) will have a unique number. The first part made has a Serial Number of 0000 0000 0000H. The Serial Number in each subsequent part will be incremented by one.

8–bit CRC

The Cyclical Redundancy Check (CRC) byte aids in verifying data integrity. This value is calculated over the Family Code and Serial Number and written into the device at the time of manufacture. A detailed explanation of CRCs is found in the "Book of DS19xx Touch Memory Standards".

B. Owning a Range of Special Registration Numbers

All components with the Dallas Semiconductor 1–Wire registration number are manufactured in whole lots. A whole lot equates to all the devices on one wafer. By the nature of the manufacturing process, each wafer (or lot) creates a fixed quantity of parts per lot, the quantity varying from product to product. When lasering each wafer during manufacturing, the starting registration number and the range are recorded, so lot integrity is maintained throughout the manufacturing process. Therefore at the end of the assembly process, each lot can be guaranteed to contain all of the yielding parts within the range specified on the shipping container. For ordering purposes, each lot size represents an order multiple. The terminology on the order form uses "Order Multiple" but is the same as a lot. Lot sizes or order multiples for each product type are as follows:

Device	typ. lot size	min. order (cust. sp. nrs.)
DS1982	2300	3 lots
DS1990A	4200	2 lots
DS1991	1100	2 lots
DS1992	2300	2 lots
DS1993	2300	2 lots
DS1994	850	4 lots
DS2401	4200	2 lots
DS2405	4200	2 lots
DS2502	2300	3 lots

C. Ordering Options

All 1–Wire devices are sold with three purchase options: Broken Lots, Whole Lots, and Special Registration Number Range Whole Lots. The key word here is LOT sales.

Broken Lots

Definition: The only guarantee is that no two parts are the same. One has to take the numbers as they are available. There is no restriction on the quantity purchased.

Whole Lots

Definition: The registration number of all devices falls within a specific range. Starting and ending number are labeled on the container. The lot is made up of all yielding devices within the range. This range is set by the number of devices fabricated on a wafer and varies depending on product type. Minimum order is one lot.

Special Registration Number Range, Whole Lots only

Definition: The registration numbers of all devices fall within a specific range which the customer can partially define. The lot is made up of all yielding devices within the range. This range is set by the number of device s fabricated on a wafer and varies depending on product type.

New customers are assigned a "Custom ID". There is a $10,000 setup fee (NRE Charge) for each Custom ID. There is a 12 week lead time from the date the Special Registration Number Range Selection Form is accepted by Dallas Semiconductor. Special Registration Number Range parts carry a price premium. Contact Dallas Semiconductor or your manufacturers representative. The minimum order quantity is detailed on the previous page.

Tape And Reel

The tape and reel option is available for the TO–92 through–hole package, and the SOT–223, 8–pin SOIC, or 6–pin C–lead surface mount packages. EIA standard 468–A specifies the dimensions and tolerances to lead tape the TO–92 package. The SOT–223 and 8–pin SOIC packages are specified by EIA–481–A.

The reel size for the TO–92 package is 1,000 parts per reel. In the event of overage, the extra components will be placed on a partial reel. The reel size for the SOT–223 and 8–pin SOIC packages is 2,500 parts per reel. Again, overage will be put on a partial reel. The tape and reel option is not available for Touch Memory.

II. UNIQUEWARE™

A. General Information

Dallas Semiconductor can supply globally unique addresses in the form of chips to meet the standards of Ethernet, Token Ring, and cellular phones. The DS2502 Add–Only Memory can be custom–ordered for quick delivery. Each device is registered, programmed to the customer's requirements, and locked under strict manufacturing controls. The unique registration number authenticates the chip and tracks the transfer of ownership. Delivery of proprietary codes can be restricted to those authorized.

B. Customization

ROM Section

In contrast to Special Registration Number Range parts, UniqueWare has no NRE–charge. UniqueWare chips are identified by the number 5E7H in the 12 most significant bits of the 48–bit serial number and the family code of 89H. This identification scheme is valid for all orders. With UniqueWare, the customization is not coded in the laser ROM, but in the second page (page address 1) of EPROM. **This page is write–protected after programming at Dallas Semiconductor.**

Memory Section

Data Structure within UniqueWare devices is TMEX–compatible (length byte, up to 28 byte of data, continuation pointer, inverted CRC16). The first 4 of the up to 28 data bytes are reserved as project ID, assigned by Dallas Semiconductor. The unique project ID allows the customer to identify its proprietary product version. The remaining 24 bytes contain the unique address and other customer or application specific information. The customer defines how these bytes are used.

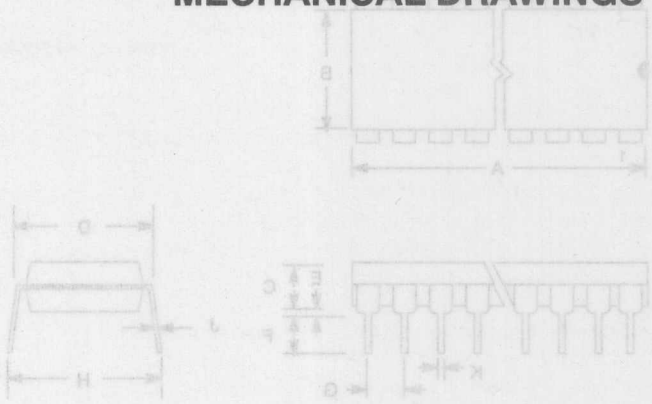
If not otherwise specified, the first page of the device (page address 0) contains a file directory according to TMEX standards. The default file name for UniqueWare data is IDNR.000. On request, page 0 will not be programmed as a TMEX device directory. This leaves a total of 3 pages or 96 bytes to be programmed by the customer.

Depending on customer specification, the preprogrammed and locked file can be up to 3 pages. If shorter, there is space for up to two more files in the device. The names of these files should be preprogrammed in the device directory. Their contents may be written later at the customer's site.

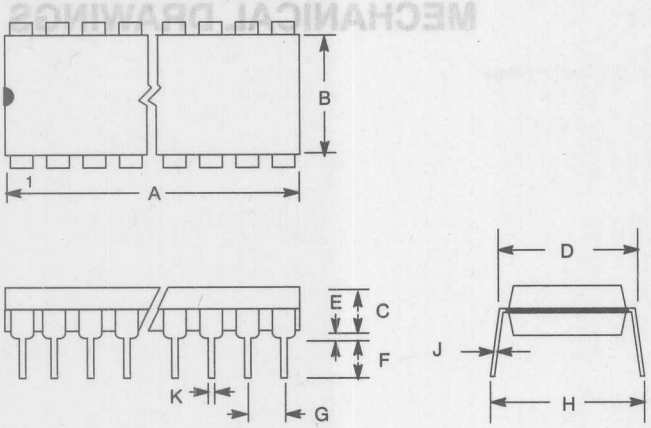
C. Ordering

For details please contact Dallas Semiconductor or your manufacturer's representative. The tape and reel option is also available for UniqueWare.

MECHANICAL DRAWINGS



8– TO 28–PIN DIP (300 MIL)



Includes:

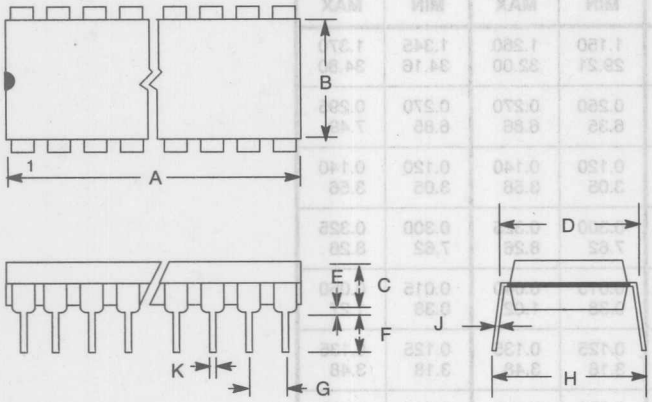
DS1000	DS1211	DS1632
DS1000M	DS1215	DS1640
DS1003	DS1221	DS1651
DS1003M	DS1222	DS1652
DS1004M	DS1228	DS1652B
DS1005	DS1229	DS1653
DS1005M	DS1231	DS1666
DS1007	DS1232	DS1667
DS1010	DS1232LP	DS1669
DS1012M	DS1234	DS1802
DS1013	DS1236	DS1830
DS1013M	DS1237	DS1867
DS1020	DS1238	DS1868
DS1033M	DS1239	DS1869
DS1035M	DS1259	DS2009D
DS1040M	DS1267	DS2010D
DS1044	DS1275	DS2011D
DS1045	DS1291	DS2013D
DS1200	DS1293	
DS1206	DS1336	
DS1210	DS1620	

PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.04	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

PKG	18-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.890	0.920	0.970	1.040	1.150	1.260	1.345	1.370
MM	22.61	23.36	24.63	26.42	29.21	32.00	34.16	34.80
B IN.	0.240	0.260	0.240	0.270	0.250	0.270	0.270	0.295
MM	6.10	6.60	6.09	6.86	6.35	6.86	6.85	7.49
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.295	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.49	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.050
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.27
F IN.	0.120	0.140	0.120	0.140	0.125	0.135	0.125	0.135
MM	3.04	3.56	3.04	3.56	3.18	3.48	3.18	3.48
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.23	2.79	2.23	2.79	2.23	2.79	2.23	2.79
H IN	0.320	0.370	0.310	0.390	0.320	0.370	0.320	0.370
MM	8.13	9.40	7.87	9.91	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.022	0.015	0.022
MM	0.38	0.53	0.38	0.53	0.38	0.56	0.38	0.56

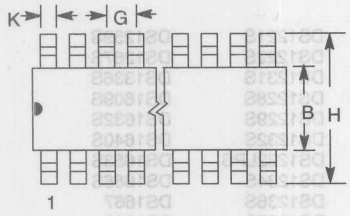
24– TO 40–PIN DIP (600 MIL)

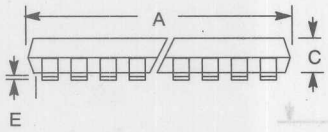


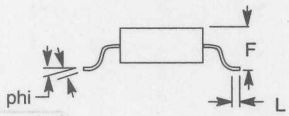
Includes:
DS1212
DS1609
DS2009
DS2010
DS2011
DS2012
DS2013

PKG	24-PIN		28-PIN		40-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25	1.445 36.70	1.470 37.34	2.050 52.07	2.075 52.71
B IN. MM	0.530 13.46	0.550 13.97	0.530 13.46	0.550 13.97	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06	0.140 3.56	0.160 4.06	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88	0.600 15.24	0.625 15.88	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27	0.015 0.380	0.040 1.02	0.015 0.380	0.040 1.02
F IN. MM	0.120 3.05	0.145 3.68	0.120 3.05	0.145 3.68	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN MM	0.625 15.88	0.675 17.15	0.625 15.88	0.675 17.15	0.625 15.88	0.675 17.15
J IN MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56	0.015 0.38	0.022 0.56	0.015 0.38	0.022 .56

8–PIN SOIC (150 MIL AND 200 MIL)



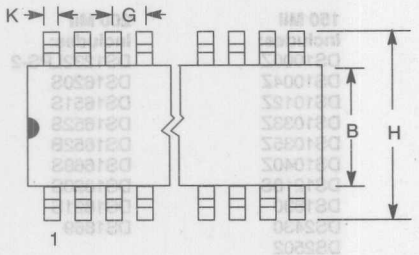




150 Mil Includes:	200 Mil Includes:
DS1000Z	DS1232LPS-2
DS1004Z	DS1620S
DS1012Z	DS1651S
DS1033Z	DS1652S
DS1035Z	DS1652B
DS1040Z	DS1669S
DS1218S	DS1820S
DS1830	DS1821S
DS2430	DS1869
DS2502	

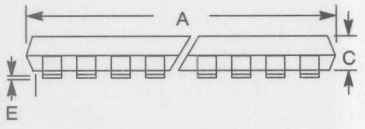
PKG	8-PIN (150 MIL)		8-PIN (200 MIL)	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.188 4.78	0.196 4.98	0.203 5.16	0.213 5.41
B IN. MM	0.150 3.81	0.158 4.01	0.203 5.16	0.213 5.41
C IN. MM	0.052 1.32	0.062 1.57	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25
F IN. MM	0.058 1.47	0.068 1.73	.074 1.88	.084 2.13
G IN. MM	.050 BSC 1.27 BSC			
H IN MM	0.230 5.84	0.244 6.20	0.302 7.67	0.318 8.07
J IN MM	0.007 0.17	0.010 0.25	0.006 0.15	0.010 0.25
K IN. MM	0.013 0.33	0.019 0.49	0.013 0.33	0.020 0.51
L IN. MM	.016 .40	.035 .89	.019 0.48	.030 .76
PHI	0°	8°	0°	8°

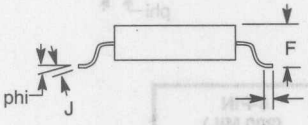
16–, 20–, AND 24–PIN SOIC (300 MIL)



Includes:

DS1000S	DS1221S	DS1259S
DS1005S	DS1222S	DS1267S
DS1007S	DS1231S	DS1336S
DS1010S	DS1228S	DS1609S
DS1013S	DS1229S	DS1632S
DS1020S	DS1232S	DS1640S
DS1045S	DS1232LPS	DS1653S
DS1200S	DS1234S	DS1666S
DS1205S	DS1236S	DS1667
DS1206	DS1237S	DS1867
DS1210S	DS1238S	DS1868
DS1211S	DS1239S	DS2404S–C01

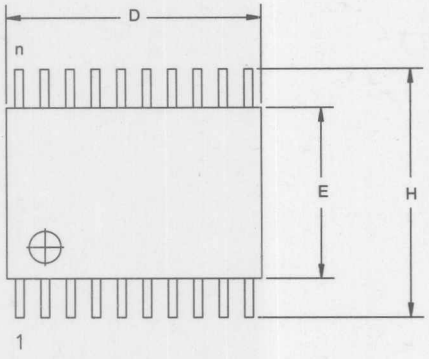


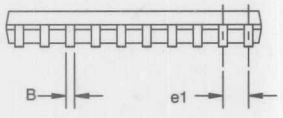


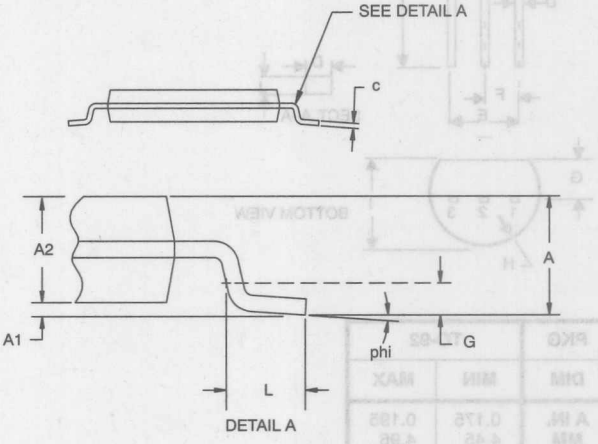
PKG	16-PIN		20-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46	0.500 12.70	0.511 12.99	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.65	0.290 7.37	0.300 7.65	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC					
H IN MM	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48	0.013 0.33	0.019 0.48	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02	.016 .406	.040 1.20	.016 .40	.040 1.02
PHI	0°	8°	0°	8°	0°	8°

20-PIN TSSOP

Includes:
DS1033E
DS1035E
DS1802
DS1867
DS2430





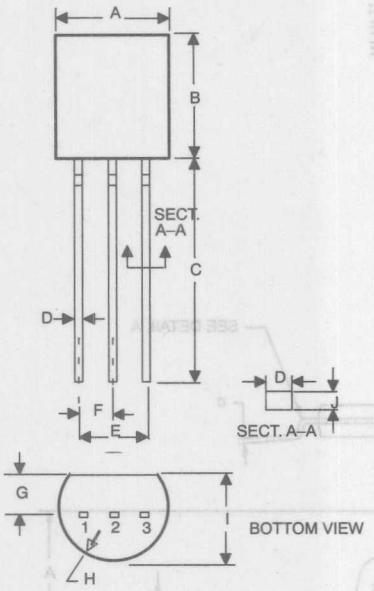


DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

TO-92 PACKAGE

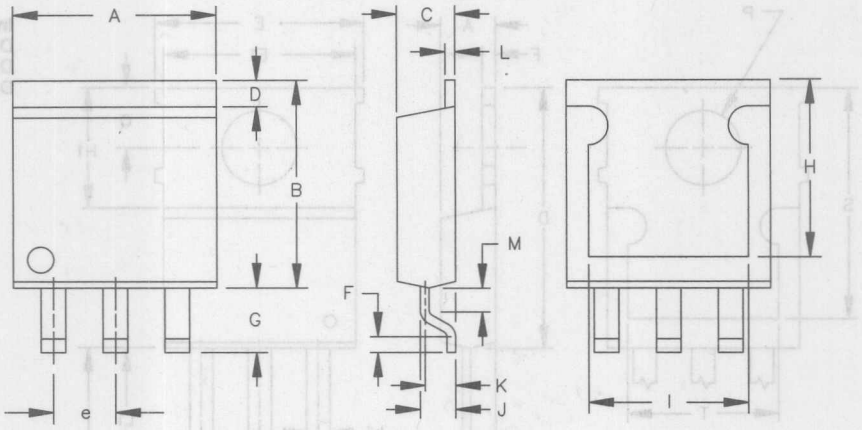
Includes:

DS1233
DS1233A
DS1233D
DS1833
DS2223
DS2224
DS2401
DS2405
DS2430
DS2502
DS2505



PKG	TO-92	
DIM	MIN	MAX
A IN. MM	0.175 4.45	0.195 4.96
B IN. MM	0.170 4.32	0.195 4.96
C IN. MM	0.500 12.70	0.610 15.49
D IN. MM	0.016 0.406	0.022 0.559
E IN. MM	0.095 2.41	0.105 2.67
F IN. MM	0.045 1.14	0.060 1.52
G IN. MM	0.45 1.14	0.060 1.52
H IN MM	0.085 2.16	0.095 2.41
I IN MM	0.130 3.30	0.155 3.94
J IN MM	0.014 0.35	0.020 0.51

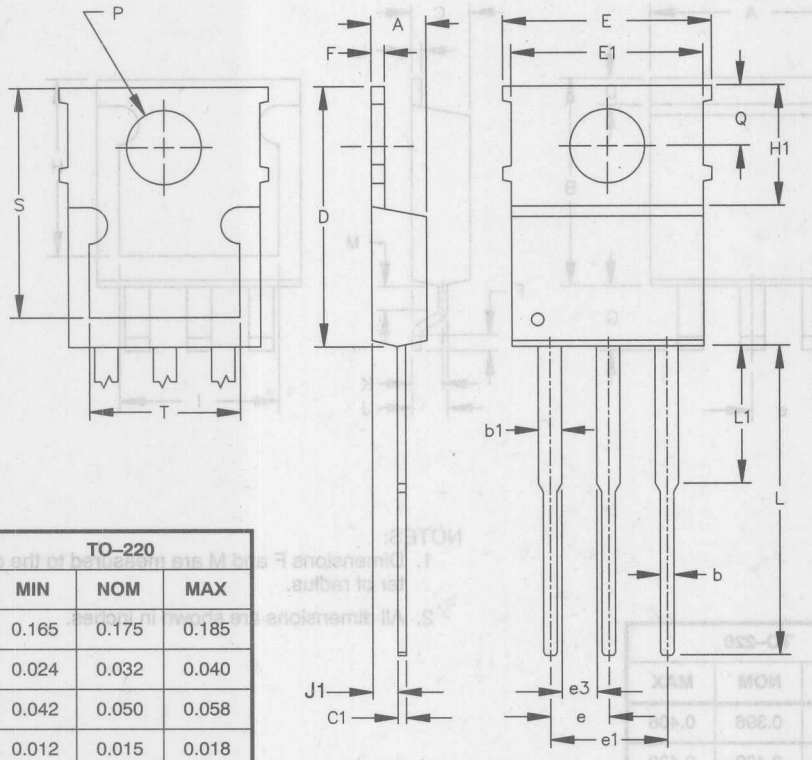
3L D2PAK (TO–220 TABLESS)



NOTES:
1. Dimensions F and M are measured to the center of radius.
2. All dimensions are shown in inches.

PKG	TO–220		
DIM	MIN	NOM	MAX
A	0.386	0.396	0.406
B	0.410	0.420	0.430
C	0.160	0.170	0.180
D	0.035	0.045	0.055
e	0.095	0.105	0.115
F	0.025	0.035	0.045
G	0.125	0.135	0.145
H	0.265	0.275	0.285
I	0.195	0.205	0.215
J	0.088	0.098	0.108
K	0.080	0.090	0.100
L	0.040	0.050	0.060
M	0.070	0.080	0.090

3L TO–220



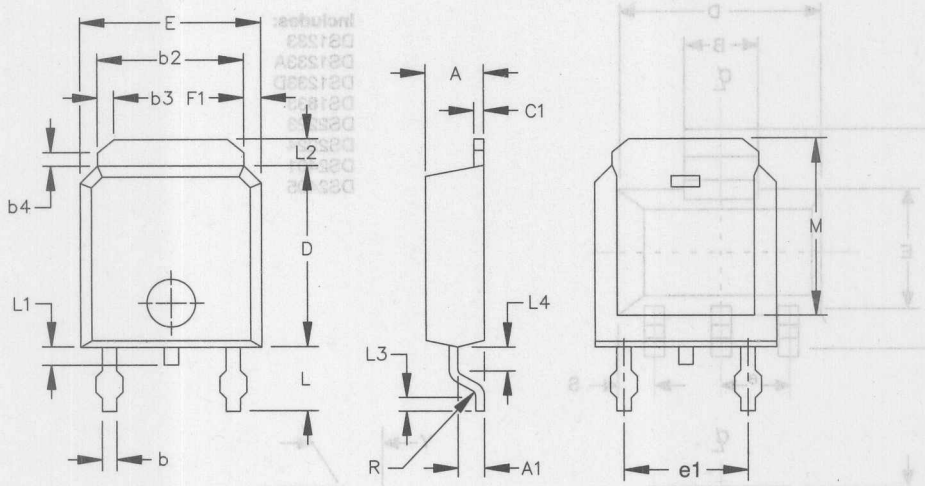
Includes:
DS1633
DS1821T
DS1837

PKG	TO–220		
DIM	MIN	NOM	MAX
A	0.165	0.175	0.185
b	0.024	0.032	0.040
b1	0.042	0.050	0.058
C1	0.012	0.015	0.018
D	0.573	0.588	0.603
E	0.394	0.404	0.414
E1	0.390	0.400	0.410
e	0.090	0.100	0.110
e1	0.190	0.200	0.210
e3	0.045	0.050	0.055
F	0.045	0.050	0.055
H1	0.236	0.248	0.260
J1	0.095	0.105	0.115
L	0.535	0.545	0.555
L1	0.220	0.230	0.240
P	0.146	0.151	0.156
Q	0.100	0.108	0.116
S	0.465	0.475	0.485
T	0.195	0.205	0.215

All dimensions are shown in inches.

3L DPAK (TO–252)

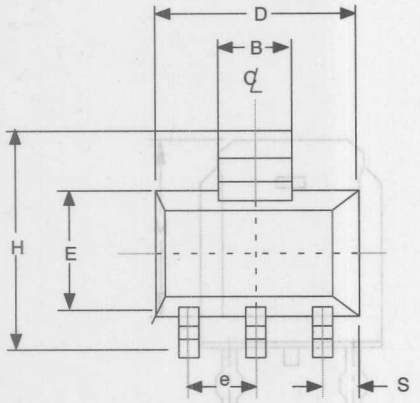
Includes:
DS1837

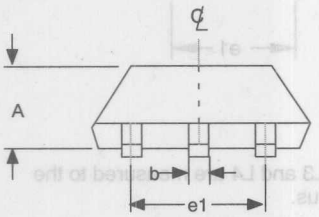


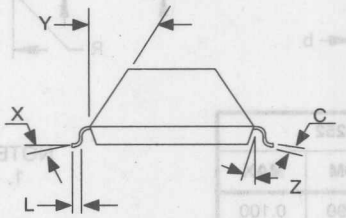
PKG	TO–252		
DIM	MIN	NOM	MAX
A	0.080	0.090	0.100
A1	0.035	0.040	0.045
b	0.025	0.030	0.035
b2	0.205	0.210	0.215
b3	0.030	0.035	0.040
b4	0.020	0.025	0.030
C1	0.018	0.020	0.023
D	0.230	0.240	0.250
E	0.250	0.260	0.270
F1	0.020	0.025	0.030
L	0.090	0.100	0.110
L1	0.010	0.025	0.040
L2	0.030	0.040	0.050
L3	0.021	0.024	0.028
L4	0.033	0.038	0.043
M	0.165	0.175	0.185
e1	0.170	0.180	0.190
R	0.008	0.010	0.012

NOTE:
1. Dimensions L3 and L4 are measured to the center of radius.
2. All dimensions are shown in inches.

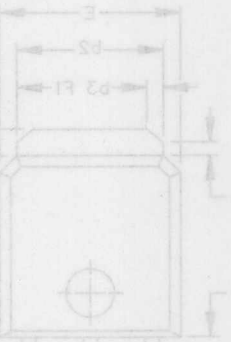
SOT–223 PACKAGE







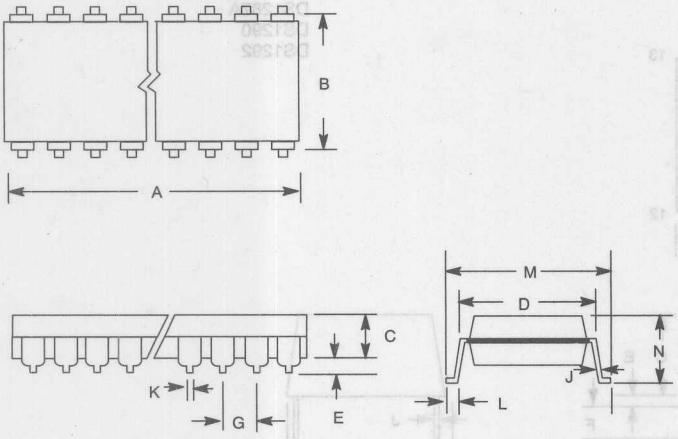
Includes:
DS1233
DS1233A
DS1233D
DS1833
DS2223
DS2224
DS2401
DS2405



DIM	INCHES	
	MIN	MAX
A	–	0.067
B	0.025	0.033
B	0.116	0.124
C	0.009	0.013
D	0.248	0.263
E	0.0905 TYP.	
E1	0.181 TYP.	
E	0.130	0.145
H	0.264	0.287
L	0.016	0.036
S	0.033	0.041
X	10° MAX	
Y	10°	20°
Z	10°	20°

8- TO 20-PIN GULLWING (300 MIL)

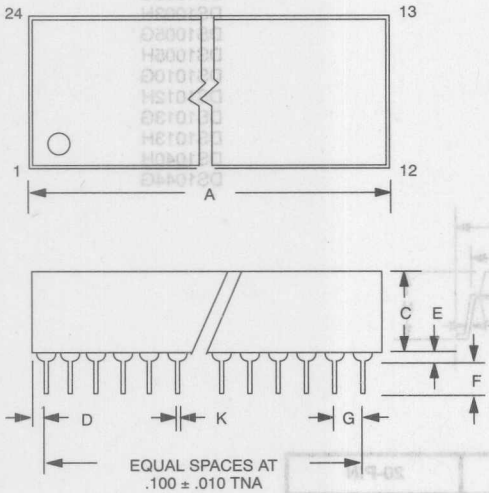
Includes:
DS1000G
DS1000H
DS1003G
DS1003H
DS1005G
DS1005H
DS1010G
DS1012H
DS1013G
DS1013H
DS1040H
DS1044G



PKG	8-PIN		14-PIN		16-PIN		20-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.345 8.76	0.400 10.16	0.740 12.19	0.780 13.20	0.740 18.79	0.780 9.81	0.960 24.38	1.040 26.41
B IN. MM	0.240 6.10	0.260 6.60	0.240 6.10	0.260 6.60	0.240 6.10	0.260 6.60	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26
E IN. MM	0.020 0.51	0.040 1.02	0.020 0.51	0.040 1.02	0.020 0.51	0.040 1.02	0.020 0.51	0.040 1.02
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
J IN. MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53
L IN. MM	0.030 0.76	0.050 1.27	0.030 0.76	0.050 1.27	0.030 0.76	0.050 1.27	0.030 0.76	0.050 1.27
M IN. MM	0.370 9.40	0.420 10.67	0.370 9.40	0.420 10.67	0.370 9.40	0.420 10.67	0.370 9.40	0.420 10.67
N IN. MM	0.160 4.06	0.180 4.57	0.160 4.06	0.180 4.57	0.160 4.06	0.180 4.57	0.160 4.06	0.180 4.57

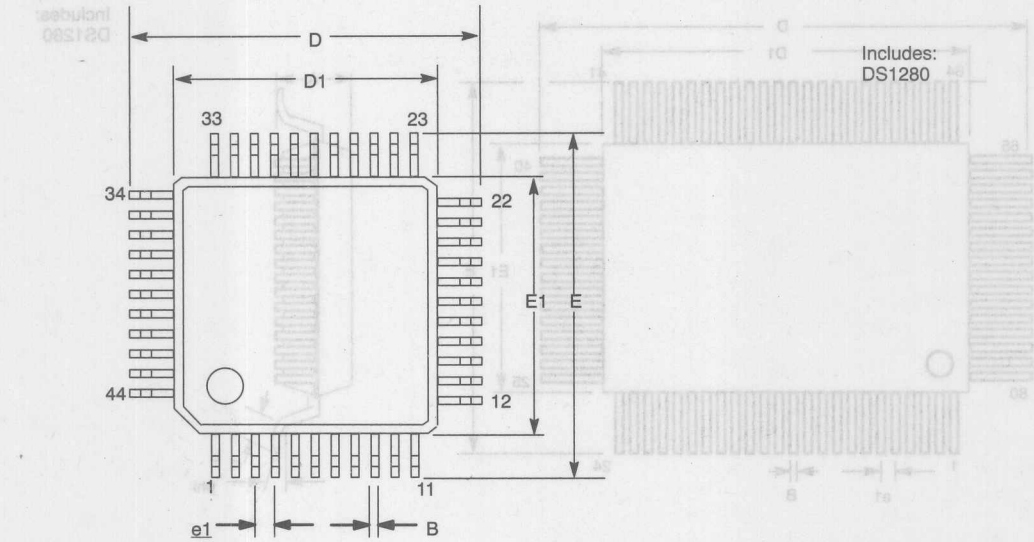
16- AND 24- PIN ENCAPSULATED PACKAGE (FLUSH BOTTOM – 450 MIL.)

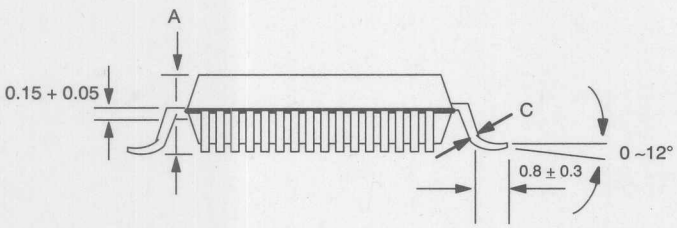
Includes:
DS1287
DS1287A
DS1290
DS1292



PKG	16-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.820 20.83	0.840 21.34	1.310 33.27	1.330 33.78
B IN. MM	0.440 11.18	0.460 11.68	0.440 11.18	0.460 11.68
C IN. MM	0.330 8.38	0.370 9.40	0.330 8.38	0.370 9.40
D IN. MM	0.180 4.57	0.210 5.33	0.215 5.46	0.245 6.22
E IN. MM	0.020 0.51	0.040 1.02	0.020 0.51	0.040 1.02
F IN. MM	0.110 2.79	0.140 3.56	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN MM	0.330 8.38	0.380 9.65	0.330 8.38	0.380 9.65
J IN MM	0.008 0.20	0.012 0.31	0.008 0.20	0.012 0.31
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53

44–PIN QUAD FLAT PACK (PRELIMINARY)

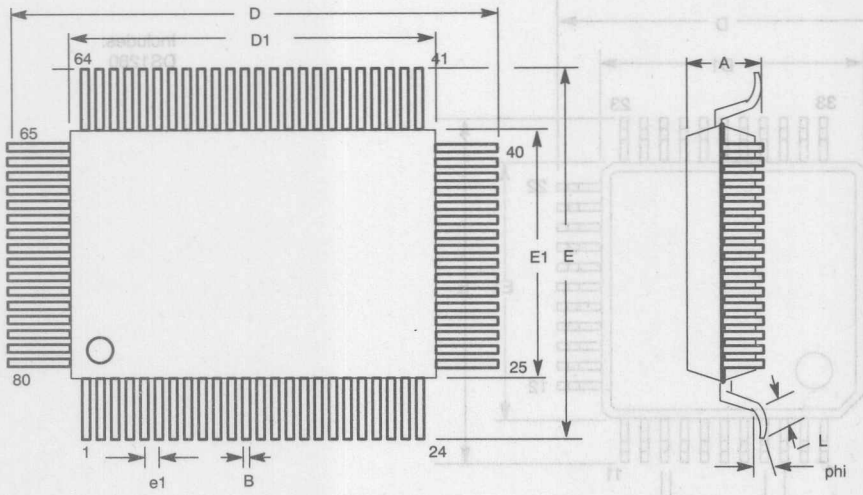




PKG	10 X 10 BODY		14 X 14 BODY	
DIM	MIN	MAX	MIN	MAX
A MM	–	2.45	–	3.4
B MM	0.30	0.45	0.20	0.50
C MM	0.13	0.23	0.10	0.20
D MM	13.65	14.35	16.95	18.00
E MM	13.65	14.35	16.95	18.00
D1 MM	9.90	10.10	13.80	14.20
E1 MM	9.90	10.10	13.80	14.20
L MM	0.65	0.95	0.50	1.10
e1 IN MM	0.315 0.80 BSC		0.039 1.00 BSC	

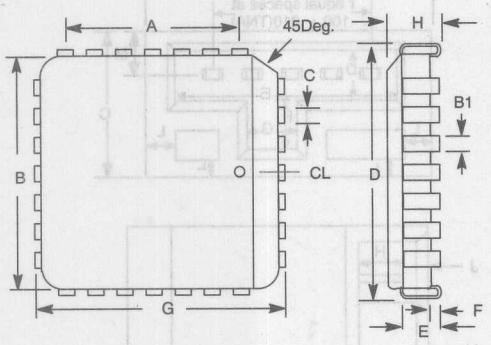
80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)

Includes:
DS1280

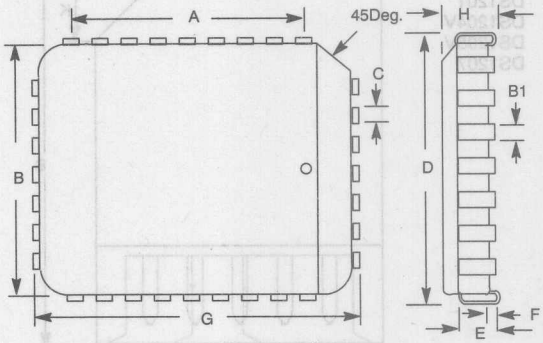


PKG	80-PIN	
DIM	MIN	MAX
A IN. MM	0.11 2.80	0.128 3.25
B IN. MM	0.010 0.25	0.020 0.45
e1 IN. MM	0.031 BSC 0.80 BSC	
D1 IN. MM	0.781 19.85	0.793 20.15
E1 IN. MM	0.545 13.85	0.557 14.15
E IN. MM	0.688 17.50	0.720 18.30
D IN. MM	0.921 23.40	0.953 24.20
L IN MM	0.025 0.65	0.038 0.95
phi	0°	8°

28- AND 32- PIN PLASTIC LEADED CHIP CARRIERS (PLCC)



28- Pin Includes:
DS1212Q

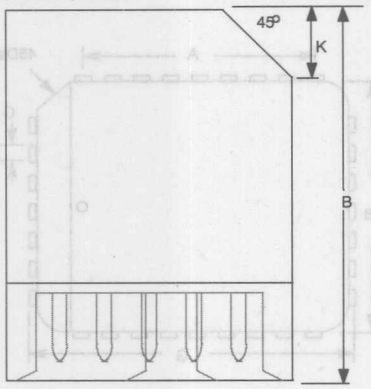


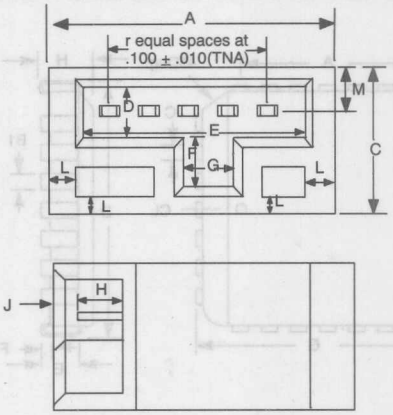
32-Pin Includes:
DS2009Q
DS2010Q
DS2011Q
DS2012Q

PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.300 BSC 7.62		0.400 BSC 10.16	
B IN. MM	0.445 11.30	0.460 11.68	0.442 11.30	0.460 11.68
B1 IN MM	0.013 0.33	0.021 0.53	0.013 0.33	0.021 0.53
C IN MM	0.027 0.68	0.33 0.84	0.027 0.68	0.33 0.84
D IN. MM	0.480 12.19	0.500 12.70	0.480 12.19	0.500 12.70
D2 IN. MM	0.390 9.91	0.430 10.92	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05	0.060 1.52	0.095 2.41
E2 IN. MM	0.390 9.91	0.430 10.92	0.490 12.45	0.530 13.46
F IN. MM	0.020 0.51		0.015 0.38	
G IN MM	0.480 12.19	0.500 12.70	0.580 14.7	0.600 15.24
H IN MM	0.165 4.19	0.180 4.57	0.100 2.54	0.140 3.56

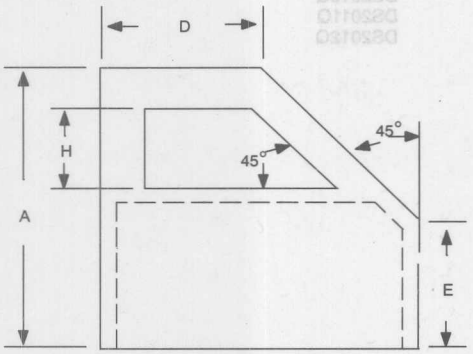
ELECTRONIC KEY/TAG

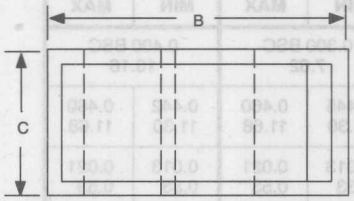
Includes:
DS1201
DS1204V
DS1205V
DS1207





KEY/TAG CAP

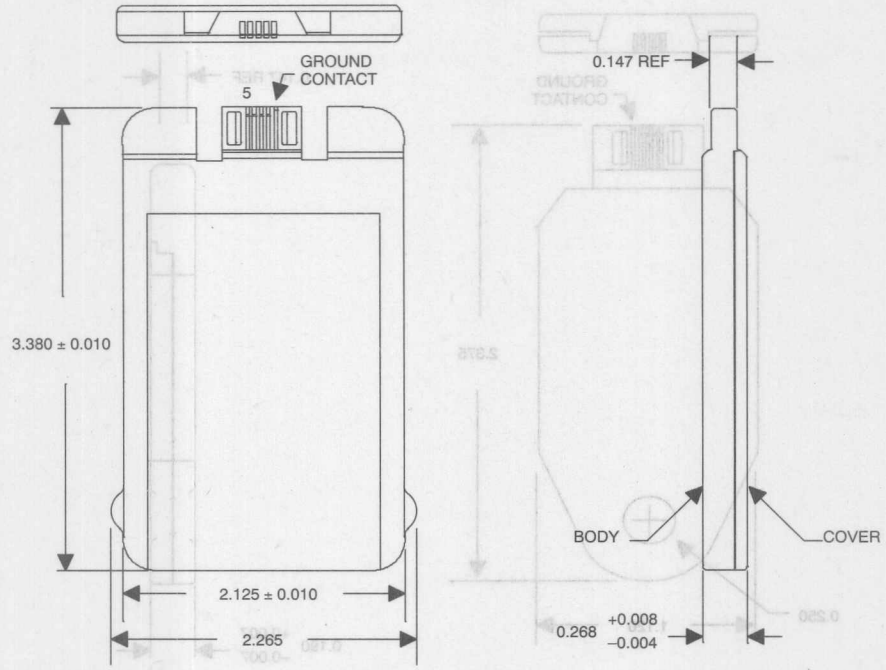




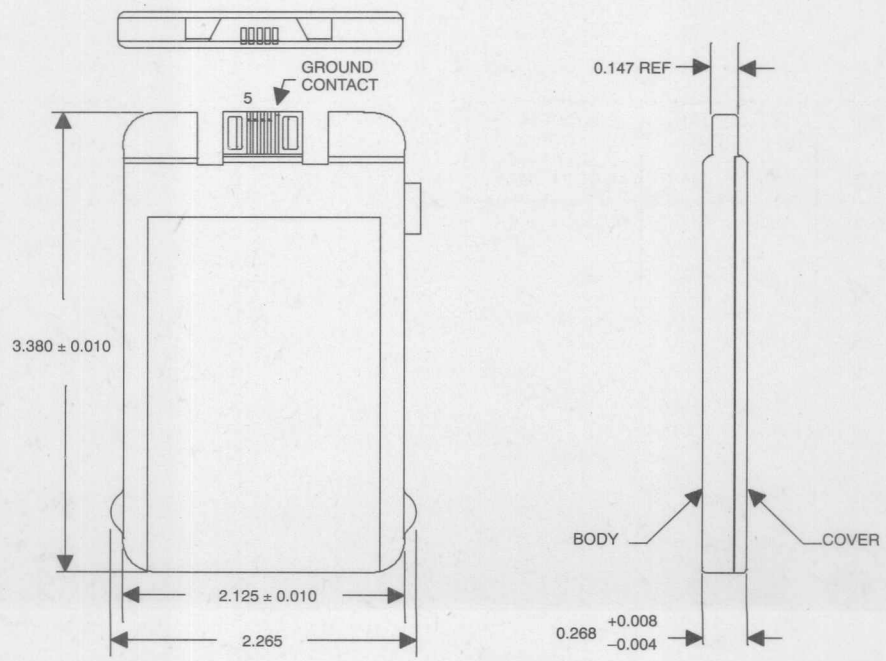
PKG	ELECTRONIC KEY/TAG		KEY/TAG CAP	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.610 15.50	0.650 16.51	0.790 20.07	0.810 20.57
B IN. MM	0.740 18.80	0.760 19.30	0.680 17.27	0.700 17.78

C IN. MM	0.310 7.87	0.355 9.02	0.405 10.29	0.425 10.80
D IN. MM	0.100 2.54	0.110 2.79	0.290 7.37	0.310 7.87
E IN. MM	0.505 12.83	0.515 13.08	0.410 10.41	0.430 10.92
F IN. MM	0.100 2.54	0.110 2.79		

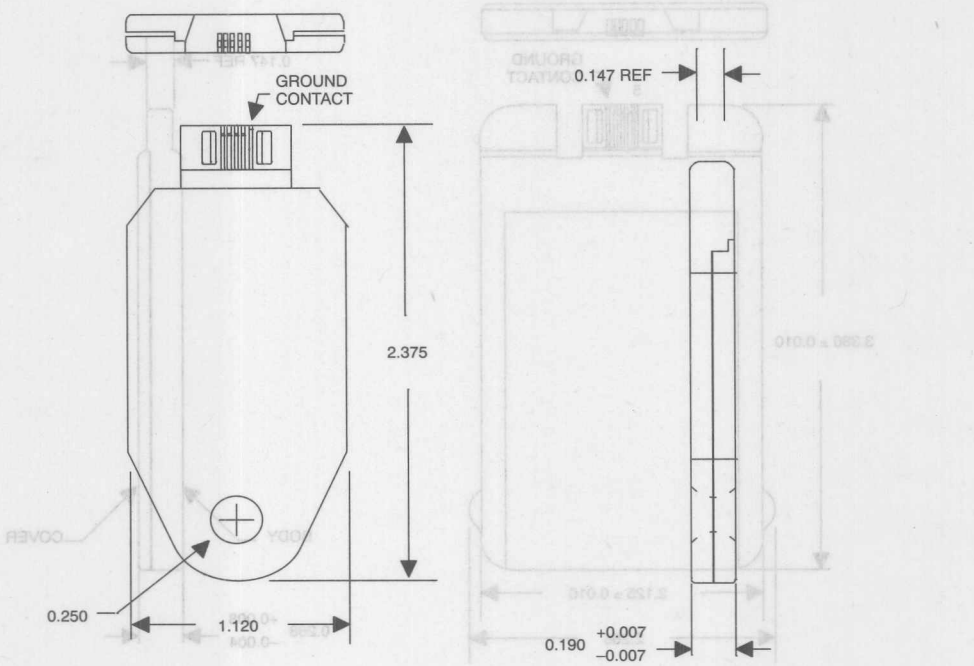
CYBERCARD PACKAGE, NON–POLARIZED



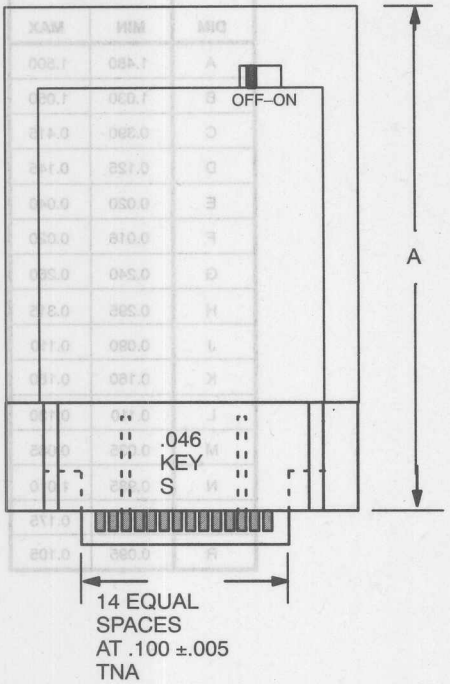
CYBERCARD PACKAGE, POLARIZED



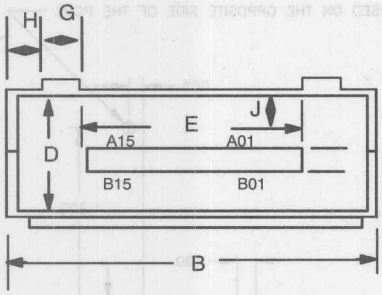
CYBERKEY PACKAGE

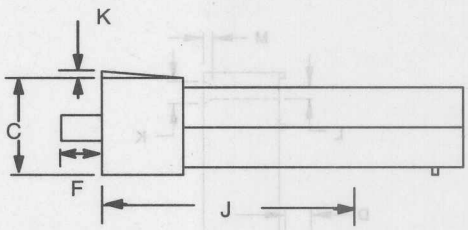


NON-VOLATILE READ/WRITE CARTRIDGE

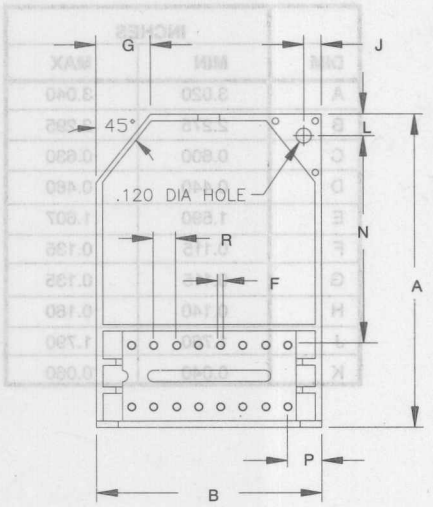


DIM	INCHES MIN	INCHES MAX
A	3.020	3.040
B	2.275	2.295
C	0.600	0.630
D	0.440	0.460
E	1.590	1.607
F	0.115	0.135
G	0.115	0.135
H	0.140	0.160
J	1.760	1.790
K	0.040	0.060



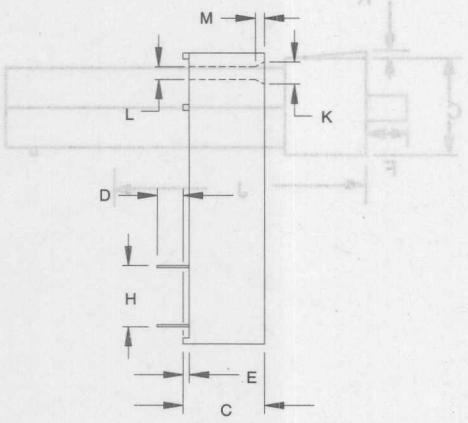


DS1260 SMART BATTERY



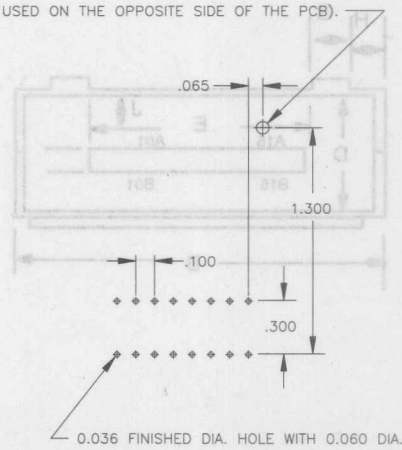
BOTTOM VIEW

DIM	INCHES MIN	INCHES MAX
A	1.480	1.500
B	1.030	1.050
C	0.390	0.415
D	0.125	0.145
E	0.020	0.040
F	0.016	0.020
G	0.240	0.260
H	0.295	0.315
J	0.090	0.110
K	0.160	0.180
L	0.110	0.130
M	0.035	0.065
N	0.985	1.010
P	0.155	0.175
R	0.095	0.105

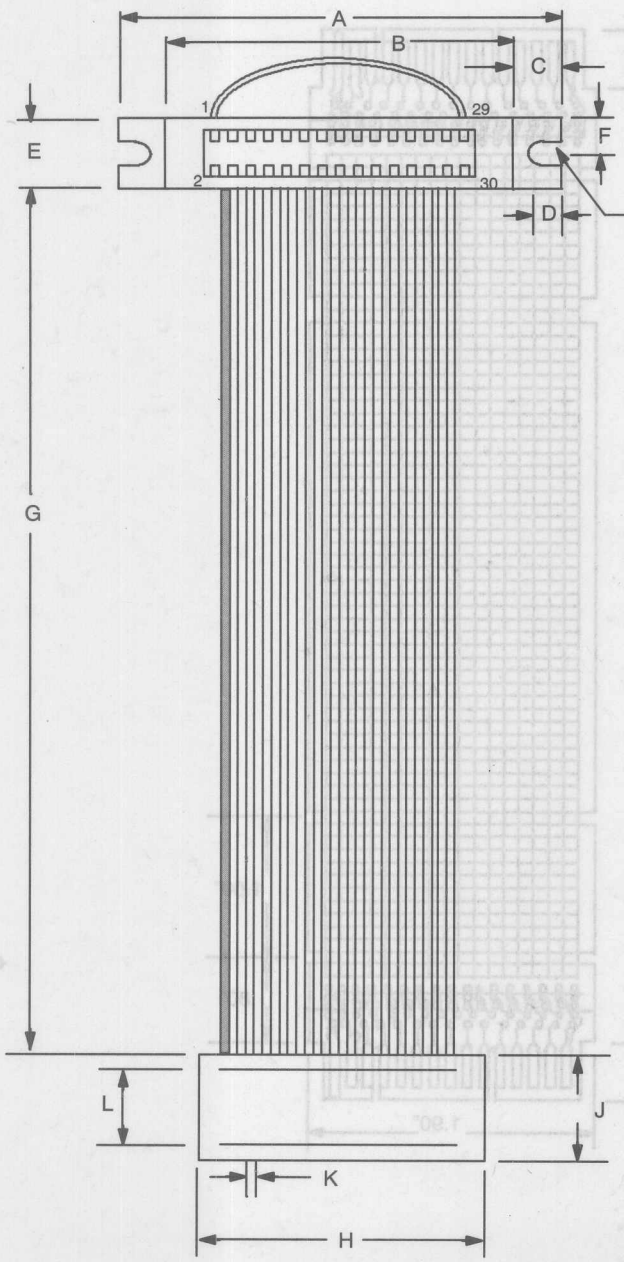


SIDE VIEW

0.150 DIA. HOLE (UNSUPPORTED) (FLAT WASHER SHOULD BE USED ON THE OPPOSITE SIDE OF THE PCB).



BYTEWIDE CABLE HARNESS



DIM.	INCHES	
	MIN.	MAX.
A	2.480	2.520
B	1.940	1.980
C	.260	.280
D	.160	.175
E	.395	.415
F	.195	.205
G	5.25	5.65
H	1.470	1.500
J	.715	.735
K	.090	.110
L	.590	.610

NOTES: COLOR STRIPE INDICATES PIN 1
END ON 28-PIN PULG.
DIMENSION L IS CENTER TO CENTER

DS9003
CARTRIDGE PROTO
BOARD