

### FEATURES

- 256-position digital potentiometer**
- Two-time programmable (TTP) set-and-forget resistance setting allows second-chance permanent programming**
- Unlimited adjustments prior to one-time programming (OTP) activation**
- OTP overwrite allows dynamic adjustments with user-defined preset**
- End-to-end resistance: 2.5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$**
- Compact MINI\_SO-10 (3 mm  $\times$  4.9 mm) package**
- Fast settling time:  $t_s = 5 \mu\text{s}$  typical in power-up**
- Full read/write of wiper register**
- Power-on preset to midscale**
- Extra package address decode pins AD0 and AD1**
- Single-supply 2.7 V to 5.5 V**
- Low temperature coefficient: 35 ppm/ $^{\circ}\text{C}$**
- Low power,  $I_{DD} = 6 \mu\text{A}$  maximum**
- Wide operating temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$**
- Evaluation board and software are available**
- Software replaces  $\mu\text{C}$  in factory programming applications**

### APPLICATIONS

- Systems calibration**
- Electronics level setting**
- Mechanical trimmers replacement in new designs**
- Permanent factory PCB setting**
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors**
- RF amplifier biasing**
- Automotive electronics adjustment**
- Gain control and offset adjustment**

### GENERAL OVERVIEW

The AD5170 is a 256-position, two-time programmable, digital potentiometer<sup>1</sup> that employs fuse link technology, giving users two opportunities to permanently program the resistance setting. For users who do not need to program the digital potentiometer setting in memory more than once, the OTP feature is a cost-effective alternative to EEMEM. The AD5170 performs the same electronic adjustment function as mechanical potentiometers or variable resistors with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

### Rev. B

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### FUNCTIONAL BLOCK DIAGRAM

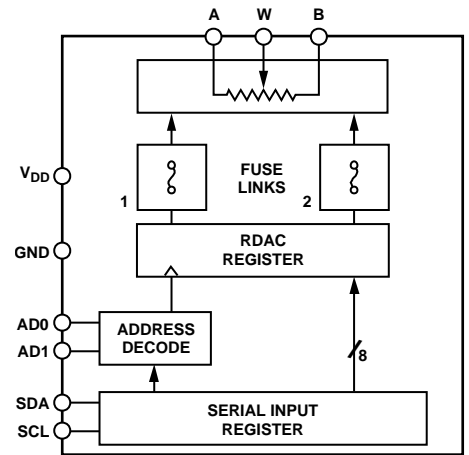


Figure 1.

The AD5170 is programmed using a 2-wire, I<sup>2</sup>C<sup>®</sup> compatible digital interface. Unlimited adjustments are allowed before permanently setting the resistance value, and there are two opportunities for permanent programming. During OTP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

Unlike traditional OTP digital potentiometers, the AD5170 has a unique temporary OTP overwrite feature that allows for new adjustments even after the fuse has been blown. However, the OTP setting is restored during subsequent power-up conditions. This feature allows users to treat these digital potentiometers as volatile potentiometers with a programmable preset.

For applications that program the AD5170 at the factory, Analog Devices offers device programming software that runs on Windows NT<sup>®</sup>, Windows<sup>®</sup> 2000, and Windows<sup>®</sup> XP operating systems. This software effectively replaces any external I<sup>2</sup>C controllers, thus enhancing the time-to-market of the user's systems.

<sup>1</sup> The terms digital potentiometer, VR, and RDAC are used interchangeably.

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### 11/03—Revision 0: Initial Version

## ELECTRICAL CHARACTERISTICS—2.5 k $\Omega$ Version

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-2	$\pm 0.1$	+2	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	6	$\pm 0.75$	+6	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$	$T_A = 25^\circ\text{C}$	-20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/ $^\circ\text{C}$
$R_{WB}$ (Wiper Resistance)	$R_{WB}$	Code = 0x00, $V_{DD} = 5\text{ V}$		160	200	$\Omega$
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE</b> (Specifications apply to all VRs)						
Differential Nonlinearity <sup>4</sup>	DNL		-1.5	$\pm 0.1$	+1.5	LSB
Integral Nonlinearity <sup>4</sup>	INL		-2	$\pm 0.6$	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	Code = 0xFF	-10	-2.5	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = 0x00	0	2	10	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	$V_A, V_B, V_W$		GND		$V_{DD}$	V
Capacitance <sup>6</sup> A, B	$C_A, C_B$	$f = 1\text{ MHz}$ , measured to GND, code = 0x80		45		pF
Capacitance W	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = 0x80		60		pF
Shutdown Supply Current <sup>7</sup>	$I_{A\_SD}$	$V_{DD} = 5.5\text{ V}$		0.01	1	$\mu\text{A}$
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		1		nA
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High (SDA and SCL) <sup>8</sup>	$V_{IH}$	$V_{DD} = 5\text{ V}$	$0.7 V_{DD}$		$V_{DD} + 0.5$	V
Input Logic Low (SDA and SCL) <sup>8</sup>	$V_{IL}$	$V_{DD} = 5\text{ V}$	-0.5		$+0.3 V_{DD}$	V
Input Logic High (AD0 and AD1)	$V_{IH}$	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low (AD0 and AD1)	$V_{IL}$	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>5</sup>	$C_{IL}$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD\_RANGE}$		2.7		5.5	V
OTP Supply Voltage <sup>8, 9</sup>	$V_{DD\_OTP}$	$T_A = 25^\circ\text{C}$	5.25		5.5	V
Supply Current	$I_{DD}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3.5	6	$\mu\text{A}$
OTP Supply Current <sup>8, 10</sup>	$I_{DD\_OTP}$	$V_{DD\_OTP} = 5.5\text{ V}$ , $T_A = 25^\circ\text{C}$	100			mA
Power Dissipation <sup>11</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$ , $V_{DD} = 5\text{ V}$			30	$\mu\text{W}$
Power Supply Sensitivity	PSS	$V_{DD} = 5\text{ V} \pm 10\%$ , code = midscale		$\pm 0.02$	$\pm 0.08$	%/%
<b>DYNAMIC CHARACTERISTICS<sup>12</sup></b>						
Bandwidth -3 dB	BW_2.5K	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1\text{ V rms}$ , $V_B = 0\text{ V}$ , $f = 1\text{ kHz}$		0.1		%
$V_W$ Settling Time	$t_s$	$V_A = 5\text{ V}$ , $V_B = 0\text{ V}$ , $\pm 1\text{ LSB}$ error band		1		$\mu\text{s}$
Resistor Noise Voltage Density	$e_{N\_WB}$	$R_{WB} = 1.25\text{ k}\Omega$ , $R_s = 0$		3.2		nV/ $\sqrt{\text{Hz}}$

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<sup>1</sup> Typical specifications represent average readings at 25°C and  $V_{DD} = 5\text{ V}$ .

<sup>2</sup> Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup>  $V_{AB} = V_{DD}$ , Wiper ( $V_W$ ) = no connect.

<sup>4</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ . DNL specification limits of  $\pm 1\text{ LSB}$  maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor terminals A, B, W have no limitations on polarity with respect to each other.

<sup>6</sup> Guaranteed by design and not subject to production test.

<sup>7</sup> Measured at the A terminal. The A terminal is open circuited in shutdown mode.

<sup>8</sup> The minimum voltage requirement on the  $V_{IH}$  is  $0.7\text{ V} \times V_{DD}$ . For example,  $V_{IH\text{ min}} = 3.5\text{ V}$  when  $V_{DD} = 5\text{ V}$ . It is typical for the SCL and SDA resistors to be pulled up to  $V_{DD}$ . However, care must be taken to ensure that the minimum  $V_{IH}$  is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

<sup>9</sup> Different from operating power supply; power supply for OTP is used one time only.

<sup>10</sup> Different from operating current; supply current for OTP lasts approximately 400 ms for use one time only.

<sup>11</sup>  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ . CMOS logic level inputs result in minimum power dissipation.

<sup>12</sup> All dynamic characteristics use  $V_{DD} = 5\text{ V}$ .

## ELECTRICAL CHARACTERISTICS—10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$ VERSIONS

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ;  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-1	$\pm 0.1$	+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	-2.5	$\pm 0.25$	+2.5	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$	$T_A = 25^\circ\text{C}$	-20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/ $^\circ\text{C}$
$R_{WB}$ (Wiper Resistance)	$R_{WB}$	Code = 0x00, $V_{DD} = 5\text{ V}$		160	200	$\Omega$
<b>DC CHARACTERISTICS — POTENTIOMETER DIVIDER MODE</b> (Specifications apply to all VRs)						
Differential Nonlinearity <sup>4</sup>	DNL		-1	$\pm 0.1$	+1	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1	$\pm 0.3$	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	Code = 0xFF	-2.5	-1	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = 0x00	0	1	2.5	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	$V_A, V_B, V_W$		GND		$V_{DD}$	V
Capacitance <sup>6</sup> A, B	$C_A, C_B$	$f = 1\text{ MHz}$ , measured to GND, code = 0x80		45		pF
Capacitance W <sup>6</sup>	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = 0x80		60		pF
Shutdown Supply Current <sup>7</sup>	$I_{A\_SD}$	$V_{DD} = 5.5\text{ V}$		0.01	1	$\mu\text{A}$
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		1		nA
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High (SDA and SCL) <sup>8</sup>	$V_{IH}$	$V_{DD} = 5\text{ V}$	$0.7 V_{DD}$		$V_{DD} + 0.5$	V
Input Logic Low (SDA and SCL) <sup>8</sup>	$V_{IL}$	$V_{DD} = 5\text{ V}$	-0.5		$+0.3 V_{DD}$	V
Input Logic High (AD0 and AD1)	$V_{IH}$	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low (AD0 and AD1)	$V_{IL}$	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>6</sup>	$C_{IL}$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD\_RANGE}$		2.7		5.5	V
OTP Supply Voltage <sup>8, 9</sup>	$V_{DD\_OTP}$		5.25		5.5	V
Supply Current	$I_{DD}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3.5	6	$\mu\text{A}$
OTP Supply Current <sup>8, 10</sup>	$I_{DD\_OTP}$	$V_{DD\_OTP} = 5.5\text{ V}$ , $T_A = 25^\circ\text{C}$	100			mA
Power Dissipation <sup>11</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$ , $V_{DD} = 5\text{ V}$			30	$\mu\text{W}$
Power Supply Sensitivity	PSS	$V_{DD} = 5\text{ V} \pm 10\%$ , code = midscale		$\pm 0.02$	$\pm 0.08$	%/%
<b>DYNAMIC CHARACTERISTICS<sup>12</sup></b>						
Bandwidth -3 dB	BW	$R_{AB} = 10\text{ k}\Omega$ , code = 0x80 $R_{AB} = 50\text{ k}\Omega$ , code = 0x80 $R_{AB} = 100\text{ k}\Omega$ , code = 0x80		600 100 40		kHz kHz kHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1\text{ V rms}$ , $V_B = 0\text{ V}$ , $f = 1\text{ kHz}$ , $R_{AB} = 10\text{ k}\Omega$		0.1		%
$V_W$ Settling Time (10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$ )	$t_s$	$V_A = 5\text{ V}$ , $V_B = 0\text{ V}$ , $\pm 1\text{ LSB}$ error band		2		$\mu\text{s}$
Resistor Noise Voltage Density	$e_{N\_WB}$	$R_{WB} = 5\text{ k}\Omega$ , $R_S = 0$		9		nV/ $\sqrt{\text{Hz}}$

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<sup>1</sup> Typical specifications represent average readings at 25°C and  $V_{DD} = 5\text{ V}$ .

<sup>2</sup> Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup>  $V_{AB} = V_{DD}$ , Wiper ( $V_W$ ) = no connect.

<sup>4</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ . DNL specification limits of  $\pm 1$  LSB maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor terminals A, B, W have no limitations on polarity with respect to each other.

<sup>6</sup> Guaranteed by design and not subject to production test.

<sup>7</sup> Measured at the A terminal. The A terminal is open circuited in shutdown mode.

<sup>8</sup> The minimum voltage requirement on the  $V_{IH}$  is  $0.7\text{ V} \times V_{DD}$ . For example,  $V_{IH\text{ min}} = 3.5\text{ V}$  when  $V_{DD} = 5\text{ V}$ . It is typical for the SCL and SDA resistors to be pulled up to  $V_{DD}$ . However, care must be taken to ensure that the minimum  $V_{IH}$  is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

<sup>9</sup> Different from operating power supply, power supply OTP is used one time only.

<sup>10</sup> Different from operating current, supply current for OTP lasts approximately 400 ms for use one time only.

<sup>11</sup>  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ . CMOS logic level inputs result in minimum power dissipation.

<sup>12</sup> All dynamic characteristics use  $V_{DD} = 5\text{ V}$ .

## TIMING CHARACTERISTICS—2.5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$ VERSIONS

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ;  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>I<sup>2</sup>C INTERFACE TIMING CHARACTERISTICS<sup>1</sup></b> (Specifications apply to all parts)						
SCL Clock Frequency	$f_{SCL}$				400	kHz
$t_{BUF}$ Bus Free Time between STOP and START	$t_1$		1.3			$\mu\text{s}$
$t_{HD;STA}$ Hold Time (Repeated START)	$t_2$	After this period, the first clock pulse is generated.	0.6			$\mu\text{s}$
$t_{LOW}$ Low Period of SCL Clock	$t_3$		1.3			$\mu\text{s}$
$t_{HIGH}$ High Period of SCL Clock	$t_4$		0.6			$\mu\text{s}$
$t_{SU;STA}$ Setup Time for Repeated START Condition	$t_5$		0.6			$\mu\text{s}$
$t_{HD;DAT}$ Data Hold Time <sup>2</sup>	$t_6$				0.9	$\mu\text{s}$
$t_{SU;DAT}$ Data Setup Time	$t_7$		100			ns
$t_F$ Fall Time of Both SDA and SCL Signals	$t_8$				300	ns
$t_R$ Rise Time of Both SDA and SCL Signals	$t_9$				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	$t_{10}$		0.6			$\mu\text{s}$

<sup>1</sup> See Figure 45 for locations of measured values.

<sup>2</sup> The maximum  $t_{HD;DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Value
$V_{DD}$ to GND	-0.3 V to +7 V
$V_A$ , $V_B$ , $V_W$ to GND	$V_{DD}$
Terminal Current, A to B, A to W, B to W <sup>1</sup>	
Pulsed	$\pm 20$ mA
Continuous	$\pm 5$ mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Maximum Junction Temperature ( $T_{JMAX}$ )	$150^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$300^\circ\text{C}$
Thermal Resistance <sup>2</sup> $\theta_{JA}$ : MSOP-10	$230^\circ\text{C/W}$

<sup>1</sup> Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Package power dissipation =  $(T_{JMAX} - T_A)/\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

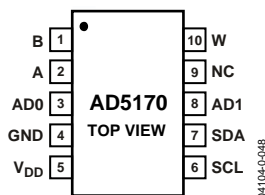


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin	Mnemonic	Description
1	B	B Terminal. $GND \leq V_B \leq V_{DD}$ .
2	A	A Terminal. $GND \leq V_A \leq V_{DD}$ .
3	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
4	GND	Digital Ground.
5	V <sub>DD</sub>	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V <sub>DD</sub> needs to be a minimum of 5.25 V and have a 100 mA driving capability.
6	SCL	Serial Clock Input. Positive edge triggered. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that V <sub>IH</sub> min is $0.7 V \times V_{DD}$ .
7	SDA	Serial Data Input/Output. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that V <sub>IH</sub> min is $0.7 V \times V_{DD}$ .
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	NC	No Connect.
10	W	W Terminal. $GND \leq V_W \leq V_{DD}$ .

TYPICAL PERFORMANCE CHARACTERISTICS

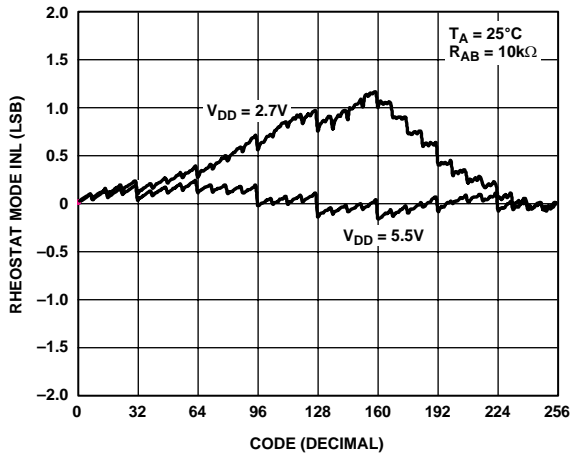


Figure 3. R-INL vs. Code vs. Supply Voltages

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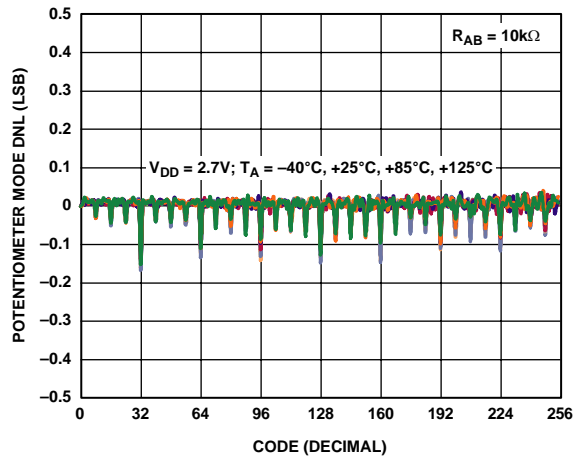


Figure 6. DNL vs. Code vs. Temperature

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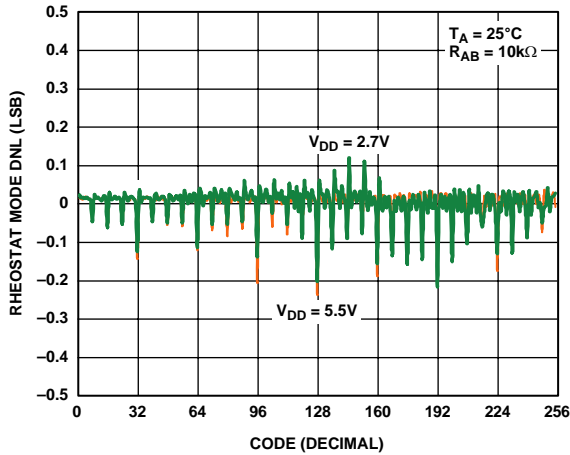


Figure 4. R-DNL vs. Code vs. Supply Voltages

04104-0-003

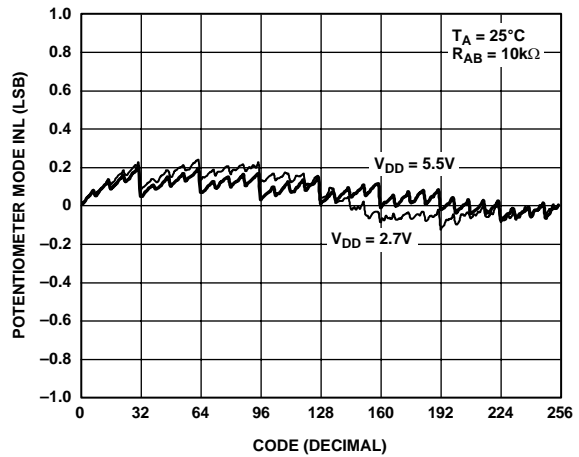


Figure 7. INL vs. Code vs. Supply Voltages

04104-0-006

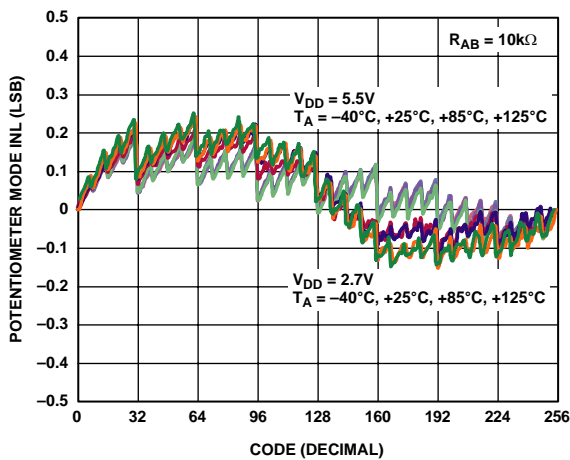


Figure 5. INL vs. Code vs. Temperature

04104-0-004

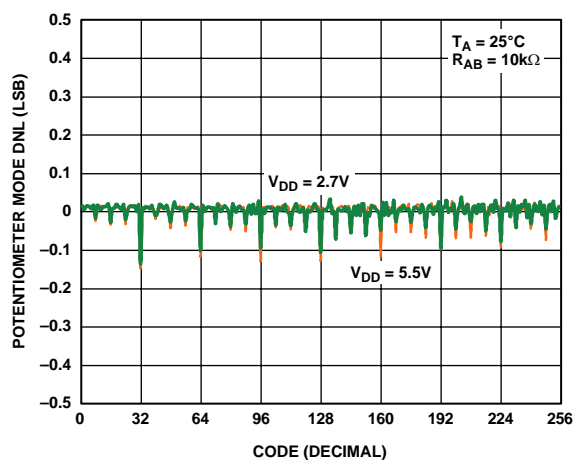


Figure 8. DNL vs. Code vs. Supply Voltages

04104-0-007

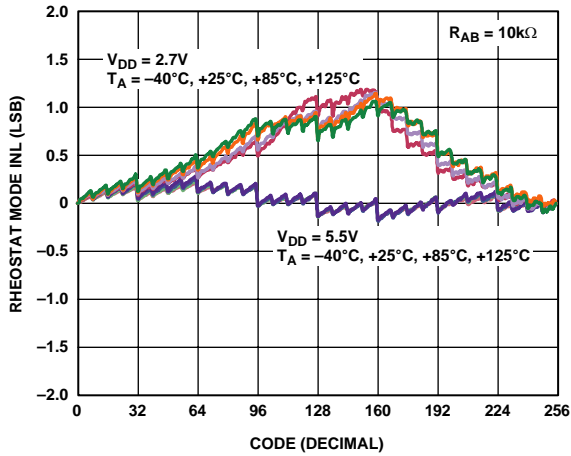


Figure 9. R-INL vs. Code vs. Temperature

04104-0-008

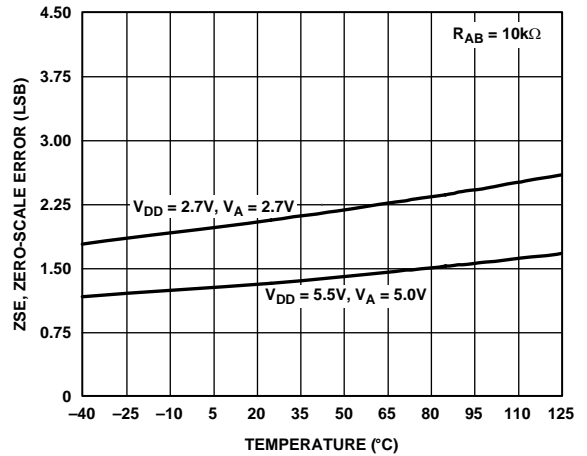


Figure 12. Zero-Scale Error vs. Temperature

04104-0-011

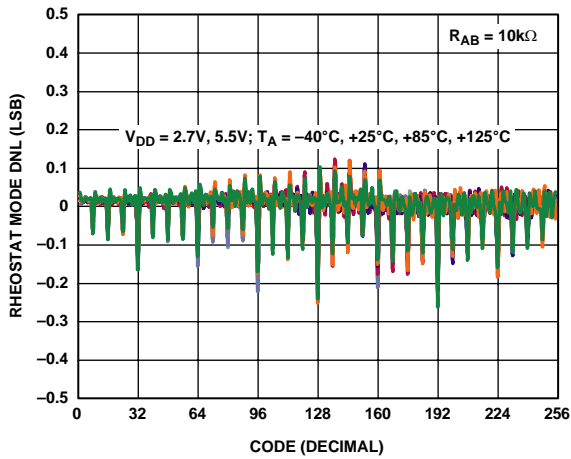


Figure 10. R-DNL vs. Code vs. Temperature

04104-0-009

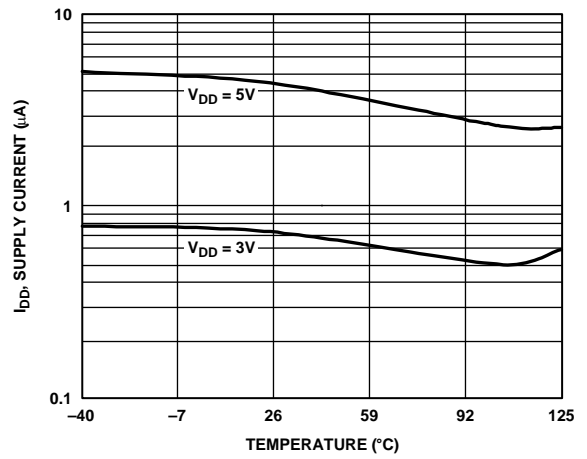


Figure 13. Supply Current vs. Temperature

04104-0-012

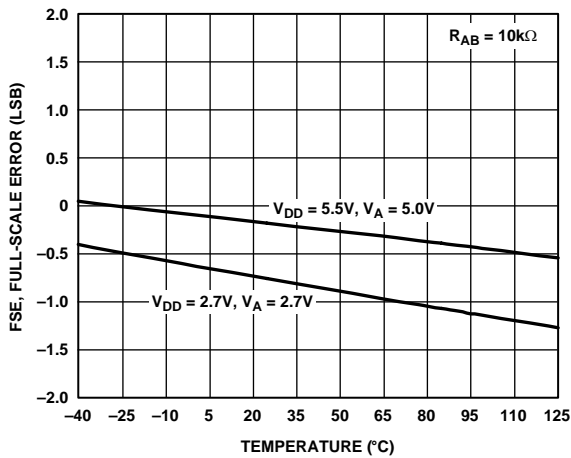


Figure 11. Full-Scale Error vs. Temperature

04104-0-010

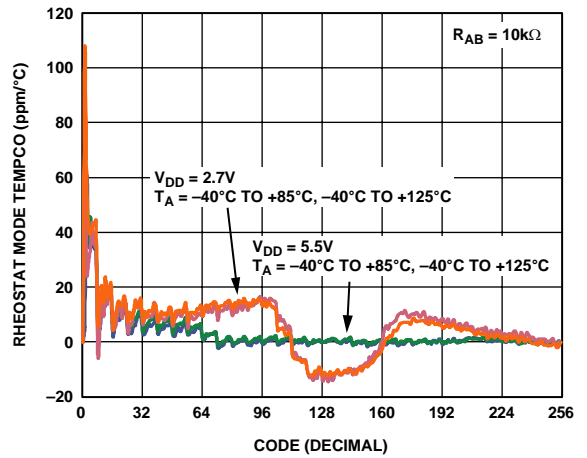


Figure 14. Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

04104-0-013

# AD5170

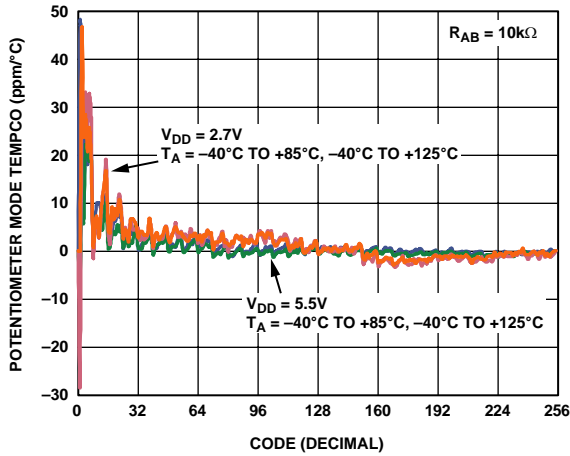


Figure 15. Potentiometer Mode Tempco  $\Delta V_{WB}/\Delta T$  vs. Code

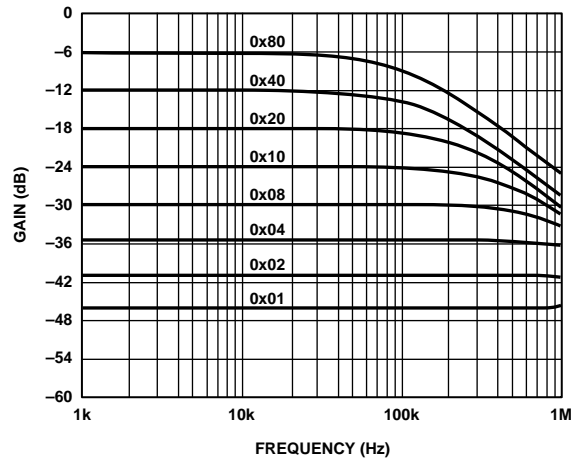


Figure 18. Gain vs. Frequency vs. Code,  $R_{AB} = 50 \text{ k}\Omega$

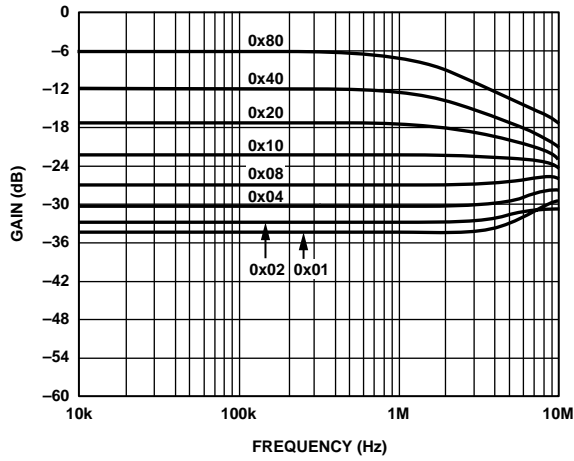


Figure 16. Gain vs. Frequency vs. Code,  $R_{AB} = 2.5 \text{ k}\Omega$

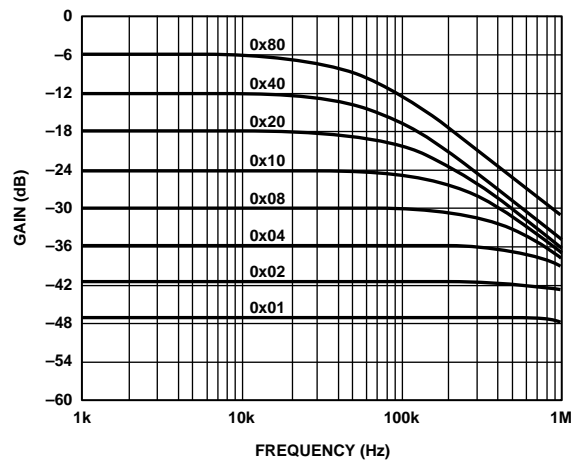


Figure 19. Gain vs. Frequency vs. Code,  $R_{AB} = 100 \text{ k}\Omega$

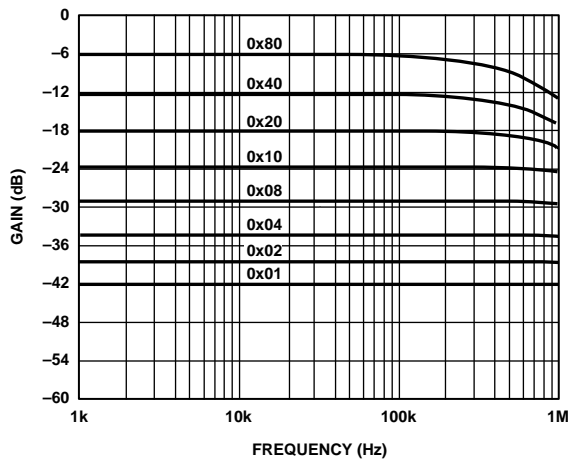


Figure 17. Gain vs. Frequency vs. Code,  $R_{AB} = 10 \text{ k}\Omega$

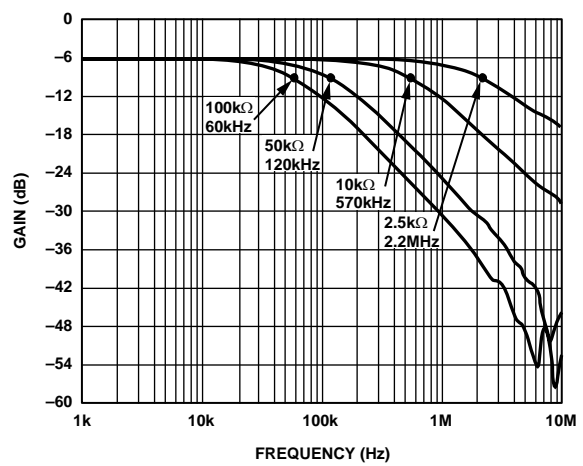


Figure 20. -3 dB Bandwidth at Code = 0x80

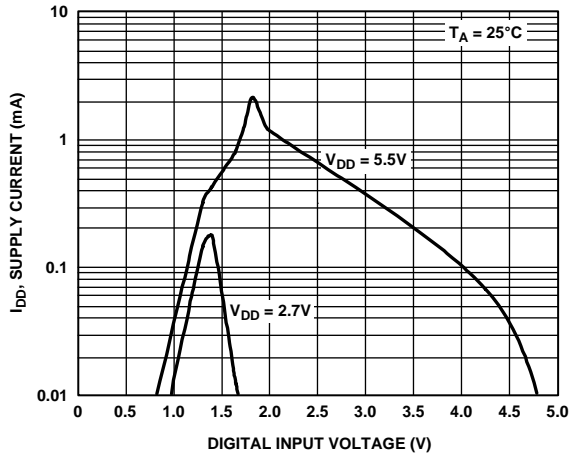


Figure 21.  $I_{DD}$  vs. Input Voltage

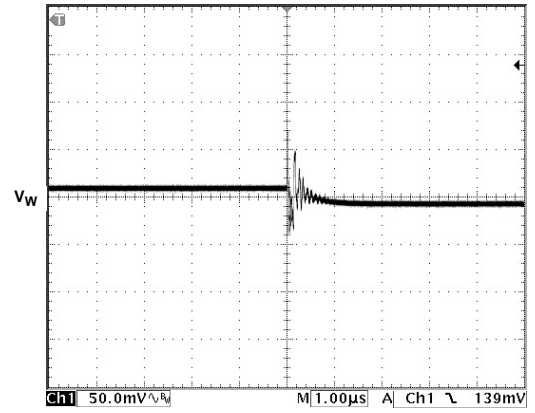


Figure 23. Midscale Glitch, Code 0x80 to Code 0x7F

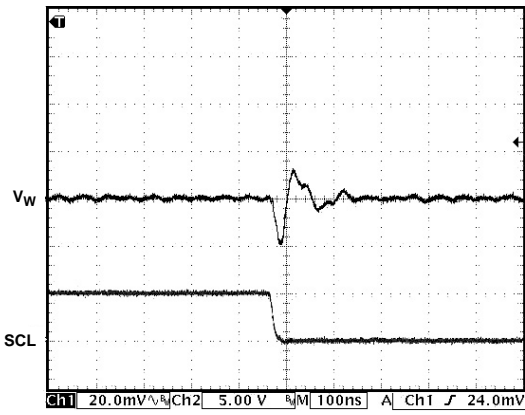


Figure 22. Digital Feedthrough

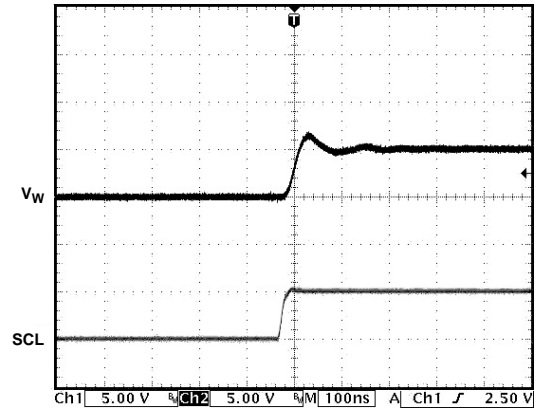


Figure 24. Large Signal Settling Time

04104-0-020

04104-0-025

04104-0-021

04104-0-023

## TEST CIRCUITS

Figure 25 to Figure 30 illustrate the test circuits that define the test conditions used in the product specification tables.

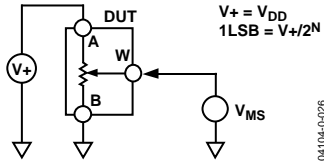


Figure 25. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

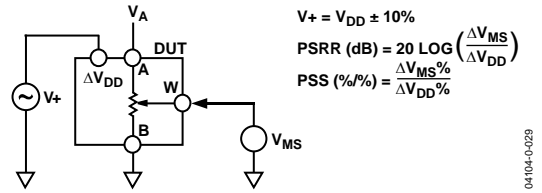


Figure 28. Test Circuit for Power Supply Sensitivity (PSS, PSRR)

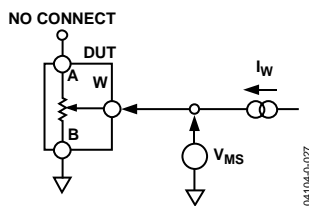


Figure 26. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

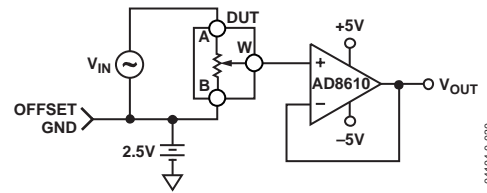


Figure 29. Test Circuit for Gain vs. Frequency

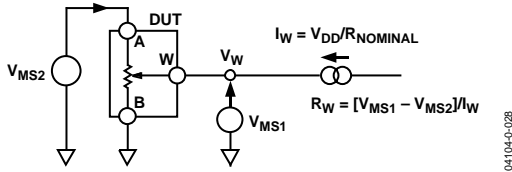


Figure 27. Test Circuit for Wiper Resistance

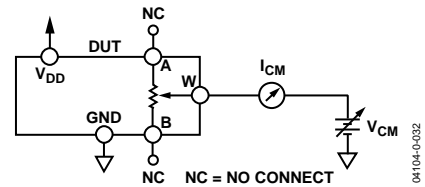


Figure 30. Test Circuit for Common-Mode Leakage Current

## THEORY OF OPERATION

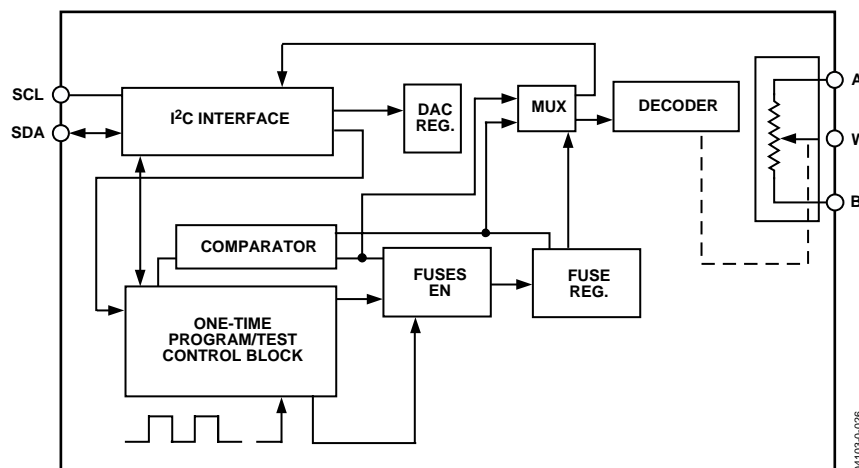


Figure 31. Detailed Functional Block Diagram

The AD5170 is a 256-position, digitally controlled, variable resistor (VR) that employs fuse link technology to achieve memory retention of resistance setting.

An internal power-on preset places the wiper at midscale during power-on. If the OTP function has been activated, the device powers up at the user-defined permanent setting.

### ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5170 presets to midscale during initial power-on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit high along with the proper coding (see Table 8 and Table 9) and one-time  $V_{DD\_OTP}$ . Note that fuse link technology of the AD517x family of digital potentiometers requires  $V_{DD\_OTP}$  between 5.25 V and 5.5 V to blow the fuses to achieve a given nonvolatile setting. On the other hand,  $V_{DD}$  can be 2.7 V to 5.5 V during operation. As a result, system supply that is lower than 5.25 V requires external supply for one-time programming. Note that the user is allowed only one attempt in blowing the fuses. If the user fails to blow the fuses at the first attempt, the fuses' structures may have changed such that they may never be blown regardless of the energy applied at subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back to check the programming status (see Table 9). Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses have been blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 31 shows a detailed functional block diagram.

### PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE—RHEOSTAT OPERATION

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 2.5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ . The nominal resistance ( $R_{AB}$ ) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

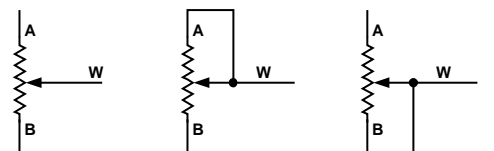


Figure 32. Rheostat Mode Configuration

Assuming a 10 k $\Omega$  part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 50  $\Omega$  wiper contact resistance, such a connection yields a minimum of 100  $\Omega$  ( $2 \times 50 \Omega$ ) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 139  $\Omega$  ( $R_{WB} = R_{AB}/256 + 2 \times R_W = 39 \Omega + 2 \times 50 \Omega$ ) for data 0x01. The third connection is the next tap point, representing 178  $\Omega$  ( $2 \times 39 \Omega + 2 \times 50 \Omega$ ) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100  $\Omega$  ( $R_{AB} + 2 \times R_W$ ).

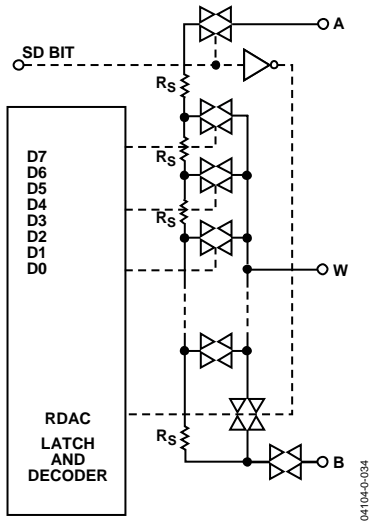


Figure 33. AD5170 Equivalent RDAC Circuit

The general equation that determines the digitally programmed output resistance between Terminal W and Terminal B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where  $D$  is the decimal equivalent of the binary code loaded in the 8-bit RDAC register,  $R_{AB}$  is the end-to-end resistance, and  $R_W$  is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if  $R_{AB} = 10 \text{ k}\Omega$  and the A terminal is open-circuited, the output resistance  $R_{WB}$  is set for the RDAC latch codes, as shown in Table 6.

Table 6. Codes and Corresponding  $R_{WB}$  Resistance

D (Dec.)	$R_{WB}$ ( $\Omega$ )	Output State
255	9,961	Full scale ( $R_{AB} - 1 \text{ LSB} + R_W$ )
128	5,060	Midscale
1	139	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of  $100 \Omega$  is present. Care should be taken to limit the current flow between Terminal W and Terminal B in this state to a maximum pulse current of no more than  $20 \text{ mA}$ . Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper, Terminal W, and Terminal A also produces a digitally controlled, complementary resistance,  $R_{WA}$ . When these terminals are used, the B terminal can be opened. Setting the resistance value for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

For  $R_{AB} = 10 \text{ k}\Omega$  and B terminal open circuited, Table 7 shows some examples of the output resistance ( $R_{WA}$ ) vs. RDAC latch codes.

Table 7. Codes and Corresponding  $R_{WA}$  Resistance

D (Dec.)	$R_{WA}$ ( $\Omega$ )	Output State
255	139	Full scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero scale

Typical device-to-device matching is process-lot dependent and may vary by up to  $\pm 30\%$ . Because the resistance element is processed using thin film technology, the change in  $R_{AB}$  with temperature has a very low  $35 \text{ ppm}/^\circ\text{C}$  temperature coefficient.

## PROGRAMMING THE POTENTIOMETER DIVIDER—VOLTAGE OUTPUT OPERATION

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A proportional to the input voltage at A to B. Unlike the polarity of  $V_{DD}$  to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

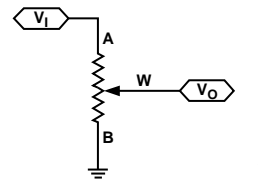


Figure 34. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to  $5 \text{ V}$  and the B terminal to ground produces an output voltage at the wiper to B starting at  $0 \text{ V}$  up to  $1 \text{ LSB}$  less than  $5 \text{ V}$ . Each  $\text{LSB}$  of voltage is equal to the voltage applied across Terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance,  $V_W$  can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in divider mode results in a more accurate operation over temperature. Unlike rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors,  $R_{WA}$  and  $R_{WB}$ , and not the absolute values. Thus, the temperature drift reduces to  $15 \text{ ppm}/^\circ\text{C}$ .



### ESD PROTECTION

All digital inputs—SDA, SCL, AD0, and AD1—are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 35 and Figure 36.

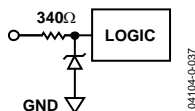


Figure 35. ESD Protection of Digital Pins

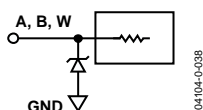


Figure 36. ESD Protection of Resistor Terminals

### TERMINAL VOLTAGE OPERATING RANGE

The AD5170  $V_{DD}$  to GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed  $V_{DD}$  or GND are clamped by the internal forward-biased diodes (see Figure 37).

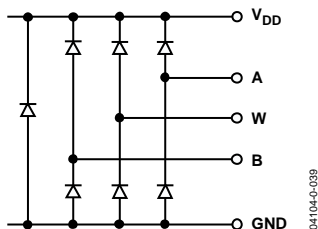


Figure 37. Maximum Terminal Voltages Set by  $V_{DD}$  and GND

### POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 37), it is important to power  $V_{DD}$ /GND before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that  $V_{DD}$  is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is GND,  $V_{DD}$ , the digital inputs, and then  $V_A/V_B/V_W$ . The relative order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and the digital inputs is not important as long as they are powered after  $V_{DD}$ /GND.

### POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies share the same  $V_{DD}$  terminal of the AD5170. The AD5170 employs fuse link technology that requires 5.25 V to 5.5 V for blowing the internal fuses to achieve a given setting, but normal  $V_{DD}$  can be anywhere between 2.7 V and 5.5 V after the fuse programming process. As a result, dual-voltage supplies and isolation are

needed if system  $V_{DD}$  is lower than the required  $V_{DD\_OTP}$ . The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.25 V to 5.5 V and able to provide a 100 mA current for 400 ms for successful one-time programming. Once fuse programming is completed, the  $V_{DD\_OTP}$  supply must be removed to allow normal operation at 2.7 V to 5.5 V, and the device consumes current in the  $\mu A$  range. Figure 38 shows the simplest implementation of a dual-supply requirement by using a jumper. This approach saves one voltage supply, but draws additional current and requires manual configuration.

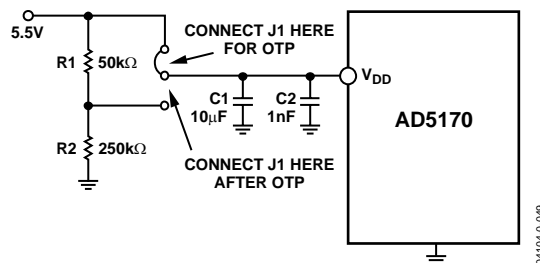


Figure 38. Power Supply Requirement

An alternate approach in 3.5 V to 5.25 V systems adds a signal diode between the system supply and the OTP supply for isolation, as shown in Figure 39. Note that the  $V_{DD\_OTP}$  must be removed once OTP is completed.

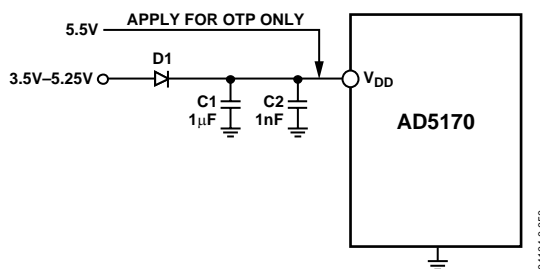


Figure 39. Isolate 5.5 V OTP Supply from 3.5 V to 5.25 V Normal Operating Supply

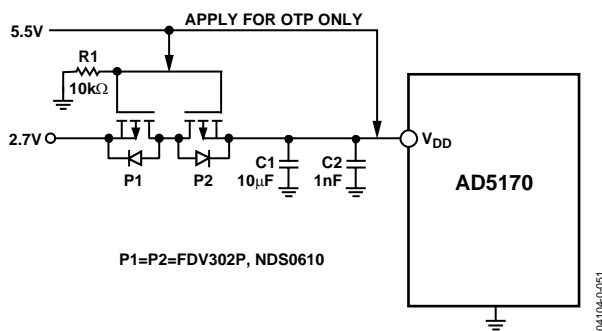


Figure 40. Isolate 5.5 V OTP Supply from 2.7 V Normal Operating Supply

# AD5170

For those who operate their systems at 2.7 V, use of the bidirectional, low threshold, P-Channel MOSFETs is recommended for the supply's isolation. As shown in Figure 40, this assumes that the 2.7 V system voltage is applied first, and the P1 and P2 gates are pulled to ground, thus turning on P1 and subsequently P2. As a result,  $V_{DD}$  of the AD5170 approaches 2.7 V. When the AD5170 setting is found, the factory tester applies the  $V_{DD\_OTP}$  to both the  $V_{DD}$  and the MOSFETs gates, turning off P1 and P2. The OTP command is executed at this time to program the AD5170 while the 2.7 V source is protected. Once the fuse programming is completed, the tester withdraws the  $V_{DD\_OTP}$  and the setting for AD5170 is permanently fixed.

The AD5170 achieves the OTP function by blowing internal fuses. Users should always apply the 5.25 V to 5.5 V one-time-program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement may lead to a change in the fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between  $0.7 V \times V_{DD}$  and  $V_{DD} + 0.5 V$ . Refer to the Level Shifting for Different Voltage Operation section.

Poor PCB layout introduces parasitics that may affect the fuse programming. Therefore, it is recommended to add a 10  $\mu\text{F}$  tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the  $V_{DD}$  pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides both a fast response and larger supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, while C2 reduces high frequency noise during normal operation.

## LAYOUT CONSIDERATIONS

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

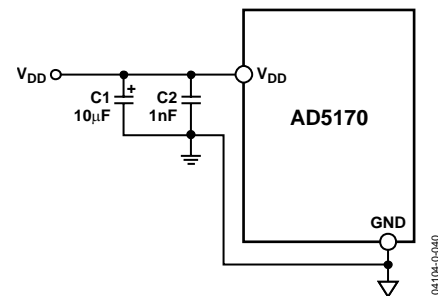


Figure 41. Power Supply Bypassing

## EVALUATION SOFTWARE/HARDWARE

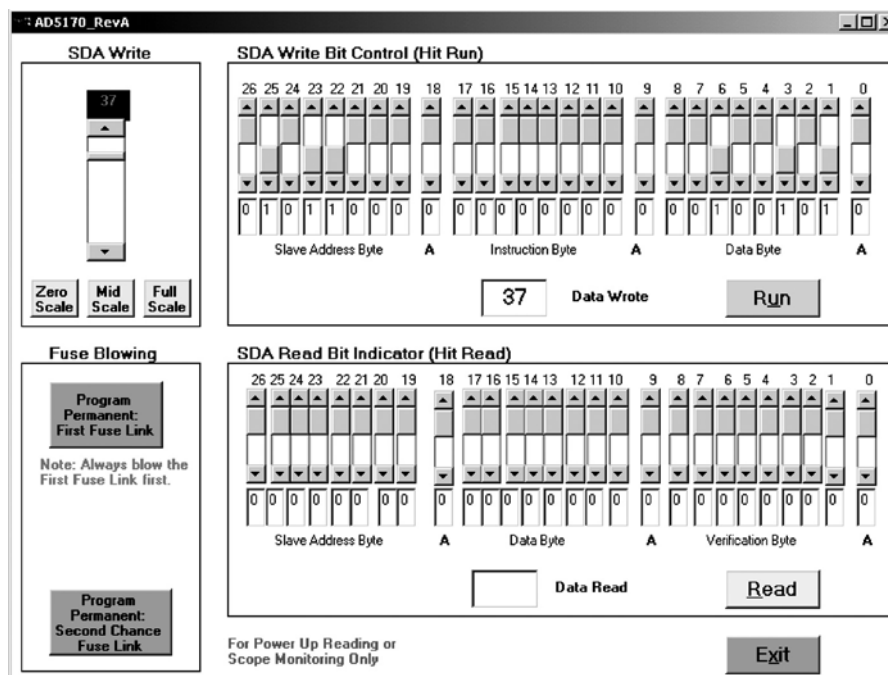


Figure 42. AD5170 Computer Software Interface

There are two ways of controlling the AD5170. Users can either program the devices with computer software or external I<sup>2</sup>C controllers.

### SOFTWARE PROGRAMMING

Due to the advantages of the one-time programmable feature, consider programming the device in the factory before shipping the final product to end users. ADI offers device programming software that can be implemented in the factory on PCs running Windows® 95 or later. As a result, external controllers are not required, which significantly reduces development time. The program is an executable file that does not require knowledge of programming languages or programming skills, and it is easy to set up and to use. Figure 42 shows the software interface. The software can be downloaded from [www.analog.com](http://www.analog.com).

The AD5170 starts at midscale after power-up prior to OTP programming. To increment or decrement the resistance, move the scroll bars on the left. To write any specific value, use the bit pattern in the upper screen and click **Run**. The format of writing data to the device is shown in Table 8. Once the desired setting is found, click **Program Permanent: First Fuse Link** to blow the internal fuse links.

To read the validation bits and data from the device, click **Read**. The format of the read bits is shown in Table 9.

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## DEVICE PROGRAMMING

To apply the device programming software in the factory, you modify a parallel port cable and configure Pin 2, Pin 3, Pin 15, and Pin 25 for SDA\_write, SCL, SDA\_read, and DGND, respectively, for the control signals (see Figure 43). You should also lay out the PCB of the AD5170 with SCL and SDA pads, as shown in Figure 44, such that pogo pins can be inserted for factory programming.

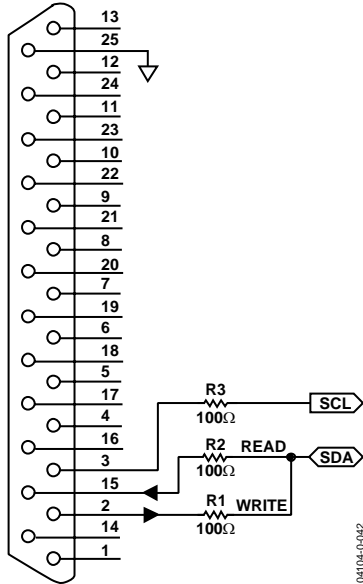


Figure 43. Parallel Port Connection

(Pin 2 = SDA\_write, Pin 3 = SCL, Pin 15 = SDA\_read, and Pin 25 = DGND)

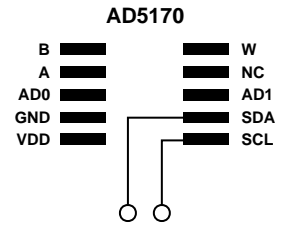


Figure 44. Recommended AD5170 PCB Layout

## I<sup>2</sup>C INTERFACE

Table 8 and Table 9 use the following codes:

S = Start condition.

P = Stop condition.

A = Acknowledge.

AD0, AD1 = Package pin-programmable address bits.

X = Don't care.

$\overline{W}$  = Write.

R = Read.

2T = Second fuse link array for two-time programming. Logic 0 corresponds to first trim. Logic 1 corresponds to second trim.

Note that blowing Trim 2 before Trim 1 effectively disables Trim 1 and, in turn, only allows one-time programming.

SD = Shutdown connects wiper to B terminal and open circuits the A terminal. It does not change the contents of the wiper register.

T = OTP programming bit. Logic 1 permanently programs the wiper.

OW = Overwrite the fuse setting and program the digital potentiometer to a different setting. Note that upon power-up, the digital potentiometer presets to either midscale or fuse setting depending on whether the fuse link has been blown.

D7, D6, D5, D4, D3, D2, D1, D0 = Data bits.

E1, E0 = OTP validation bits:

0, 0 = Ready to program.

1, 0 = Fatal error. Some fuses not blown. Do not retry.

Discard this unit.

1, 1 = Programmed successfully. No further adjustments are possible.

**Table 8. Write Mode**

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	2T	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Instruction Byte									Data Byte										

**Table 9. Read Mode**

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	X	A	P
Slave Address Byte									Instruction Byte									Data Byte											

## I<sup>2</sup>C-COMPATIBLE 2-WIRE SERIAL BUS

This section describes how the 2-wire I<sup>2</sup>C serial bus protocol operates.

The master initiates a data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 46). The following byte is the slave address byte, which consists of the slave address followed by an R/ $\overline{W}$  bit (this bit determines whether data is read from or written to the slave device). AD0 and AD1 are configurable address bits that allow up to four devices on one bus (see Table 8).

The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is called the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register. If the R/ $\overline{W}$  bit is high, the master reads from the slave device. If the R/ $\overline{W}$  bit is low, the master writes to the slave device.

In write mode, the second byte is the instruction byte. The first MSB, 2T, of the instruction byte is the second trim enable bit. A logic low selects the first array of fuses, and a logic high selects the second array. This means that after blowing the fuses with Trim 1, the user still has another chance to blow them again with Trim 2. Note that using Trim 2 before Trim 1 effectively disables Trim 1 and, in turn, only allows one-time programming.

The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A and shorts the wiper to Terminal B. This operation yields almost 0  $\Omega$  in rheostat mode or 0 V in potentiometer mode. Note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

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The third MSB, T, is the one-time programmable (OTP) programming bit. A logic high blows the polyfuses and programs the resistor setting permanently. For example, if the user wanted to blow the first array of fuses, the instruction byte would be 00100XXX. To blow the second array of fuses, the instruction byte would be 10100XXX. A logic low of the T bit simply allows the device to act as a typical volatile digital potentiometer.

The fourth MSB must always be Logic 0.

The fifth MSB, OW, is an overwrite bit. When raised to a logic high, OW allows the RDAC setting to be changed even after the internal fuses have been blown. However, once OW is returned to a Logic 0, the position of the RDAC returns to the setting prior to the overwrite. Because OW is not static, if the device is powered off and on, the RDAC presets to midscale or to the setting at which the fuses were blown, depending on whether the fuses have been permanently set.

The remainder of the bits in the instruction byte are don't care bits (see Figure 46).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 45).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from write mode, with eight data bits followed by an Acknowledge bit). Similarly, transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 47).

Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the one-time programming (see Figure 47).

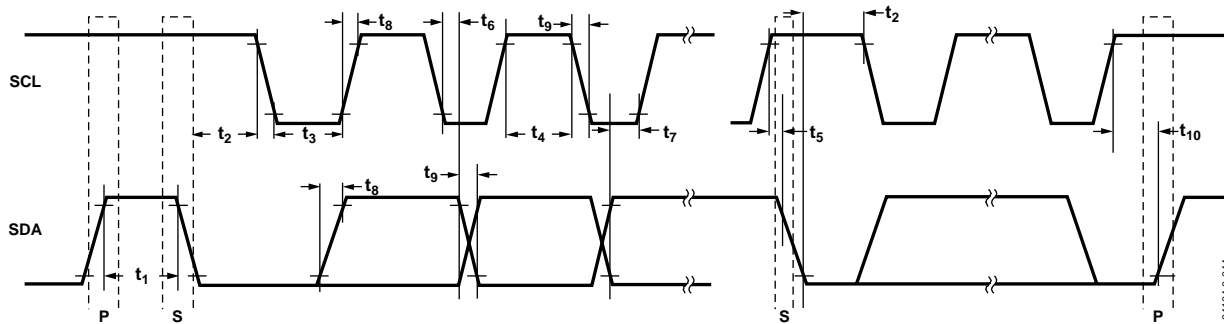


Figure 45. I<sup>2</sup>C Interface Detailed Timing Diagram

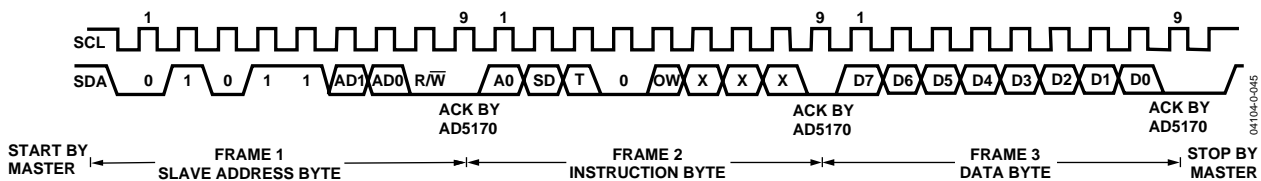


Figure 46. Writing to the RDAC Register

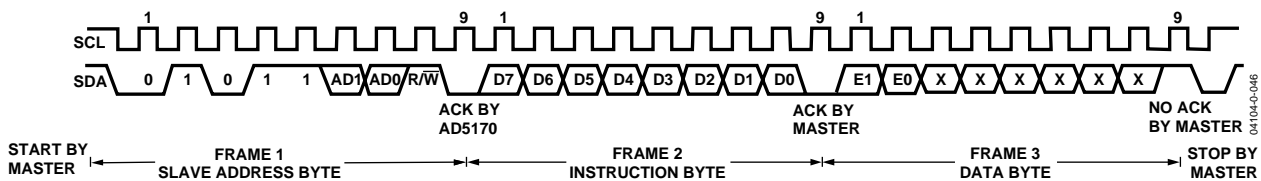


Figure 47. Reading Data from the RDAC Register

After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a STOP condition (see Figure 46). In read mode, the master issues a No Acknowledge for the 9th clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse and then brings the SDA line high to establish a STOP condition (see Figure 47).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Table 10. Validation Status

E1	E0	Status
0	0	Ready for programming.
1	0	Fatal error. Some fuses not blown. Do not retry. Discard this unit.
1	1	Successful. No further programming is possible.

**Multiple Devices on One Bus**

Figure 48 shows four AD5170s on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I<sup>2</sup>C-compatible interface.

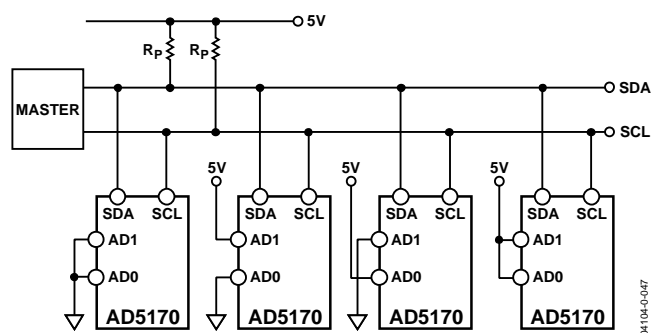


Figure 48. Multiple AD5170s on One I<sup>2</sup>C Bus

**LEVEL SHIFTING FOR DIFFERENT VOLTAGE OPERATION**

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum V<sub>IH</sub> level (0.7 V × V<sub>DD</sub>), level shift the signals for read/write communications between the AD5170 and the controller. Figure 49 shows one of the implementations. For example, when SDA1 is at 2.5 V, M1 turns off and SDA2 becomes 5 V. When the SDA1 is at 0 V, M1 turns on and the SDA2 approaches 0 V. As a result, proper level shifting is established. M1 and M2 should be low threshold, N-channel power MOSFETs, such as FDV301N.

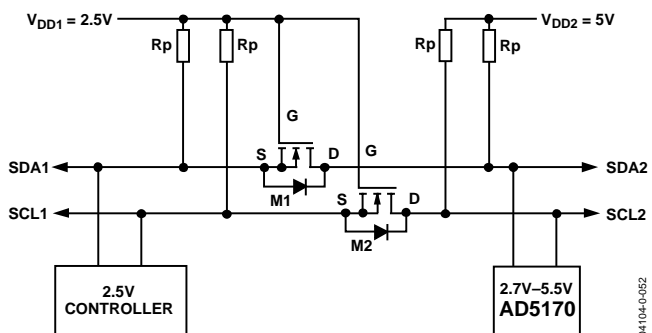
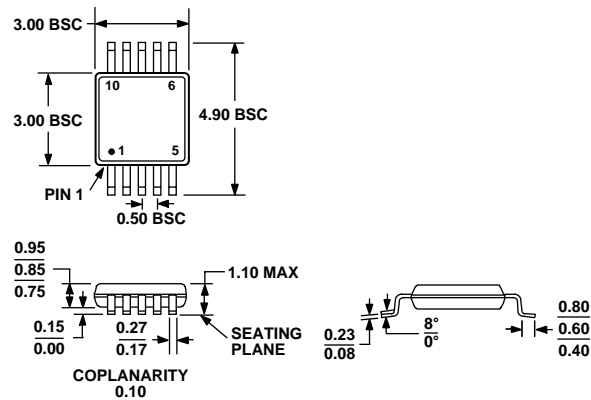


Figure 49. Level Shifting for Different Voltage Operation

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 50. 10-Lead Mini Small Outline Package [MINI\_SO]  
(RM-10)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	R <sub>AB</sub> (kΩ)	Temperature	Package Description	Package Option	Branding
AD5170BRM2.5	2.5	-40°C to +125°C	MSOP-10	RM-10	D0Y
AD5170BRM2.5-RL7	2.5	-40°C to +125°C	MSOP-10	RM-10	D0Y
AD5170BRMZ2.5 <sup>1</sup>	2.5	-40°C to +125°C	MSOP-10	RM-10	D8M
AD5170BRM10	10	-40°C to +125°C	MSOP-10	RM-10	D0Z
AD5170BRM10-RL7	10	-40°C to +125°C	MSOP-10	RM-10	D0Z
AD5170BRMZ10 <sup>1</sup>	10	-40°C to +125°C	MSOP-10	RM-10	D6S
AD5170BRMZ10-RL7 <sup>1</sup>	10	-40°C to +125°C	MSOP-10	RM-10	D6S
AD5170BRM50	50	-40°C to +125°C	MSOP-10	RM-10	D0W
AD5170BRM50-RL7	50	-40°C to +125°C	MSOP-10	RM-10	D0W
AD5170BRMZ50 <sup>1</sup>	50	-40°C to +125°C	MSOP-10	RM-10	D8L
AD5170BRM100	100	-40°C to +125°C	MSOP-10	RM-10	D0X
AD5170BRM100-RL7	100	-40°C to +125°C	MSOP-10	RM-10	D0X
AD5170BRMZ100 <sup>1</sup>	100	-40°C to +125°C	MSOP-10	RM-10	D8K
AD5170EVAL <sup>2</sup>			Evaluation Board		

<sup>1</sup> Z= Pb-free part.

<sup>2</sup> The evaluation board is shipped with the 10 kΩ RAB resistor option; however, the board is compatible with all available resistor value options.

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